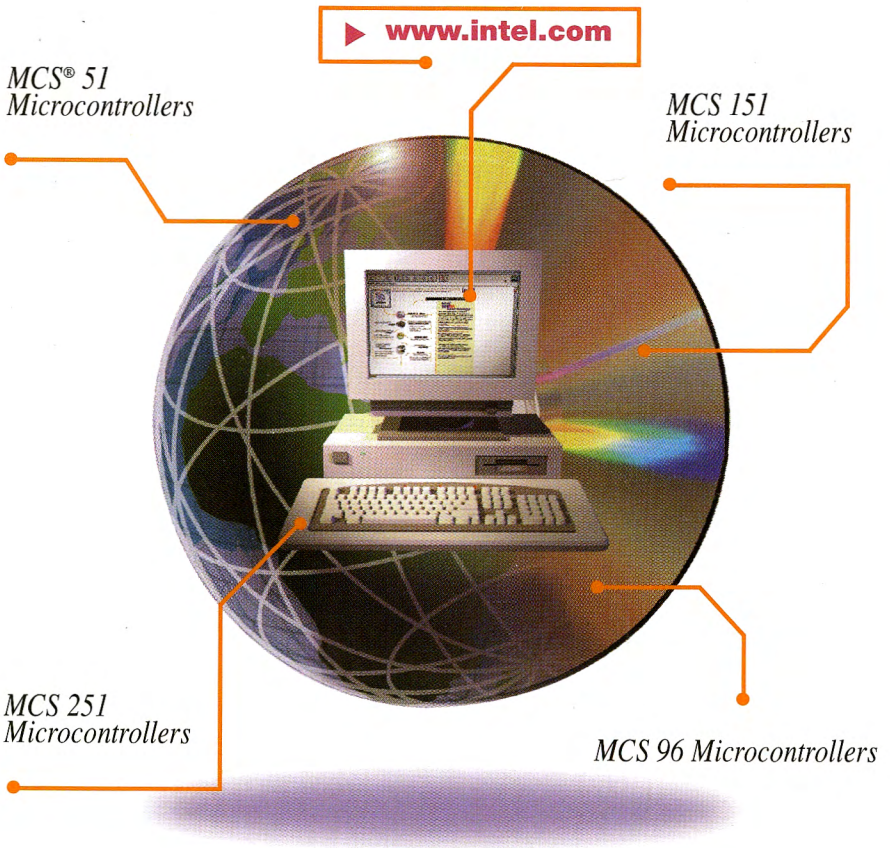
Embedded Microcontrollers



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Embedded Microcontrollers

MCS® 51 Microcontrollers, MCS 151 Microcontrollers, MCS 251 Microcontrollers, MCS 96 Microcontrollers

1997

DATASHEET DESIGNATIONS

Intel uses various datasheet markings to designate each phase of the document as it relates to the product. The markings appear in the lower inside corner of each datasheet page. Following are the definitions of each marking:

Datasheet Marking	Description
Product Preview	Contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available.
Advanced Information	Contains information on products being sampled or in the initial production phase of development.*
Preliminary	Contains preliminary information on new products in production.*
No Marking	Contains information on products in full production.*

*Specifications within these datasheets are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

November 1995

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CHAPTER 6
CAN 82527 Controller

Alphanumeric Index

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MCS®51 Microcontroller Family

87C51/80C51BH/80C31BH
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Commercial/Express

87C51/80C51BH/80C51BHP/80C31BH
***See Table 1 for Proliferation Options**

- **High Performance CHMOS EPROM**
- **24 MHz Operation**
- **Improved Quick-Pulse Programming Algorithm**
- **3-Level Program Memory Lock**
- **Boolean Processor**
- **128-Byte Data RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Extended Temperature Range (−40°C to +85°C)**
- **5 Interrupt Sources**
- **Programmable Serial Port**
- **TTL- and CMOS-Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **ONCE Mode Facilitates System Testing**
- **Power Control Modes**
  — Idle
  — Power Down

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 4 Kbytes of the program memory can reside on-chip (except 80C31BH). In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 128 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51/80C51BH/80C31BH is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS® 51 controller family, the 87C51/80C51BH/80C31BH uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 controller family of products.

The 80C51BHP is identical to the 80C51BH. When ordering the 80C51BHP, customers must submit the 64 byte encryption table together with the ROM code. Lock bit 1 will be set to enable the internal ROM code protection and at the same time allows code verification.

The extremely low operating power, along with the two reduced power modes, Idle and Power Down, make this part very suitable for low power applications. The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

For the remainder of this document, the 87C51, 80C51BH, and 80C31BH will be referred to as the 87C51/BH, unless information applies to a specific device.

December 1996

Order Number: 272335-004

Table 1. Proliferation Options

	*Standard	-1	-2	-24
80C31BH	X	X	X	X
80C51BH	X	X	X	X
80C51BHP	X	X	X	X
87C51	X	X	X	X

NOTES:
* 3.5 MHz to 12 MHz; V_{CC} = 5V ±20%
-1 3.5 MHz to 16 MHz; V_{CC} = 5V ±20%
-2 0.5 MHz to 12 MHz; V_{CC} = 5V ±20%
-24 3.5 MHz to 24 MHz; V_{CC} = 5V ±20%

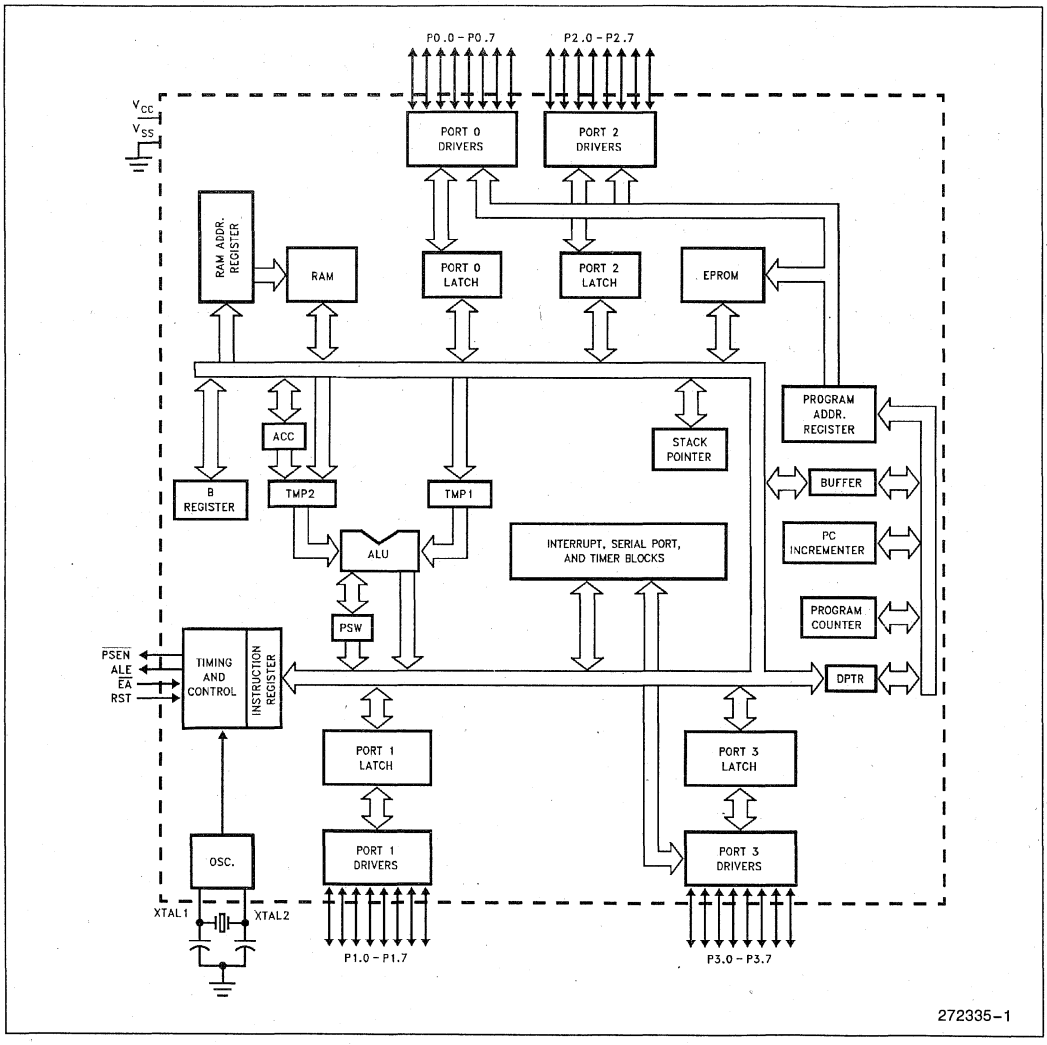


Figure 1. 87C51/BH Block Diagram

PROCESS INFORMATION

The 87C51/BH is manufactured on the CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order No. 210997.

PACKAGES

Part	Prefix	Package Type
87C51/BH	P	40-Pin Plastic DIP (OTP)
	D	40-Pin CERDIP (EPROM)
	N	44-Pin PLCC (OTP)
	S	44-Pin QFP (OTP)

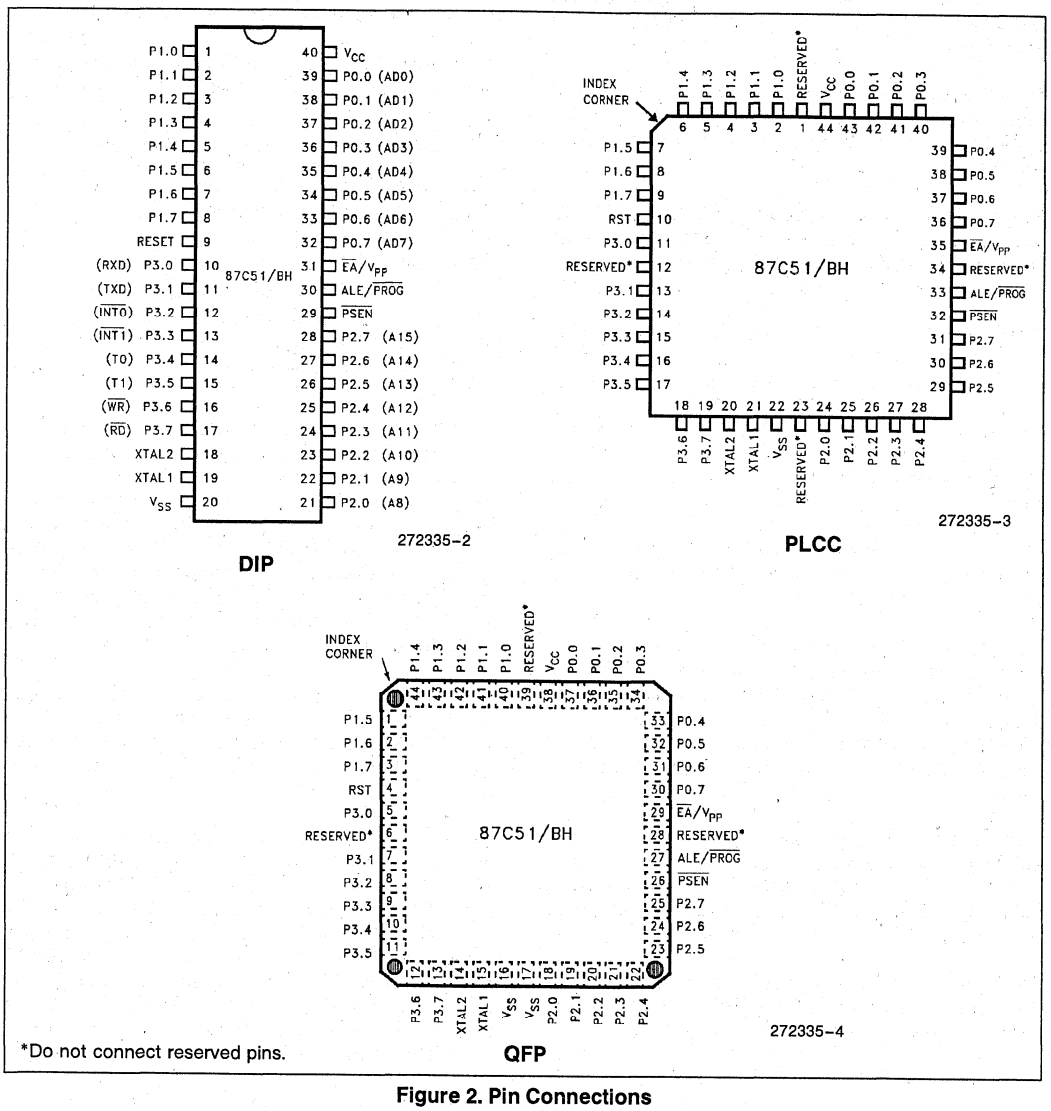


Figure 2. Pin Connections

PIN DESCRIPTION

V_{CC}: Supply voltage during normal, Idle and Power Down operations.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1's.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's.

During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives some control signals and the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial input line
P3.1	TXD	Serial output line
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 external input
P3.5	T1	Timer 1 external input
P3.6	$\overline{WR}$	External Data Memory Write strobe
P3.7	$\overline{RD}$	External Data Memory Read strobe

Port 3 also receives some control signals for EPROM programming and program verification.

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE/$\overline{PROG}$: Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming for the 87C51.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{\text{PSEN}}$: Program Store Enable is the Read strobe to External Program Memory. When the 87C51/BH is executing from Internal Program Memory, $\overline{\text{PSEN}}$ is inactive (high). When the device is executing code from External Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to External Data Memory.

$\overline{\text{EA}}$/V_{PP}: External Access enable. $\overline{\text{EA}}$ must be strapped to V_{SS} in order to enable the 87C51/BH to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits is programmed, the logic level at $\overline{\text{EA}}$ is internally latched during reset.

$\overline{\text{EA}}$ must be strapped to V_{CC} for internal program execution.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

For the 80C31BH, the $\overline{\text{EA}}$ function is connected directly to V_{SS} internally and is not connected to the external pin.

For a new system design, there is no requirement to connect the $\overline{\text{EA}}$ pin to V_{SS} externally.

For old and existing designs, the $\overline{\text{EA}}$ pin can continue to be connected to V_{SS} externally without losing compatibility.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

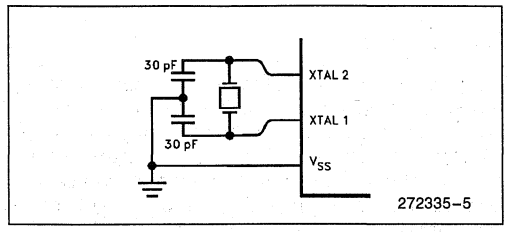


Figure 3. Using the On-Chip Oscillator

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

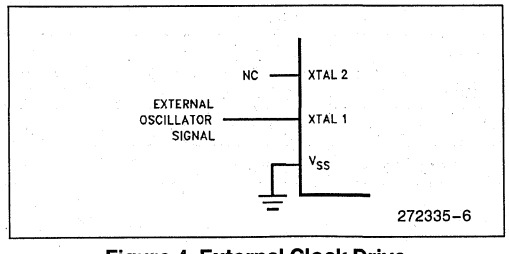


Figure 4. External Clock Drive

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Functions Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when Idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is transmitted.

On the 87C51/BH only a hardware reset can cause an exit from Power Down. Reset redefines all the SFR's but does not change the on-chip RAM.

To properly terminate Power Down, the reset should not be executed before V_{CC} is restored to its normal operating level, and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

DESIGN CONSIDERATIONS

- Exposure to light when the device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.
- The 87C51/BH now have some additional features. The features are: asynchronous port reset, 4 interrupt priority levels, power off flag, ALE disable, serial port automatic address recognition, serial port framing error detection, 64-byte encryption array, and 3 program lock bits. These features cannot be used with the older versions of 80C51BH/80C31BH. The newer version of 80C51BH/80C31BH will have change identifier "A" appended to the lot number.

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

ONCE MODE

The ONCE ("On-Circuit Emulation") mode facilitates testing and debugging of systems using the 87C51/BH without the 87C51/BH having to be removed from the circuit. The ONCE mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51/BH is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

87C51/BH EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial temperature.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 160 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 3.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

Table 3. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-in
P	Plastic	Commercial	No
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
S	QFP	Commercial	No
TP	Plastic	Extended	No
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
TS	QFP	Extended	No
LP	Plastic	Extended	Yes
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes

NOTE:
Contact distributor or local sales office to match EXPRESS prefix to proper device.

Examples:

P87C51 indicates 87C51 in a plastic package and specified for commercial temperature range, without burn-in.

LD87C51 indicates 87C51 in a cerdip package and specified for extended temperature range with burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
Maximum I_{OL} per I/O Pin ..... 15 mA
Power Dissipation..... 1.5W
(Based on package heat transfer limitations, not device power consumption.)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Unit
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
f_{OSC}	Oscillator Frequency			MHz
	87C51/BH	3.5	12	
	87C51-1/BH-1	3.5	16	
	87C51-2/BH-2	0.5	12	
	87C51-24/BH-24	3.5	24	

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage					
	Commercial	−0.5		$0.2\ V_{CC} - 0.1$	V	
	Express	−0.5		$0.2\ V_{CC} - 0.15$	V	
V_{IL1}	Input Low Voltage $\overline{EA}$					
	Commercial	0		$0.2\ V_{CC} - 0.3$	V	
	Express	−0.5		$0.2\ V_{CC} - 0.35$	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)					
	Commercial	$0.2\ V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
	Express	$0.2\ V_{CC} + 1$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)					
	Commercial	$0.7\ V_{CC}$		$V_{CC} + 0.5$	V	
	Express	$0.7\ V_{CC} + 0.1$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage(6) (Ports 1, 2, 3)			0.3	V	$I_{OL} = 100\ \mu A$(2)
				0.45	V	$I_{OL} = 1.6$ mA(2)
				1.0	V	$I_{OL} = 3.5$ mA(2)

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{OL1}	Output Low Voltage(6) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA(2)
				0.45	V	I_{OL} = 3.2 mA (2)
				1.0	V	I_{OL} = 7.0 mA(2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −30 μA(3)
		V_{CC} − 1.5			V	I_{OH} = −60 μA(3)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC} − 0.3			V	I_{OH} = −200 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA(3)
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA(3)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3) Commercial Express			 −50 −75	 μA μA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) Commercial Express			 −650 −750	 μA μA	V_{IN} = 2V
RRST	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10		pF	@ 1 MHz, 25°C
I_{CC}	Power Supply Current Active Mode @ 12 MHz @ 12 MHz (Note 6) @ 16 MHz @ 16 MHz (Note 6) @ 24 MHz @ 24 MHz (Note 6) @ 33 MHz (Note 6) Idle Mode @ 12 MHz @ 12 MHz (Note 6) @ 16 MHz @ 16 MHz (Note 6) @ 24 MHz @ 24 MHz (Note 6) @ 33 MHz (Note 6) Power Down Mode		 11.5 14.5 18 24.5 32.5 3.5 8 9.5 11.5 13.5 5	 20 25 26 30 38 40 45 7.5 9.5 9.5 11.5 13.5 15.5 17 50	 mA mA mA mA mA mA mA mA mA mA mA mA mA mA μA	(Note 4)

NOTES:
1. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temp, 5V.
2. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. See Figures 6 through 8 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:	10 mA
Maximum I_{OL} per 8-bit port—	
Port 0:	26 mA
Ports 1, 2, and 3:	15 mA
Maximum total I_{OL} for all output pins:	71 mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink greater than the listed test conditions.
6. These values are valid for the 80C51BH, 80C31BH and the 80C51BHP only.

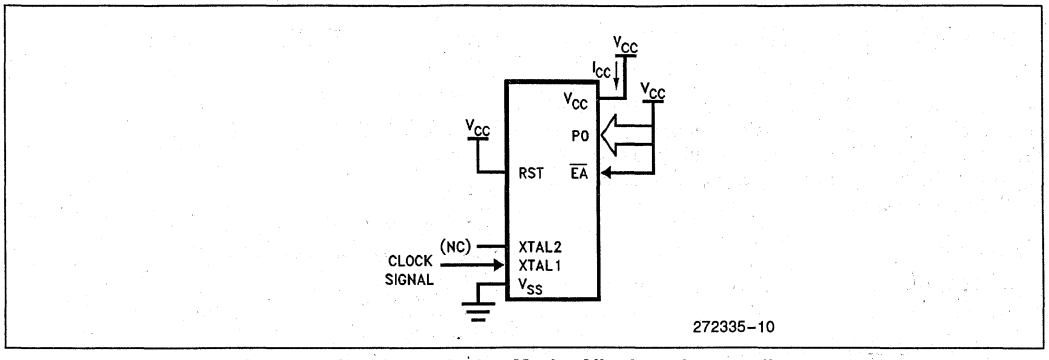


Figure 6. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

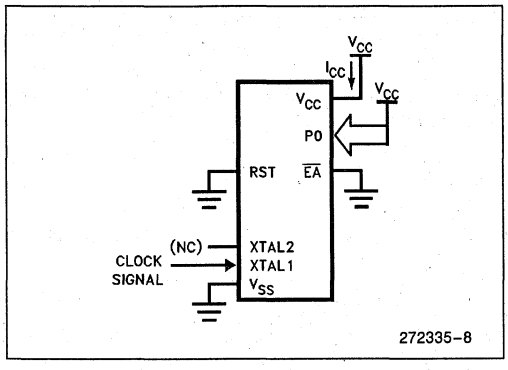


Figure 7. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

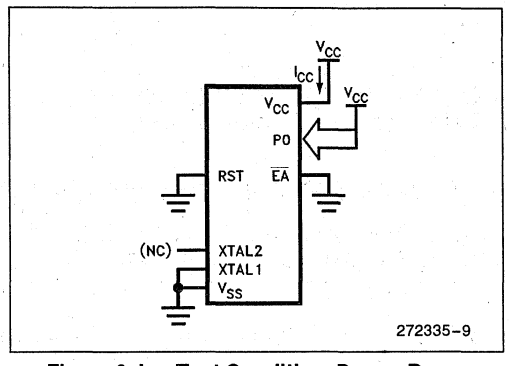


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected. V_{CC} = 2V to 5.5V.

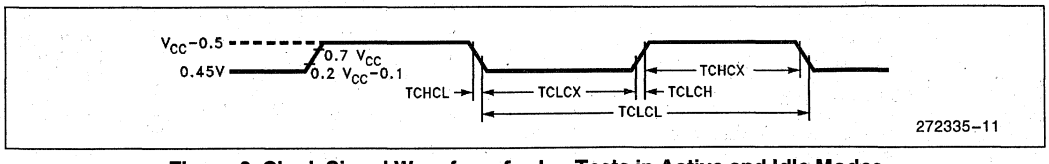


Figure 8. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A:Address.
C:Clock.
D:Input data.
H:Logic level HIGH.
I:Instruction (program memory contents).
L:Logic level LOW, or ALE.
P:$\overline{\text{PSEN}}$.
Q:Output data.
R:$\overline{\text{RD}}$ signal.
T:Time.
V:Valid.
W:$\overline{\text{WR}}$ signal.
X:No longer a valid logic level.
Z:Float.

For example,

TAVLL = Time from Address Valid to ALE Low.
TLLPL = Time from ALE Low to PSEN Low.

AC CHARACTERISTICS: (Over Operating Conditions; Load Capacitance for Port 0, ALE, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2.

Symbol	Parameter	Oscillator						Units
		12 MHz		24 MHz		Variable		
		Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 87C51/BH 87C51-1/BH-1 87C51-2/BH-2 87C51-24/BH-24					 3.5 3.5 0.5 3.5	 12 16 12 24	 MHz MHz MHz MHz
TLHLL	ALE Pulse Width	127		43		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low 87C51/BH 87C51-24/BH-24	43		 12		 TCLCL−40 TCLCL−30		 ns ns
TLLAX	Address Hold After ALE Low	53		12		TCLCL−30		ns
TLLIV	ALE Low to Valid Instr In 87C51/BH 87C51-24/BH-24		234		 91		4TCLCL−100 4TCLCL−75	 ns ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		12		TCLCL−30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		80		3TCLCL−45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instr In 87C51/BH 87C51-24/BH-24		145		 35		3TCLCL−105 3TCLCL−90	 ns ns

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2. (Continued)

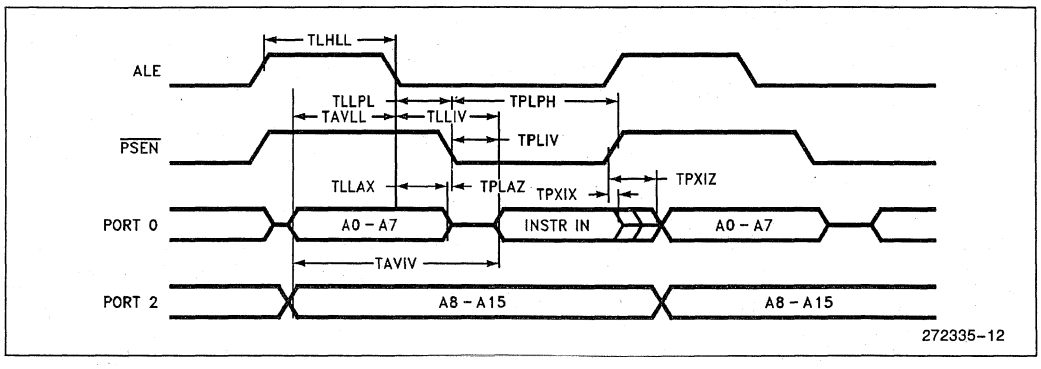
Symbol	Parameter	Oscillator						Units
		12 MHz		24 MHz		Variable		
		Min	Max	Min	Max	Min	Max	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$ 87C51/BH 87C51-24/BH-24		59		 21		 TCLCL−25 TCLCL−20	 ns ns
TAVIV	Address to Valid Instr In		312		103		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		150		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		150		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In 87C51/BH 87C51-24/BH-24		252		 113		 5TCLCL−165 5TCLCL−95	 ns ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		23		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In 87C51/BH 87C51-24/BH-24		517		 243		 8TCLCL−150 8TCLCL−90	 ns ns
TAVDV	Address to Valid Data In 87C51/BH 87C51-24/BH-24		585		 285		 9TCLCL−165 9TCLCL−90	 ns ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	75	175	3TCLCL−50	3TCLCL+ 50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low 87C51/BH 87C51-24/BH-24	 203		 77		 4TCLCL−130 4TCLCL−90		 ns ns
TQVWX	Data Valid to $\overline{WR}$ Transition 87C51/BH 80C51-24/BH-24	 33		 12		 TCLCL−50 TCLCL−30		 ns ns

EXTERNAL MEMORY CHARACTERISTICS

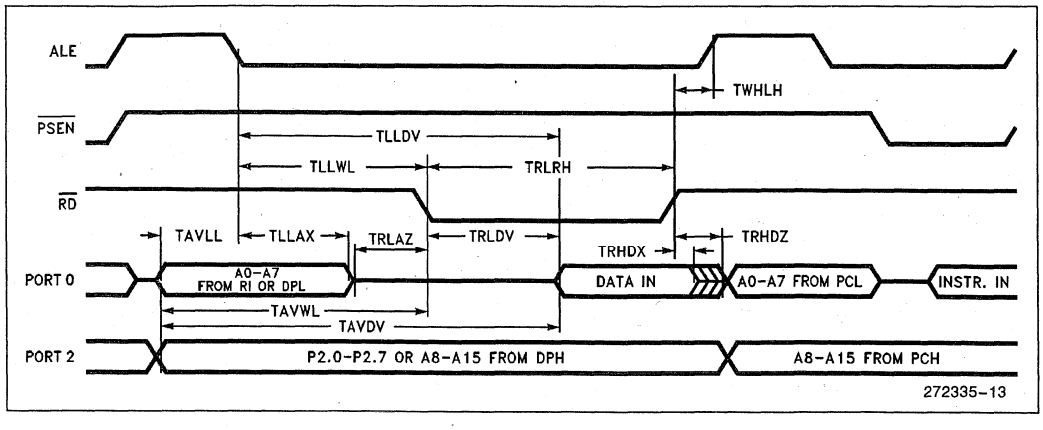
All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2. (Continued)

Symbol	Parameter	Oscillator						Units
		12 MHz		24 MHz		Variable		
		Min	Max	Min	Max	Min	Max	
TWHQX	Data Hold After $\overline{WR}$							
	87C51/BH	33				TCLCL−50		ns
	87C51-24/BH-24			7		TCLCL−35		ns
TQVWH	Data Valid to $\overline{WR}$ High							
	87C51/BH	433				7TCLCL−150		ns
	87C51-24/BH-24			222		7TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High							
	87C51/BH	43	123			TCLCL−40	TCLCL+40	ns
	87C51-24/BH-24			12	71	TCLCL−30	TCLCL+30	ns

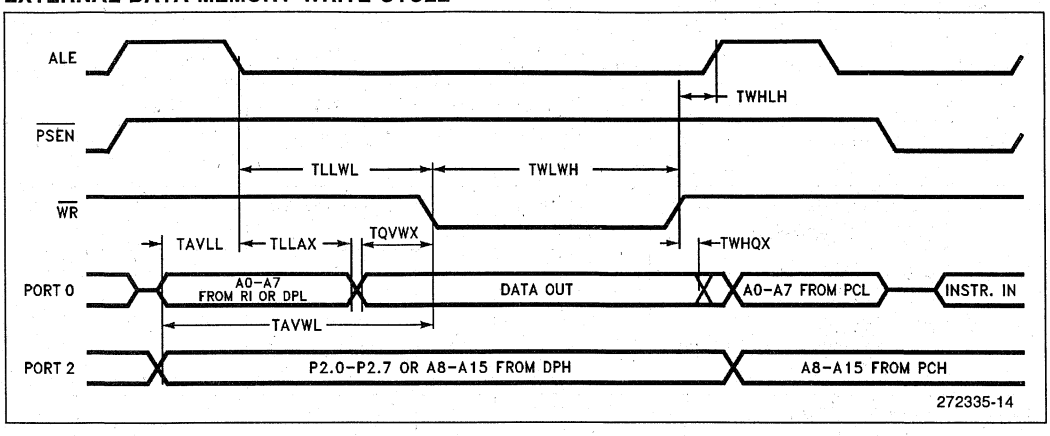
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

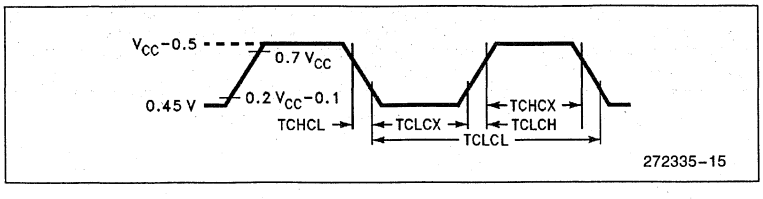


EXTERNAL CLOCK DRIVE

All parameter values apply to all devices unless otherwise indicated. In this table, 87C51/BH refers to 87C51/BH, 87C51-1/BH-1 and 87C51-2/BH-2.

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency			
	87C51/BH	3.5	12	MHz
	87C51-1/BH-1	3.5	16	MHz
	87C51-2/BH-2	0.5	12	MHz
	87C51-24/BH-24	3.5	24	MHz
TCHCX	High Time			
	87C51/BH	20		ns
	8751-24/BH-24	0.35TCLCL	0.65TCLCL	ns
TCLCX	Low Time			
	87C51/BH	20		ns
	87C51-24/BH-24	0.35TCLCL	0.65TCLCL	ns
TCLCH	Rise Time			
	87C51/BH		20	ns
	87C51-24/BH-24		10	ns
TCHCL	Fall Time			
	87C51/BH		20	ns
	87C51-24/BH-24		10	ns

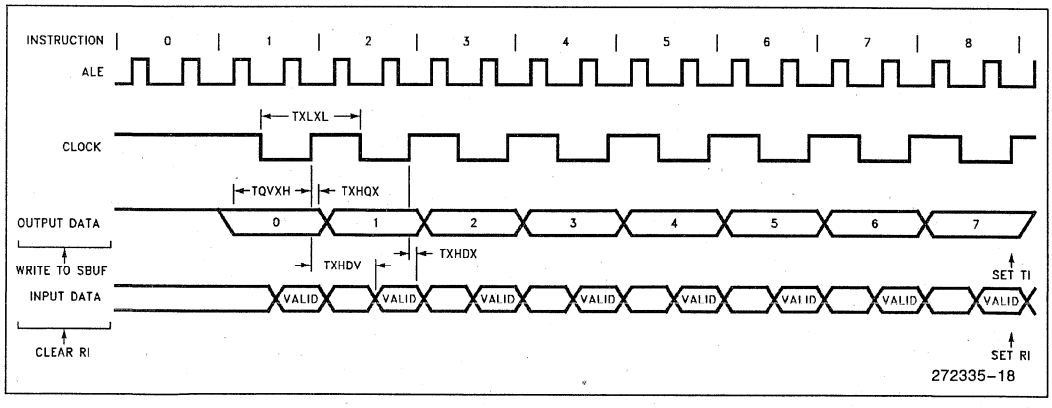
EXTERNAL CLOCK DRIVE WAVEFORM



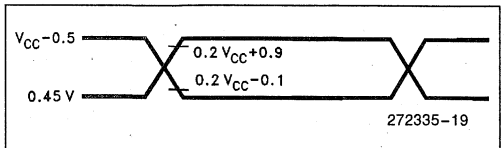
SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	12 MHz Oscillator		24 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		0.500		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		284		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge 87C51/BH 87C51-24/BH-24	50		34		2TCLCL−117 2TCLCL−34		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		283		10TCLCL−133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS

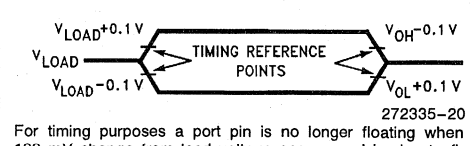


AC TESTING INPUT, OUTPUT WAVEFORMS



AC inputs during testing are driven at V_{CC} − 0.5 for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ±20 mA.

PROGRAMMING THE 87C51

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 4. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4 respectively for A0–A14.

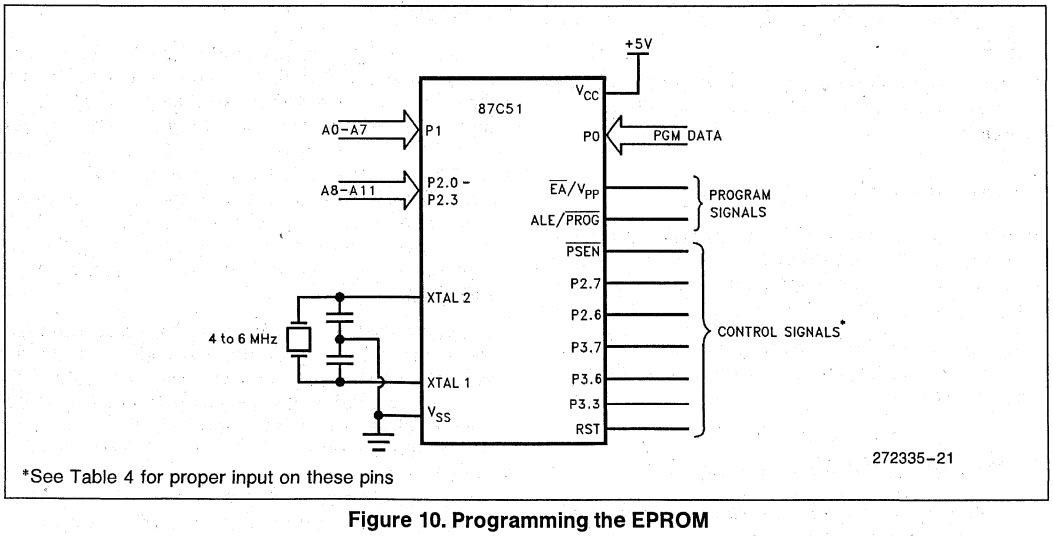
DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7.

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$.

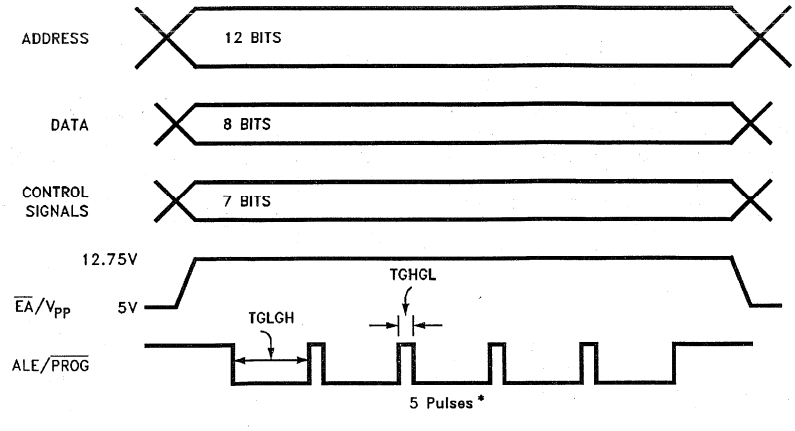
Table 4. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⎍	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3F		H	L	⎍	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⎍	12.75V	H	H	H	H	H
	Bit 2	H	L	⎍	12.75V	H	H	H	L	L
	Bit 3	H	L	⎍	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 4 for proper input on these pins

Figure 10. Programming the EPROM



*For compatibility, 25 pulses may be used.

Figure 11. Programming Waveforms

PROGRAMMING ALGORITHM

Refer to Table 4 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times* for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

Program Verify

Verification may be done after programming either one byte or a block of bytes. In either case a complete verify of the array will ensure reliable programming of the 87C51.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

ROM and EPROM Lock System

The program lock system, when programmed, protects the onboard program against software piracy.

The 80C51BH has a one level program lock system and a 64-byte encryption table. If program protection is desired, the user submits the encryption table with their code and both the lock bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table. The 87C51 has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 5.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 4 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C51 has 3 programmable lock bits that when programmed according to Table 5 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM will erase the encryption array but NOT the program lock bits. This means that after the lock bits are programmed, even though the EPROM is erased, the users will not be able to reprogram the EPROM. This improved security feature will provide a higher sense of security to the users. The users are therefore advised to finalize their code before programming the lock bits.

Reading the Signature Bytes

The 87C51 and 80C51BH have 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 4 for Read Signature Byte.

Location	Device	Contents
30H	All	89H
31H	All	58H
60H	87C51	51H
	80C51BH	11H

Erasure Characteristics (Windowed Devices Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1's state.

Table 5. Program Lock Bits and the Features

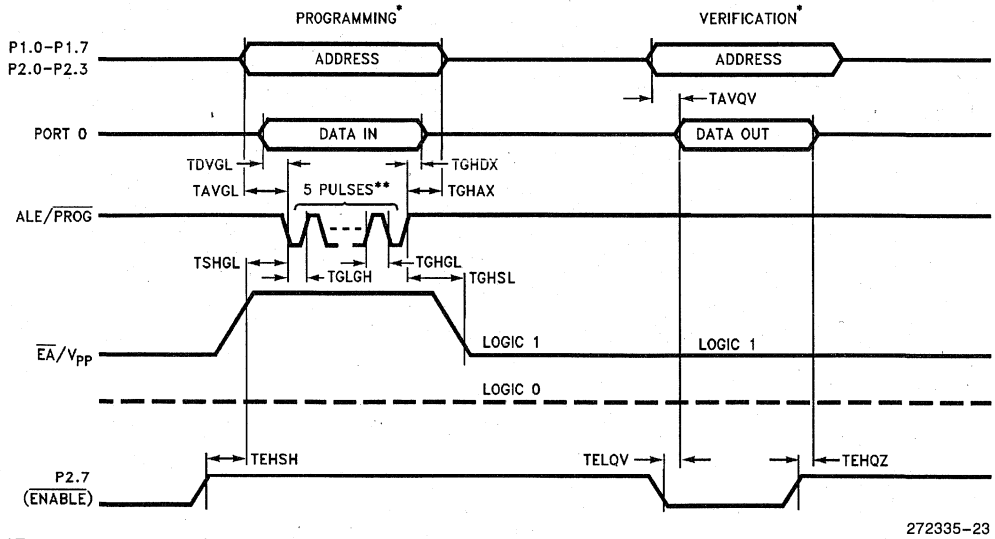
Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

EPROM PROGRAMMING, EPROM AND ROM VERIFICATION CHARACTERISTICS:

(T_A = 21°C to 27°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold After $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING, EPROM AND ROM VERIFICATION WAVEFORMS



*For programming conditions see Figure 10.
**5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel Packaging Handbook (Order No. 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
P	45°C/W	16°C/W	87C51
	75°C/W	23°C/W	BH
D	45°C/W	15°C/W	87C51
	36°C/W	13°C/W	BH
N	46°C/W	16°C/W	All
S	98°C/W	24°C/W	All

DATA SHEET REVISION HISTORY

Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this datasheet (272335-003) and the previous version (272335-002):

1. Removed −20 and −3 spec, replaced with −24 spec.
2. Added −24 spec.
3. 80C51BHP is replaced by 80C51BH with 64-byte encryption table submitted and lock bit 1 set.
4. 80C51BH/80C31BH are now having some additional features as 87C51.
5. Revised PRST value and I_{CC} idle values.
6. Added P3.3 control pin to programming and verification.
7. Added 80C51BH signature byte.

The following differences exist between the "-002" and the "-001" version of the 87C51/80C51BH/80C31BH datasheet.

1. Removed −L, I_{OL} = ±10 mA from Float Waveforms figure.

2. Removed QP, QD and QN (commercial with extended burn-in) from Table 3. Prefix Identification.

This data sheet (272335-001) replaces the following:

80C51BH/80C31BH Express	270218-003
80C51BHP	270603-004
87C51/80C51BH/80C31BH	270147-008
87C51 Express	270430-002
87C51-20/-3	272082-002

8XC52/54/58
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Commercial/Express

87C52/80C52/80C32/87C54/80C54/87C58/80C58

*See Table 1 for Proliferation Options

- **High Performance CHMOS EPROM/ ROM/CPU**
- **12/24/33 MHz Operations**
- **Three 16-Bit Timer/Counters**
- **Programmable Clock Out**
- **Up/Down Timer/Counter**
- **Three Level Program Lock System**
- **8K/16K/32K On-Chip Program Memory**
- **256 Bytes of On-Chip Data RAM**
- **Improved Quick Pulse Programming Algorithm**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **6 Interrupt Sources**
- **Programmable Serial Channel with:**
  - **Framing Error Detection**
  - **Automatic Address Recognition**
- **TTL and CMOS Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS® 51 Microcontroller Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE (On-Circuit Emulation) Mode**
- **Four-Level Interrupt Priority**
- **Extended Temperature Range Except for 33 MHz Offering (−40°C to +85°C)**

MEMORY ORGANIZATION

ROM Device	EPROM Version	ROMless Version	ROM/EPROM Bytes	RAM Bytes
80C52	87C52	80C32	8K	256
80C54	87C54	80C32	16K	256
80C58	87C58	80C32	32K	256

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 8XC52/8XC54/8XC58 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS 51 family of controllers, the 8XC52/8XC54/8XC58 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 family of products. The 8XC52/8XC54/8XC58 is an enhanced version of the 87C51/80C51BH/80C31BH. The added features make it an even more powerful microcontroller for applications that require clock output, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

Throughout this document 8XC5X will refer to the 8XC52, 80C32, 8XC54 and 8XC58 unless information applies to a specific device.

March 1996

Order Number: 272336-004

Table 1. Proliferations Options

	Standard*1	-1	-2	-24	-33
80C32	X	X	X	X	X
80C52	X	X	X	X	X
87C52	X	X	X	X	X
80C54	X	X	X	X	X
87C54	X	X	X	X	X
80C58	X	X	X	X	X
87C58	X	X	X	X	X

NOTES:
*1 3.5 MHz to 12 MHz; 5V ±20%
-1 3.5 MHz to 16 MHz; 5V ±20%
-2 0.5 MHz to 12 MHz; 5V ±20%
-24 3.5 MHz to 24 MHz; 5V ±20%
-33 3.5 MHz to 33 MHz; 5V ±10%

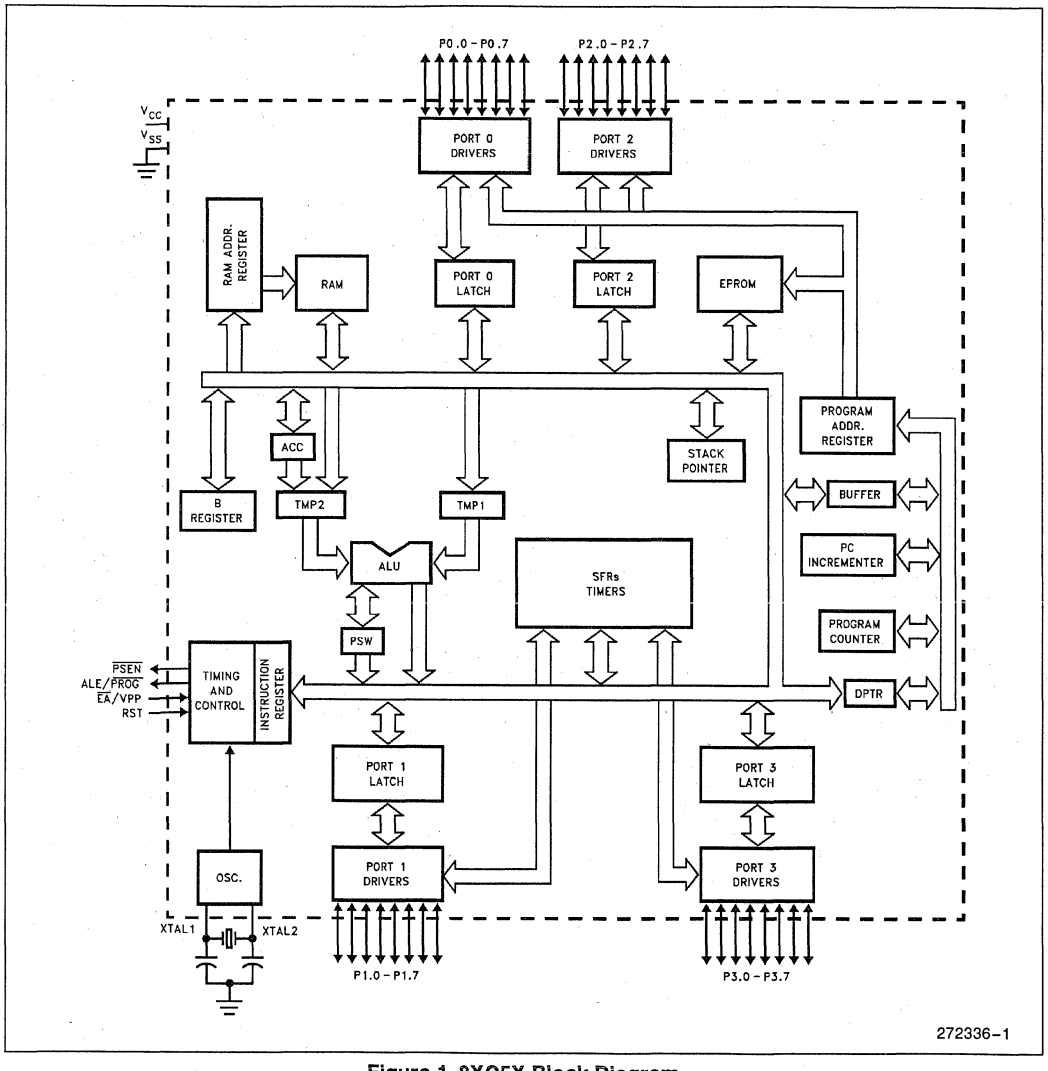


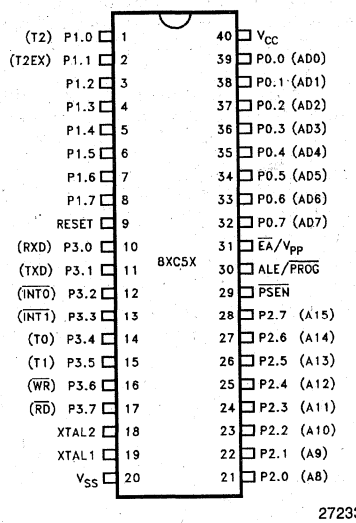
Figure 1. 8XC5X Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order No. 210997.

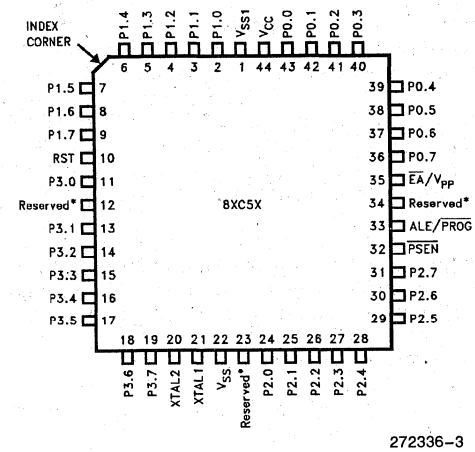
PACKAGES

Part	Prefix	Package Type
8XC5X	P	40-Pin Plastic DIP (OTP)
87C5X	D	40-Pin CERDIP (EPROM)
8XC5X	N	44-Pin PLCC (OTP)
8XC5X	S	44-Pin QFP (OTP)



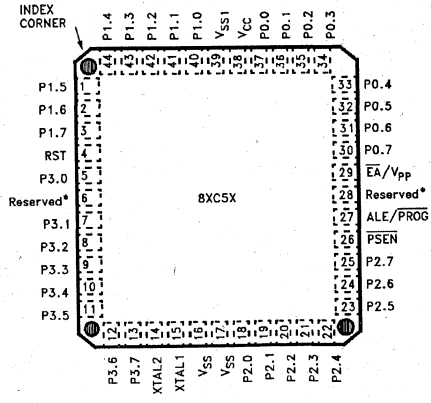
272336-2

DIP



272336-3

PLCC



272336-4

QFP

*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22). (Connection not necessary for proper operation.)

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC5X:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C5X.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC5X is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

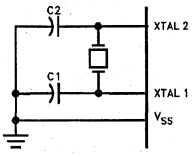
This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers", Order No. 230659.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

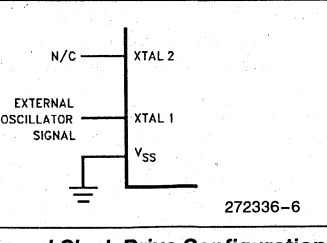


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC5X either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level, and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The window on the D87C5X must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may be functionally impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC5X without the 8XC5X having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC5X is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, (Order No. 270645) and Application Note AP-252 (Embedded Applications Handbook, Order No. 270648), "Designing with the 80C51BH."

8XC5X EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS 51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 3.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

NOTE:
Intel offers Express Temperature specifications for all 8XC5X speed options except for 33 MHz.

Table 3. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
S	QFP	Commercial	No
TP	Plastic	Extended	No
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
TS	QFP	Extended	No
LP	Plastic	Extended	Yes
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes
LS	QFP	Extended	Yes

NOTE:
Contact distributor or local sales office to match EXPRESS prefix with proper device.

EXAMPLES:
P80C52 indicates 80C52 in a plastic package and specified for commercial temperature range, without burn-in. TD80C52 indicates 80C52 in a Cerdip package and specified for extended temperature range, without burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation..... 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	4.0	6.0	V
	8XC5X-33	4.5	5.5	V
f_{OSC}	Oscillator Frequency			
	8XC5X	3.5	12	MHz
	8XC5X-1	3.5	16	MHz
	8XC5X-2	0.5	12	MHz
	8XC5X-24	3.5	24	MHz
	8XC5X-33	3.5	33	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA
		V_{CC} − 0.7			V	I_{OH} = −30 μA
		V_{CC} − 1.5			V	I_{OH} = −60 μA

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

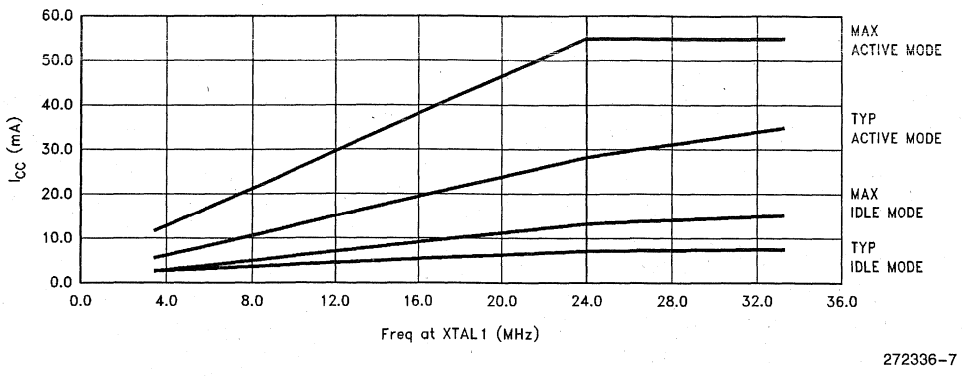
All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$V_{CC}-0.3$			V	$I_{OH} = -200\ \mu A$
		$V_{CC}-0.7$			V	$I_{OH} = -3.2$ mA
		$V_{CC}-1.5$			V	$I_{OH} = -7.0$ mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			-50	μA	$V_{IN} = 0.45V$
I_{LI}	Input leakage Current (Port 0)			± 10	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3) Commercial Express			 -650 -750	 μA μA	 $V_{IN} = 2V$
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Active Mode at 12 MHz (Figure 5) at 16 MHz at 24 MHz at 33 MHz (8XC5X-33) Idle Mode at 12 MHz (Figure 5) at 16 MHz at 24 MHz at 33 MHz (8XC5X-33) Power Down Mode 8XC5X-33		 15 20 28 35 5 6 7 7 5 5	 30 38 56 56 7.5 9.5 13.5 15 75 50	 mA mA mA mA mA mA mA mA μA μA	(Note 3)

NOTES:

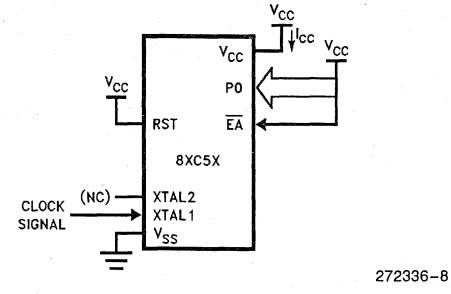
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



NOTE:
I_{CC} Max at 33 MHz is at 5V ±10% V_{CC}, while
I_{CC} Max at 24 MHz and below is at 5V ±20% V_{CC}

Figure 5. 8XC52/54/58 I_{CC} vs Frequency



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode

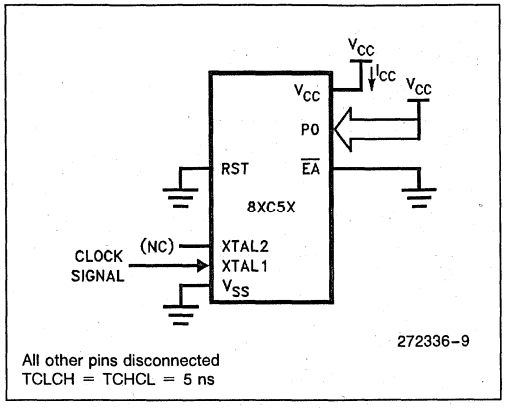


Figure 7. I_{CC} Test Condition Idle Mode

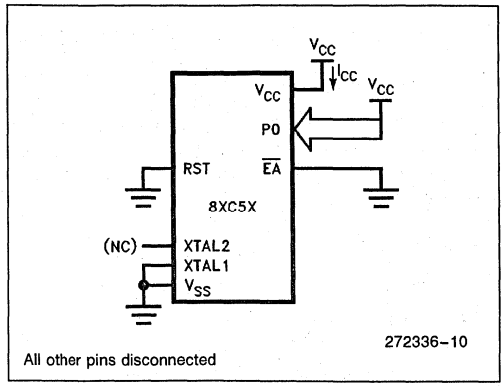


Figure 8. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 6.0V

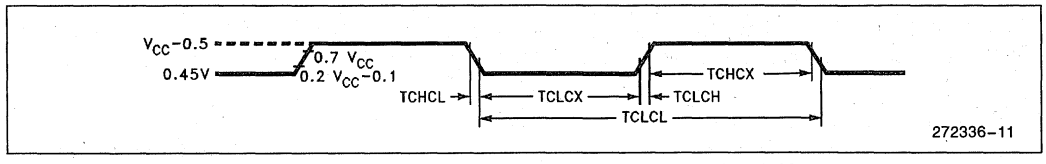


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XC5X refers to 8XC5X, 8XC5X-1, and 8XC5X-2.

Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency									
	8XC5X							3.5	12	MHz
	8XC5X-1							3.5	16	MHz
	8XC5X-2							0.5	12	MHz
	8XC5X-24							3.5	24	MHz
	8XC5X-33							3.5	33	MHz
TLHLL	ALE Pulse Width	127		43		21		2 TCLCL − 40		ns
TAVLL	Address Valid to ALE Low									
	8XC5X	43						TCLCL − 40		ns
	8XC5X-24			12				TCLCL − 30		ns
	8XC5X-33					5		TCLCL − 25		ns
TLLAX	Address Hold After ALE Low									
	8XC5X/-24	53		12				TCLCL − 30		ns
	8XC5X-33					5		TCLCL − 25		ns
TLLIV	ALE Low to Valid Instruction In									
	8XC5X		234						4 TCLCL − 100	ns
	8XC5X-24				91				4 TCLCL − 75	ns
	8XC5X-33						56		4 TCLCL − 65	ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TLLPL	ALE Low to PSEN Low									
	8XC5X/-24	53		12				TCLCL − 30		ns
	8XC5X-33					5		TCLCL − 25		ns
TPLPH	PSEN Pulse Width	205		80		46		3 TCLCL − 45		ns
TPLIV	PSEN Low to Valid Instruction In									
	8XC5X		145						3 TCLCL − 105	ns
	8XC5X-24				35				3 TCLCL − 90	ns
	8XC5X-33						35		3 TCLCL − 55	ns
TPXIX	Input Instruction Hold After PSEN	0		0		0		0		ns
TPXIZ	Input Instruction Float After PSEN									
	8XC5X		59						TCLCL − 25	ns
	8XC5X-24				21				TCLCL − 20	ns
	8XC5X-33						5		TCLCL − 25	ns
TAVIV	Address to Valid Instruction In									
	8XC5X/-24		312		103				5 TCLCL − 105	ns
	8XC5X-33						71		5 TCLCL − 80	ns
TPLAZ	PSEN Low to Address Float		10		10		10		10	ns
TRLRH	RD Pulse Width	400		150		82		6 TCLCL − 100		ns
TWLWH	WR Pulse Width	400		150		82		6 TCLCL − 100		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

All parameter values apply to all devices unless otherwise indicated.

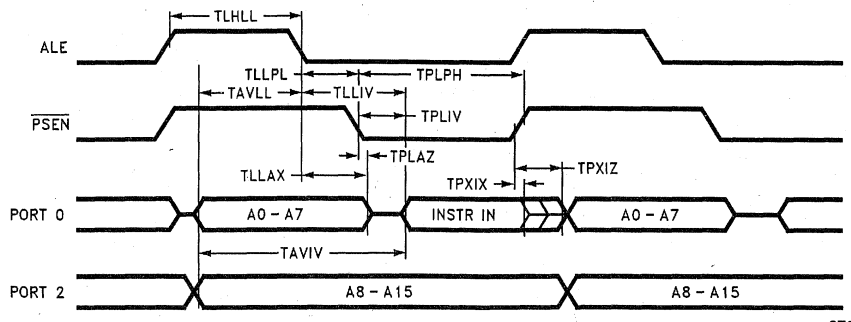
Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TRLDV	$\overline{RD}$ Low to Valid Data In									
	8XC5X		252						5 TCLCL − 165	ns
	8XC5X-24				113				5 TCLCL − 95	ns
	8XC5X-33						61		5 TCLCL − 90	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$									
	8XC5X/-24		107		23				2 TCLCL − 60	ns
	8XC5X-33						35		2 TCLCL − 25	ns
TLLDV	ALE Low to Valid Data In									
	8XC5X		517						8 TCLCL − 150	ns
	8XC5X-24/33				243		150		8 TCLCL − 90	ns
TAVDV	Address to Valid Data In									
	8XC5X		585						9 TCLCL − 165	ns
	8XC5X-24/33				285		180		9 TCLCL − 90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	75	175	41	140	3 TCLCL − 50	3 TCLCL + 50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low									
	8XC5X	203						4 TCLCL − 130		ns
	8XC5X-24			77				4 TCLCL − 90		ns
	8XC5X-33					46		4 TCLCL − 75		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

All parameter values apply to all devices unless otherwise indicated.

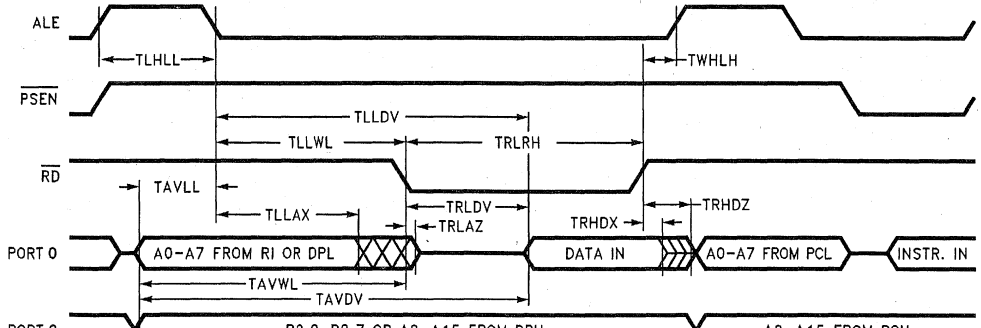
Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TQVWX	Data Valid to $\overline{WR}$ Transition									
	8XC5X	33						TCLCL − 50		ns
	8XC5X-24/33			12		0		TCLCL − 30		ns
TWHQX	Data Hold After $\overline{WR}$									
	8XC5X	33						TCLCL − 50		ns
	8XC5X-24			7				TCLCL − 35		ns
	8XC5X-33					3		TCLCL − 27		ns
TQVWH	Data Valid to $\overline{WR}$ High									
	8XC5X	433						7 TCLCL − 150		ns
	8XC5X-24/33			222		142		7 TCLCL − 70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High									
	8XC5X	43	123					TCLCL − 40	TCLCL + 40	ns
	8XC5X-24			12	71			TCLCL − 30	TCLCL + 30	ns
	8XC5X-33					5	55	TCLCL − 25	TCLCL + 25	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



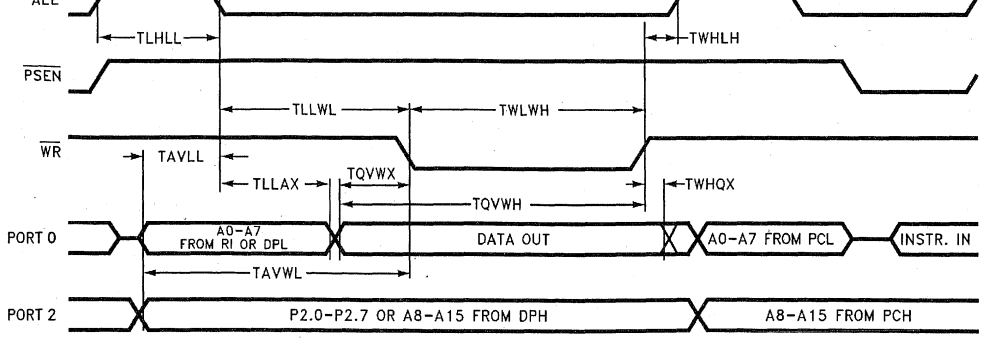
272336-25

EXTERNAL DATA MEMORY READ CYCLE



272336-26

EXTERNAL DATA MEMORY WRITE CYCLE



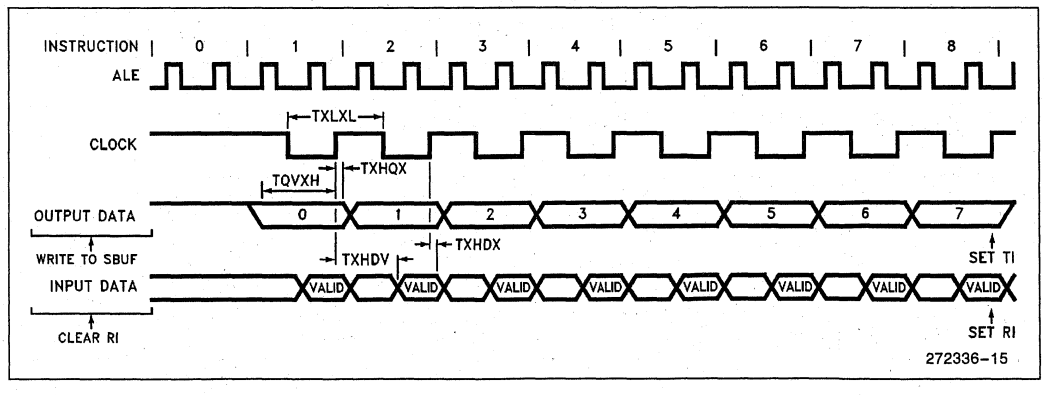
272336-27

SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.50		0.36		12 TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	700		284		167		10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge 8XC5X 8XC5X-24/33	 50		 34		 10		 2 TCLCL − 117 2 TCLCL − 50		 ns ns
TXHDX	Input Data Hold After Clock Rising Edge	0			0		0	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		283		167		10 TCLCL − 133	ns

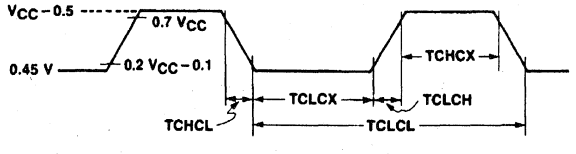
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

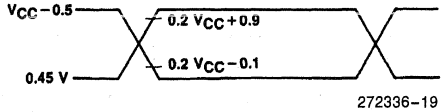
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency			MHz
	8XC5X	3.5	12	MHz
	8XC5X-1	3.5	16	MHz
	8XC5X-2	0.5	12	MHz
	8XC5X-24	3.5	24	MHz
	8XC5X-33	3.5	33	MHz
TCHCX	High Time	20		ns
	8XC5X-24/33	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCX	Low Time	20		ns
	8XC5X-24/33	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCH	Rise Time		20	ns
	8XC5X-24		10	ns
	8XC5X-33		5	ns
TCHCL	Fall Time		20	ns
	8XC5X-24		10	ns
	8XC5X-33		5	ns

EXTERNAL CLOCK DRIVE WAVEFORM



272336-16

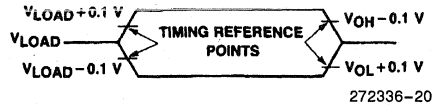
AC TESTING INPUT, OUTPUT WAVEFORMS



272336-19

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272336-20

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 4. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTES:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5 respectively for A0–A13.

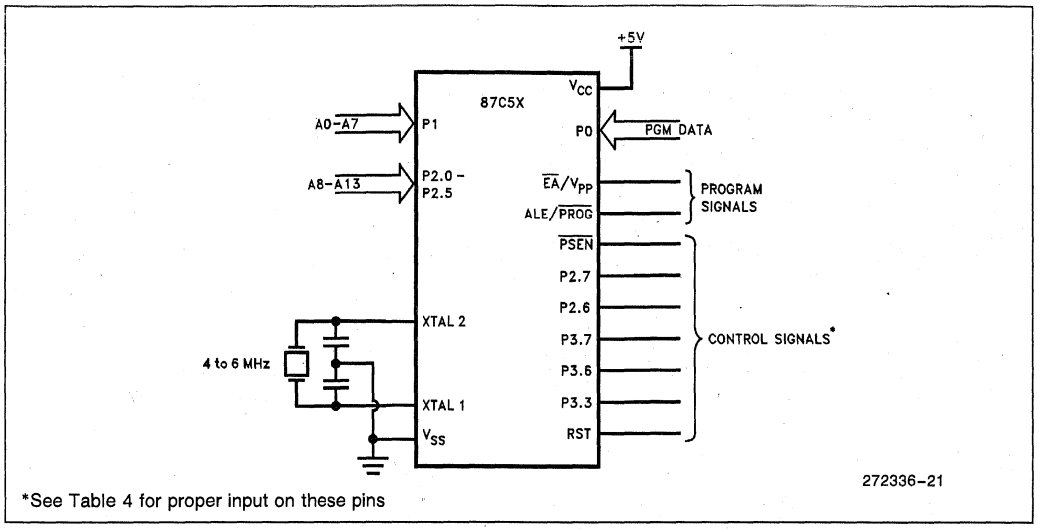
DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 4. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 4 for proper input on these pins

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 4 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C5X the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C5X.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

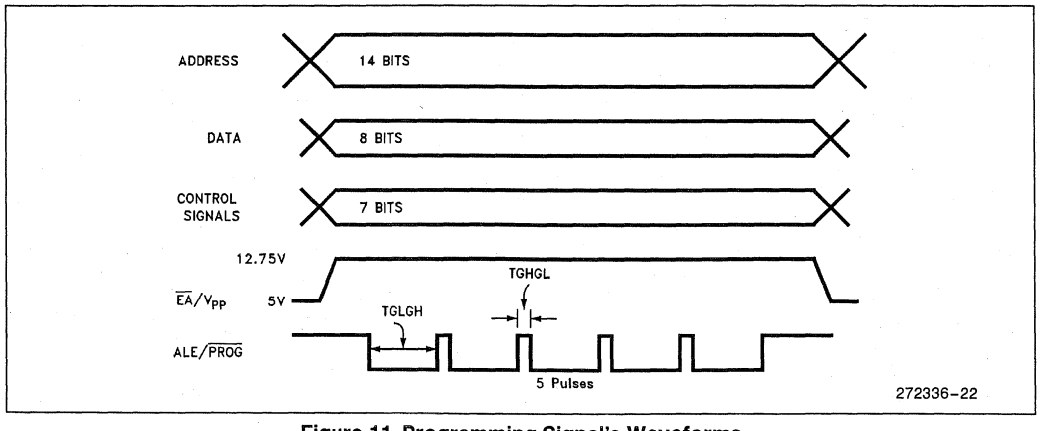


Figure 11. Programming Signal's Waveforms

ROM and EPROM Lock System

The program lock system, when programmed, protects the onboard program against software piracy.

The 80C5X has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 5. If program protection is desired. the user submits the encryption table with their code. and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C5X has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 5.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 4 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C5X has 3 programmable lock bits that when programmed according to Table 5 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 8XC5X has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 4 for Read Signature Byte.

Location	Device	Contents
30H	All	89H
31H	All	58H
60H	80C52	12H
	87C52	52H
	80C54	14H
	87C54	54H
	80C58	18H
	87C58	58H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

Table 5. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

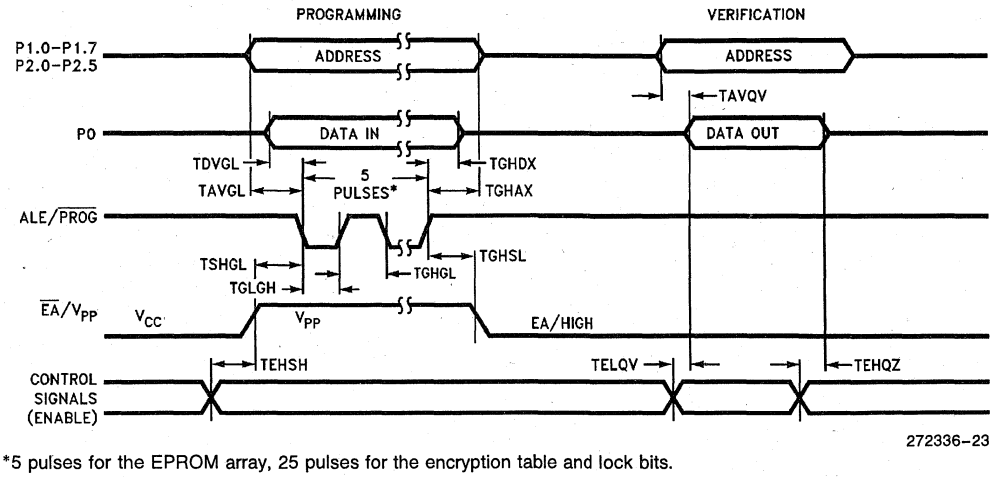
NOTE:
Any other combination of the lock bits is not defined.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel Packaging Handbook (Order Number 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
P	45°C/W	16°C/W	All
D	45°C/W	15°C/W	All
N	46°C/W	16°C/W	All
S	87°C/W	18°C/W	52
	96°C/W	24°C/W	54
	90°C/W	22°C/W	58

DATA SHEET REVISION HISTORY

Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this datasheet (272336-003) and the previous version (272336-002):

1. Removed 8XC5X-3 and 8XC5X-20 from the data sheet.
2. Included 8XC5X-24 and 8XC5X-33 devices.
3. Removed the statement "The 80C32 standard, -1 and -2, and 80C52 standard, -1 and -2, do not have the . . . " from the section DESIGN CONSIDERATION.

The following differences exist between this datasheet (272336-002) and the previous version (272336-001):

1. Removed 8XC5X-L from the data sheet.
2. Included features not available in 80C32-Standard, -1 and -2, and 80C52-Standard, -1 and -2 devices.

This 8XC5X datasheet (272336-001) replaces the following datasheets:

87C52/80C52/80C32	270757-003
87C52/80C52/80C32 EXPRESS	270868-002
87C52-20/80C52-20/80C32-20	272272-001
87C54/80C54	270816-004
87C54/80C54 EXPRESS	270901-001
87C54-20/-3 80C54-20/-3	270941-003
87C54/80C58	270900-003
87C58/80C58 EXPRESS	270902-001
87C58-20/-3 80C58-20/-3	272029-002

8XC51FX
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLERS

Commercial/Express

87C51FA/83C51FA/80C51FA/87C51FB/83C51FB/87C51FC/83C51FC
***See Table 1 for Proliferation Options**

- **High Performance CHMOS EPROM/ROM/CPU**
- **12/24/33 MHz Operation**
- **Three 16-Bit Timer/Counters**
- **Programmable Counter Array with:**
  - **— High Speed Output,**
  - **— Compare/Capture,**
  - **— Pulse Width Modulator,**
  - **— Watchdog Timer Capabilities**
- **Up/Down Timer/Counter**
- **Three Level Program Lock System**
- **8K/16K/32K On-Chip Program Memory**
- **256 Bytes of On-Chip Data RAM**
- **Improved Quick Pulse Programming Algorithm**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **7 Interrupt Sources**
- **Four Level Interrupt Priority**
- **Programmable Serial Channel with:**
  - **— Framing Error Detection**
  - **— Automatic Address Recognition**
- **TTL Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS® 51 Controller Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE (On-Circuit Emulation) Mode**
- **Extended Temperature Range Except for 33 MHz Offering (−40°C to +85°C)**

MEMORY ORGANIZATION

ROM Device	EPROM Version	ROMLESS Version	ROM/ EPROM Bytes	RAM Bytes
83C51FA	87C51FA	80C51FA	8K	256
83C51FB	87C51FB	80C51FA	16K	256
83C51FC	87C51FC	80C51FA	32K	256

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 87C51FA/8XC51FB/8XC51FC is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. The Intel 83C51FA/80C51FA is fabricated on CHMOS III technology. Being a member of the MCS® 51 controller family, the 8XC51FA/8XC51FB/8XC51FC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 controller products. The 8XC51FA/8XC51FB/8XC51FC is an enhanced version of the 8XC52/8XC54/8XC58. Its added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O and up/down counting capabilities such as motor control.

For the remainder of this document, the 8XC51FA, 8XC51FB, 8XC51FC will be referred to as the 8XC51FX, unless information applies to a specific device.

Table 1. Proliferation Options

	Standard*1	-1	-2	-24	-33
80C51FA	X	X	X	X	X
83C51FA	X	X	X	X	X
87C51FA	X	X	X	X	X
83C51FB	X	X	X	X	X
87C51FB	X	X	X	X	X
83C51FC	X	X	X	X	X
87C51FC	X	X	X	X	X

NOTES:
*1 3.5 MHz to 12 MHz; 5V ±20%
-1 3.5 MHz to 16 MHz; 5V ±20%
-2 0.5 MHz to 12 MHz; 5V ±20%
-24 3.5 MHz to 24 MHz; 5V ±20%
-33 3.5 MHz to 33 MHz; 5V ±10%

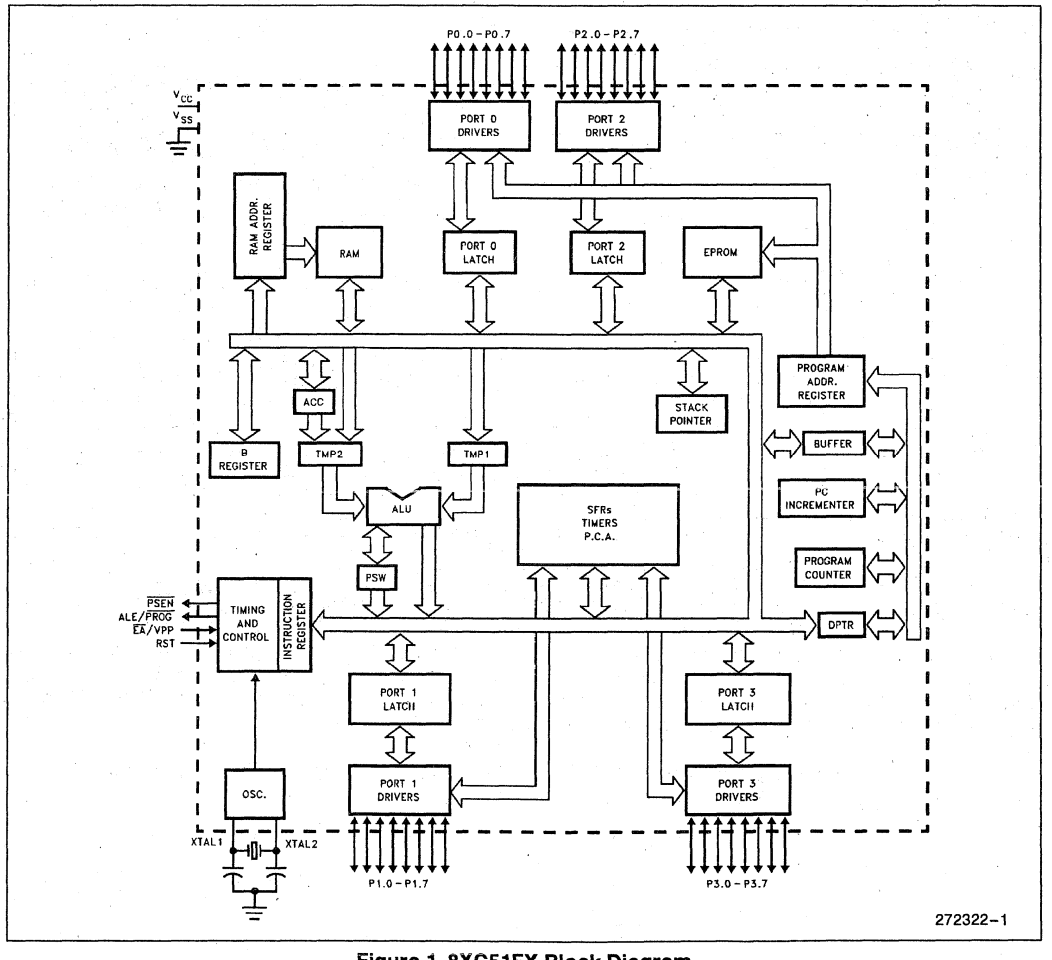


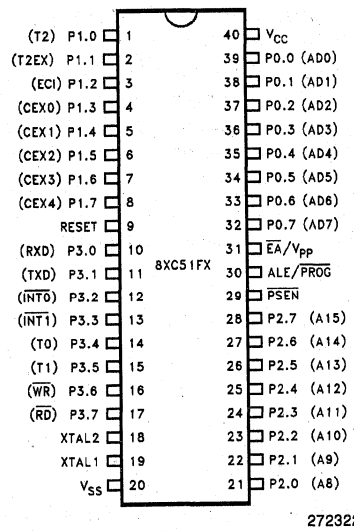
Figure 1. 8XC51FX Block Diagram

PROCESS INFORMATION

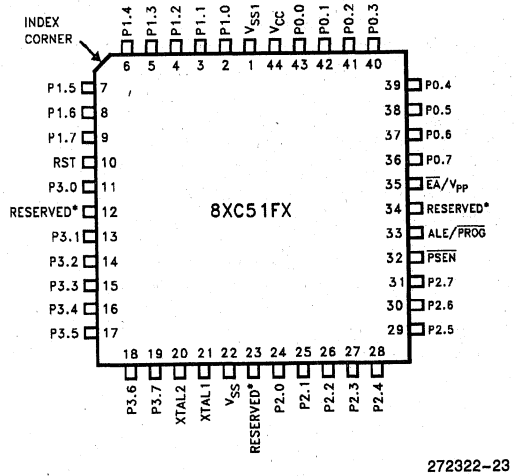
The 87C51FA/8XC51FB/8XC51FC is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order No. 210997.

PACKAGES

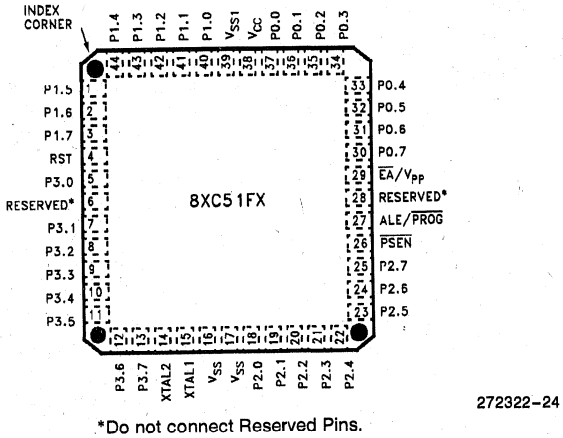
Part	Prefix	Package Type
8XC51FX	P	40-Pin Plastic DIP
	D	40-Pin CERDIP
	N	44-Pin PLCC
	S	44-Pin QFP



DIP



PLCC



*Do not connect Reserved Pins.

QFP

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP devices or any 83C51FA/80C51FA device). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitution for the V_{SS} pin. (Connection not necessary for proper operation.)

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51FX:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FX.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51FX is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

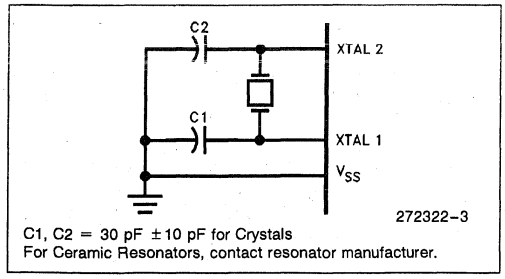
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

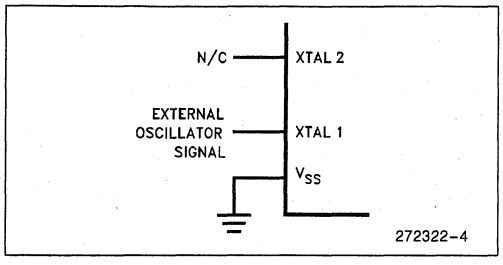


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51FX either hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- Ambient light is known to affect the internal RAM contents during operation. If the 87C51FX application requires the part to be run under ambient lighting, an opaque label should be placed over the window to exclude light.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51FX without the 8XC51FX having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51FX is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

8XC51FX EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ± 0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 3.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

NOTE:
Intel offers Express Temperature specifications for all 8XC51FX speed options except for 33 MHz.

Table 3. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
D	Cerdip	Commercial	No
N	PLCC	Commercial	No
P	Plastic	Commercial	No
S	QFP	Commercial	No
LD	Cerdip	Extended	Yes
LN	PLCC	Extended	Yes
LP	Plastic	Extended	Yes
LS	QFP	Extended	Yes
TD	Cerdip	Extended	No
TN	PLCC	Extended	No
TP	Plastic	Extended	No
TS	QFP	Extended	No

NOTE:
Contact distributor or local sales office to match EXPRESS prefix with proper device.

EXAMPLES:
P87C51FC indicates 87C51FC in a plastic package and specified for commercial temperature range, without burn-in.
LD87C51FC indicates 87C51FC in a cerdip package and specified for extended temperature range with burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias Commercial Express	 0 −40	 +70 +85	°C
V_{CC}	Supply Voltage 8XC51FX-33 All Others	 4.5 4.0	 5.5 6.0	V
f_{OSC}	Oscillator Frequency 8XC51FX 8XC51FX-1 8XC51FX-2 8XC51FX-24 8XC51FX-33	 3.5 3.5 0.5 3.5 3.5	 12 16 12 24 33	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Note 5) (Ports 1, 2 and 3)			0.3 0.45 1.0	V	I_{OL} = 100 μA I_{OL} = 1.6 mA (Note 1) I_{OL} = 3.5 mA
V_{OL1}	Output Low Voltage (Note 5) (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)			0.3 0.45 1.0	V	I_{OL} = 200 μA I_{OL} = 3.2 mA (Note 1) I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Ports 1, 2 and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V	I_{OH} = −10 μA I_{OH} = −30 μA (Note 2) I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) 83C51FA/80C51FA (Express)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V	I_{OH} = −200 μA I_{OH} = −3.2 mA (Note 2) I_{OH} = −7.0 mA I_{OH} = −6.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	V_{IN} = 0.45V

DC CHARACTERISTICS (Over Operating Conditions)

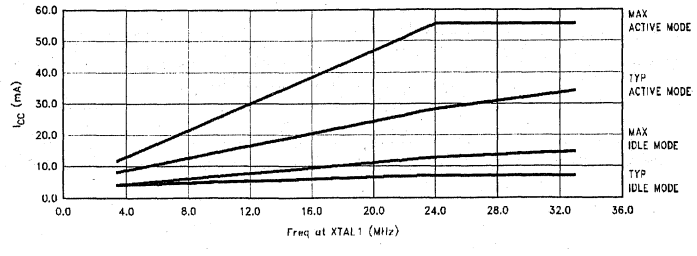
All parameter values apply to all devices unless otherwise indicated. (Continued)

Symbol	Parameter	Min	Typical (Note 4)	Max	Units	Test Conditions
I_{LI}	Input leakage Current (Port 0)			±10	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3) Express Commercial			 −750 −650	 μA	V_{IN} = 2V
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1MHz, 25°C
I_{CC}	Power Supply Current: Active Mode At 12 MHz (Figure 5) At 16 MHz At 24 MHz At 33 MHz Idle Mode At 12 MHz (Figure 5) At 16 MHz At 24 MHz At 33 MHz Power Down Mode		 15 20 28 35 5 6 7 7 5	 30 38 56 56 7.5 9.5 13.5 15 75	 mA mA mA mA mA mA mA mA μA	(Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitance loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for power down is 2V.
4. Typicals are based on limited number of samples, and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



Note:
I_{CC} max at 33 MHz is at 5V ±10% V_{CC}, while I_{CC} max at 24 MHz and below is at 5V ±20% V_{CC}.

Figure 5. 8XC51FA/FB/FC I_{CC} vs Frequency

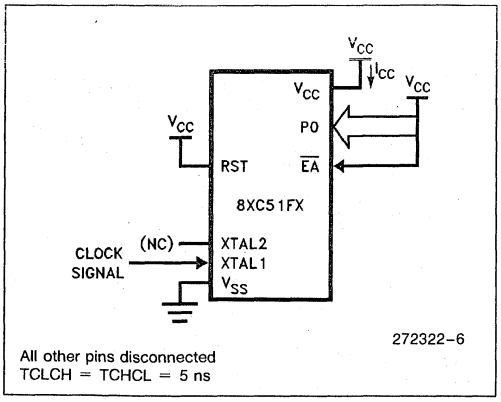


Figure 6. I_{CC} Test Condition, Active Mode

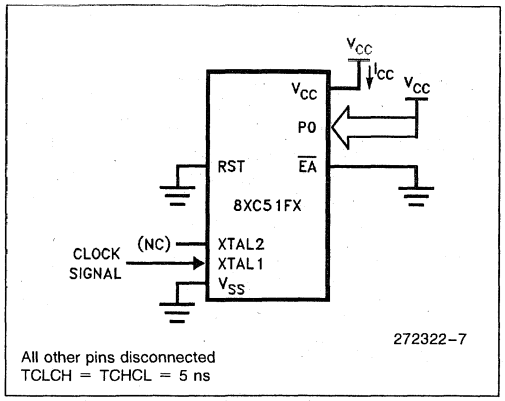


Figure 7. I_{CC} Test Condition Idle Mode

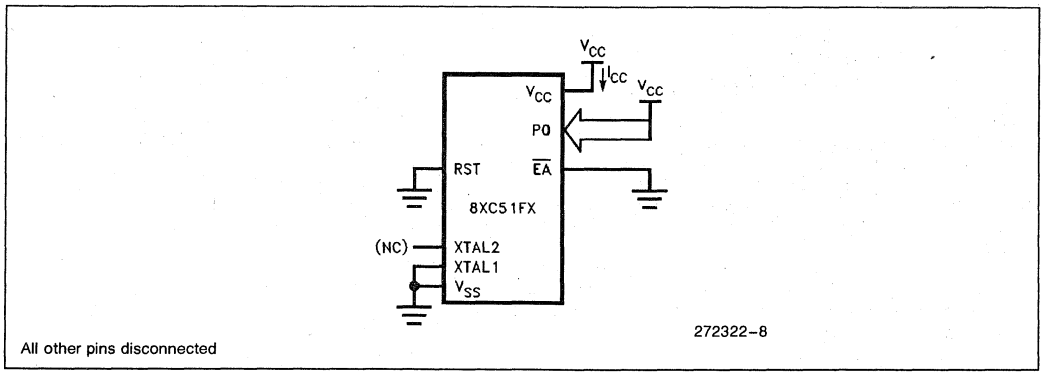


Figure 8. I_{CC} Test Condition, Power Down Mode.
V_{CC} = 2.0V to 6.0V.

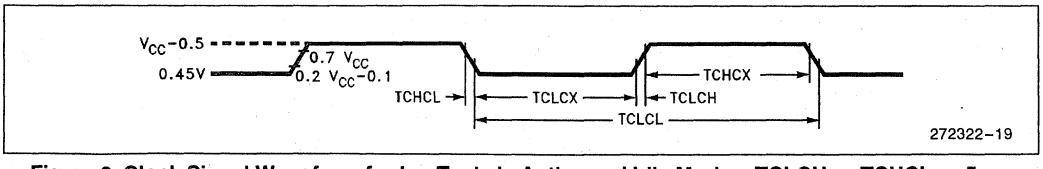


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to PSEN Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XC51FX refers to 8XC51FX, 8XC51FX-1 and 8XC51FX-2.

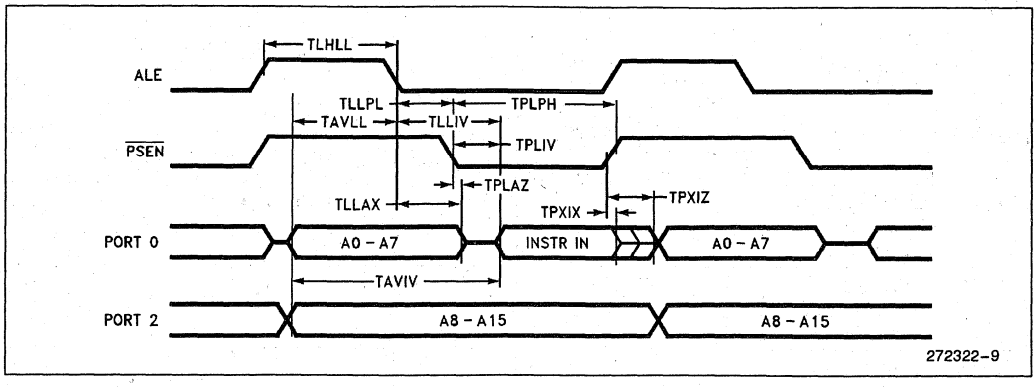
Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 8XC51FX 8XC51FX-1 8XC51FX-2 8XC51FX-24 8XC51FX-33							 3.5 3.5 0.5 3.5 3.5	 12 16 12 24 33	MHz
TLHLL	ALE Pulse Width	127		43		21		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low 8XC51FX 8XC51FX-24 8XC51FX-33	43		12		5		 TCLCL−40 TCLCL−30 TCLCL−25		 ns ns ns
TLLAX	Address Hold After ALE Low 8XC51FX/-24 8XC51FX-33	53		12		5		 TCLCL−30 TCLCL−25		 ns ns
TLLIV	ALE Low to Valid Instr In 8XC51FX 8XC51FX-24 8XC51FX-33		234		91		56		 4TCLCL−100 4TCLCL−75 4TCLCL−65	 ns ns ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low 8XC51FX/-24 8XC51FX-33	53		12		5		 TCLCL−30 TCLCL−25		 ns ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		80		46		3TCLCL−45		
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instr In 8XC51FX 8XC51FX-24 8XC51FX-33		145		35		35		 3TCLCL−105 3TCLCL−90 3TCLCL−55	 ns ns ns
TPXIX	Input Instr Hold after $\overline{\text{PSEN}}$	0		0		0		0		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

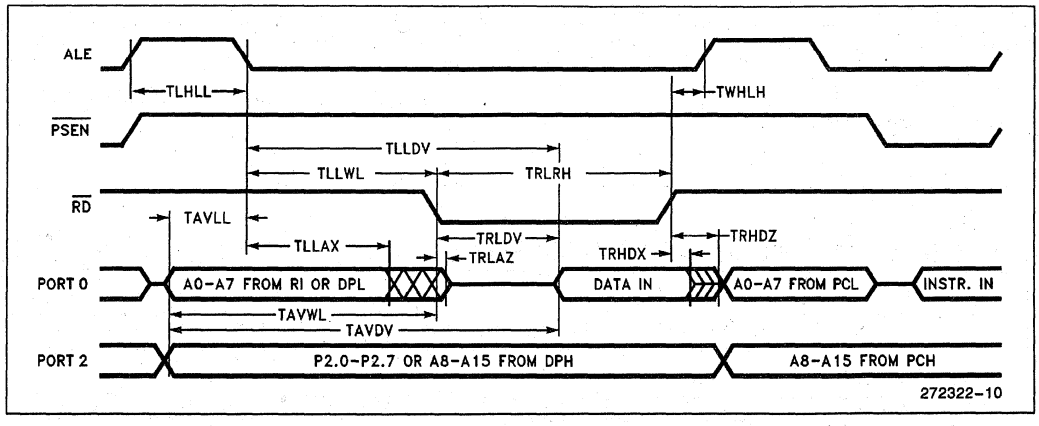
All parameter values apply to all devices unless otherwise indicated

Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TPXIZ	Input Instr Float After $\overline{PSEN}$									
	8XC51FX		59						TCLCL-25	ns
	8XC51FX-24				21				TCLCL-20	ns
	8XC51FX-33						5		TCLCL-25	ns
TAVIV	Address to Valid Instr In									
	8XC51FX/-24		312		103				5TCLCL-105	ns
	8XC51FX-33						71		5TCLCL-80	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		150		82		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		150		82		6TCLCL-100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In									
	8XC51FX		252						5TCLCL-165	ns
	8XC51FX-24				113				5TCLCL-95	ns
	8XC51FX-33						61		5TCLCL-90	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$									
	8XC51FX/24		107		23				2TCLCL-60	ns
	8XC51FX-33						35		2TCLCL-25	ns
TLLDV	ALE Low to Valid Data In									
	8XC51FX		517						8TCLCL-150	ns
	8XC51FX-24/33				243		150		8TCLCL-90	ns
TAVDV	Address to Valid Data In									
	8XC51FX		585						9TCLCL-165	ns
	8XC51FX-24/33				285		180		9TCLCL-90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	75	175	41	140	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low									
	8XC51FX	203						4TCLCL-130		ns
	8XC51FX-24			77				4TCLCL-90		ns
	8XC51FX-33					46		4TCLCL-75		ns
TQVWX	Data Valid to $\overline{WR}$ Transition									
	8XC51FX	33						TCLCL-50		ns
	8XC51FX-24/33			12		0		TCLCL-30		ns
TWHQX	Data Hold After $\overline{WR}$									
	8XC51FX	33						TCLCL-50		ns
	8XC51FX-24			7				TCLCL-35		ns
	8XC51FX-33					3		TCLCL-27		ns
TQVWH	Data Valid to $\overline{WR}$ High									
	8XC51FX	433						7TCLCL-150		ns
	8XC51FX-24/33			222		142		7TCLCL-70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High									
	8XC51FX	43	123					TCLCL-40	TCLCL+40	ns
	8XC51FX-24			12	71			TCLCL-30	TCLCL+30	ns
	8XC51FX-33					5	55	TCLCL-25	TCLCL+25	ns

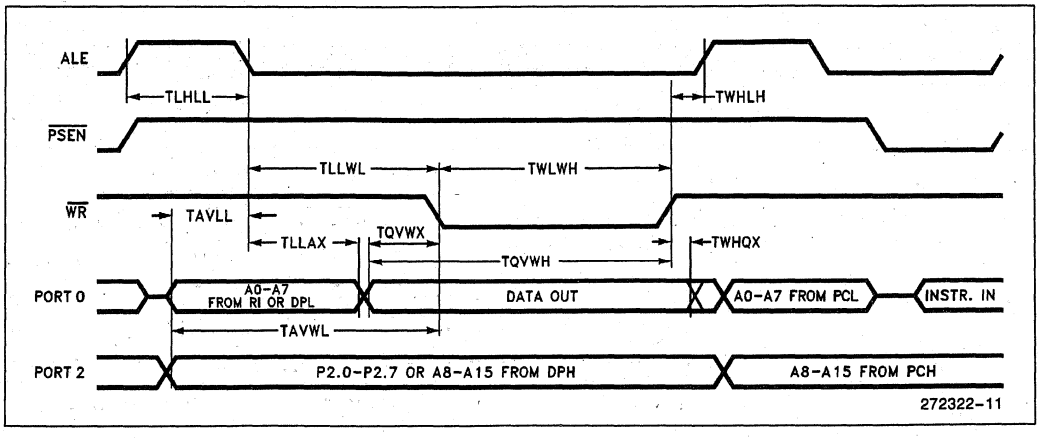
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

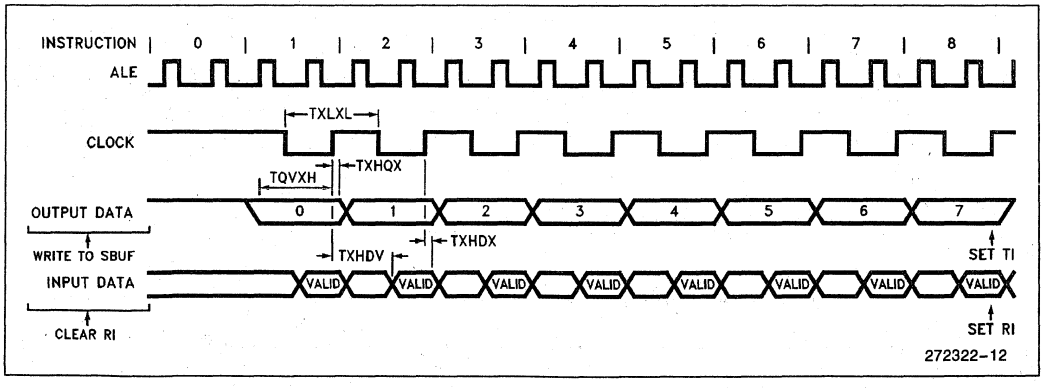


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	Oscillator								Units
		12 MHz		24 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.50		0.36		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		284		167		10TCLCL−133		ns
TXHQX	Output Data Hold After Clock Rising Edge 8XC51FX 8XC51FX-24/33	50		34		10		2TCLCL−117 2TCLCL−50		ns ns
TXHDX	Input Data Hold After Clock Rising Edge	0			0		0	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		283		167		10TCLCL−133	ns

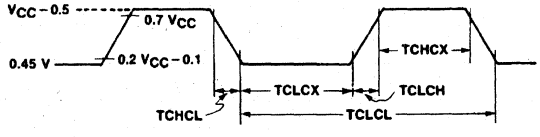
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

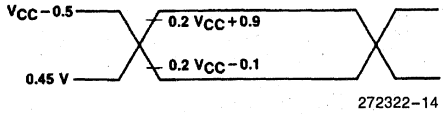
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency			MHz
	8XC51FX	3.5	12	MHz
	8XC51FX-1	3.5	16	MHz
	8XC51FX-2	0.5	12	MHz
	8XC51FX-24	3.5	24	MHz
	8XC51FX-33	3.5	33	MHz
TCHCX	High Time	20		ns
	8XC51FX-24/33	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCX	Low Time	20		ns
	8XC51FX-24/33	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCH	Rise Time		20	ns
	8XC51FX-24		10	ns
	8XC51FX-33		5	ns
TCHCL	Fall Time		20	ns
	8XC51FX-24		10	ns
	8XC51FX-33		5	ns

EXTERNAL CLOCK DRIVE WAVEFORM



272322-13

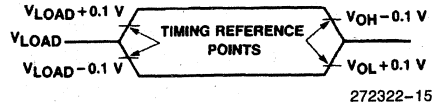
AC TESTING INPUT, OUTPUT WAVEFORMS



272322-14

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS



272322-15

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA.

PROGRAMMING THE EPROM/OTP

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal EPROM locations.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, RST $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 4. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed EPROM location. The setup is shown in Figure 10.

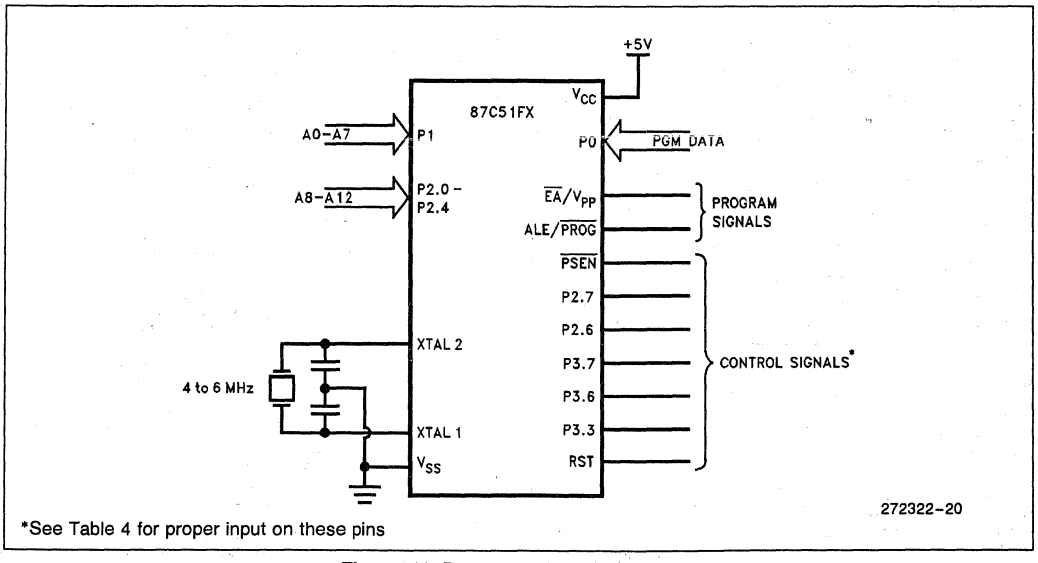
Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

NOTE:

- $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.

Table 4. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 4 for proper input on these pins

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 4 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51FX the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse, ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C51FX.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

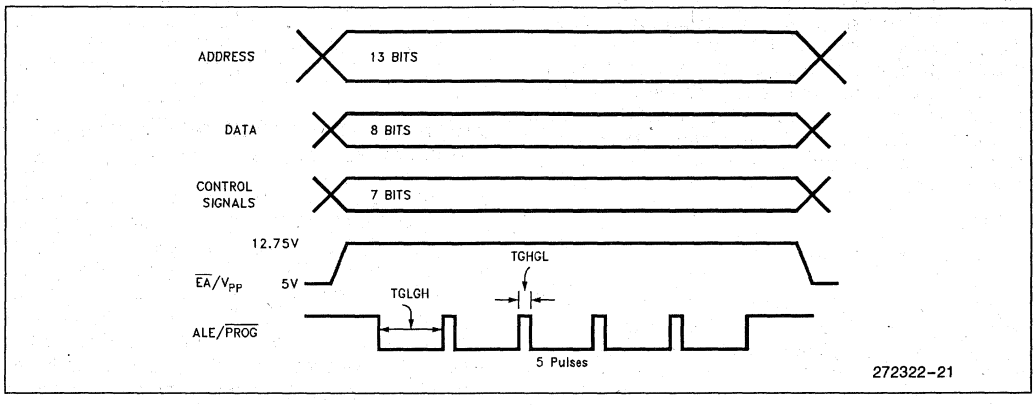


Figure 11. Programming Signals Waveforms

ROM and EPROM Lock System

The 87C51FX program lock system, when programmed, protects the onboard program against software piracy.

The 83C51FX has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 5. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table. The 83C51FA does not have protection features.

The 87C51FX has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 5.

Table 5. Program Lock Bits and the Features

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 4 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C51FX has 3 programmable lock bits that when programmed according to Table 5 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 87C51FX has 3 signature bytes in locations 30H, 31H, and 60H. The 83C51FA has 2 signature bytes in locations 30H and 31H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 4 for Read Signature Byte.

Location	Device	Contents
30H	All	89H
31H	All	58H
60H	83C51FA	7AH/FAH
	87C51FA	FAH
	83C51FB	7BH/FBH
	87C51FB	FBH
	83C51FC	7CH/FCH
	87C51FC	FCH

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

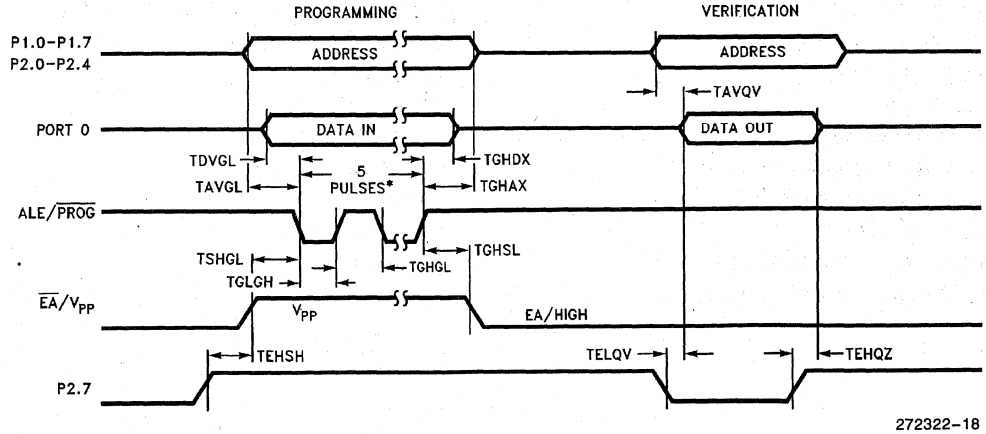
Erasure leaves all the EPROM Cells in a 1's state.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 (ENABLE) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



NOTE:
*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel Packaging Handbook (Order No. 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
P	45°C/W	16°C/W	All
D	36°C/W	13°C/W	80C51FA, 83C51FA, 8XC51FC
	45°C/W	15°C/W	87C51FA, 8XC51FB
N	46°C/W	16°C/W	All
S	97°C/W	24°C/W	FA
	96°C/W	24°C/W	FB
	87°C/W	18°C/W	FC

DATA SHEET REVISION HISTORY

Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this datasheet (272322-003) and the previous version (272322-002):

1. Removed 8XC51FX-3 and 8XC51FX-20, replaced with 8XC51FX-24.
2. Included 8XC51FX-24 and 8XC51FX-33 devices.
3. 80C51FA and 83C51FA now have the same features as 87C51FA, 8XC51FB and 8XC51FC; same DC spec used for all devices.

The following differences exist between the "-002" and "-001" version of 8XC51FX datasheet:

1. Removed 8XC51FX-L from datasheet.
2. Include V_{OH1} for 83C51FA (Express)/80C51FA (Express).

This 8XC51FX datasheet (272322-001) replaces the following datasheets:

87C51FA/83C51FA/80C51FA	270258-007
83C51FA/80C51FA EXPRESS	270620-001
87C51FA EXPRESS	270619-001
87C51FA-20/-3	272081-002
87C51FB/83C51FB	270563-005
87C51FB-20/-3 83C51FB-20/-3	272080-002
87C51FB/83C51FB EXPRESS	270767-002
87C51FC/83C51FC	270789-004
87C51FC/83C51FC EXPRESS	270903-001
87C51FC-20/-3 83C51FC-20/-3	272028-002

8XL52/54/58
LOW VOLTAGE
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLERS

Commercial/Express

87L52/80L52/87L54/80L54/87L58/80L58

- **High Performance CHMOS OTP ROM**
- **Low Voltage Operation**
- **20 MHz Commercial/16 MHz Express Operation**
- **Three 16-Bit Timer/Counters**
- **Up/Down Timer/Counter**
- **Three Level Program Lock System**
- **8K/16K/32K On-Chip Program Memory**
- **256 Bytes of On-Chip Data RAM**
- **Improved Quick Pulse Programming Algorithm**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **6 Interrupt Sources**
- **Four Level Interrupt Priority**
- **Programmable Serial Channel with:**
  — Framing Error Detection
  — Automatic Address Recognition
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS® 51 Microcontroller Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE (On-Circuit Emulation) Mode**
- **Extended Temperature Range (−40°C to +85°C)**

MEMORY ORGANIZATION

OTP ROM Version	ROM Version	ROM/ OTP ROM Bytes	RAM Bytes
87L52	80L52	8K	256
87L54	80L54	16K	256
87L58	80L58	32K	256

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 8XL52/8XL54/8XL58 is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS 51 microcontroller family, the 8XL52/8XL54/8XL58 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 microcontroller products.

The 8XL5X is a 3V version of current 8XC5X and will operate from 2.7V to 3.6V at a frequency range of 3.5 MHz to 16 MHz (Express)/20 MHz (Commercial).

For the remainder of this document, the 8XL52, 8XL54, 8XL58 will be referred to as the 8XL5X, unless information applies to a specific device.

December 1996

Order Number: 272468-003

	Standard	-1	-20*
80L52	X	X	X
87L52	X	X	X
80L54	X	X	X
87L54	X	X	X
80L58	X	X	X
87L58	X	X	X

NOTE:
Standard 3.5 MHz to 12 MHz; 2.7V to 3.6V
-1 3.5 MHz to 16 MHz; 2.7V to 3.6V
-20* 3.5 MHz to 20 MHz; 2.7V to 3.6V
*Only available for commercial standard temperature range, not available at express temperature range.

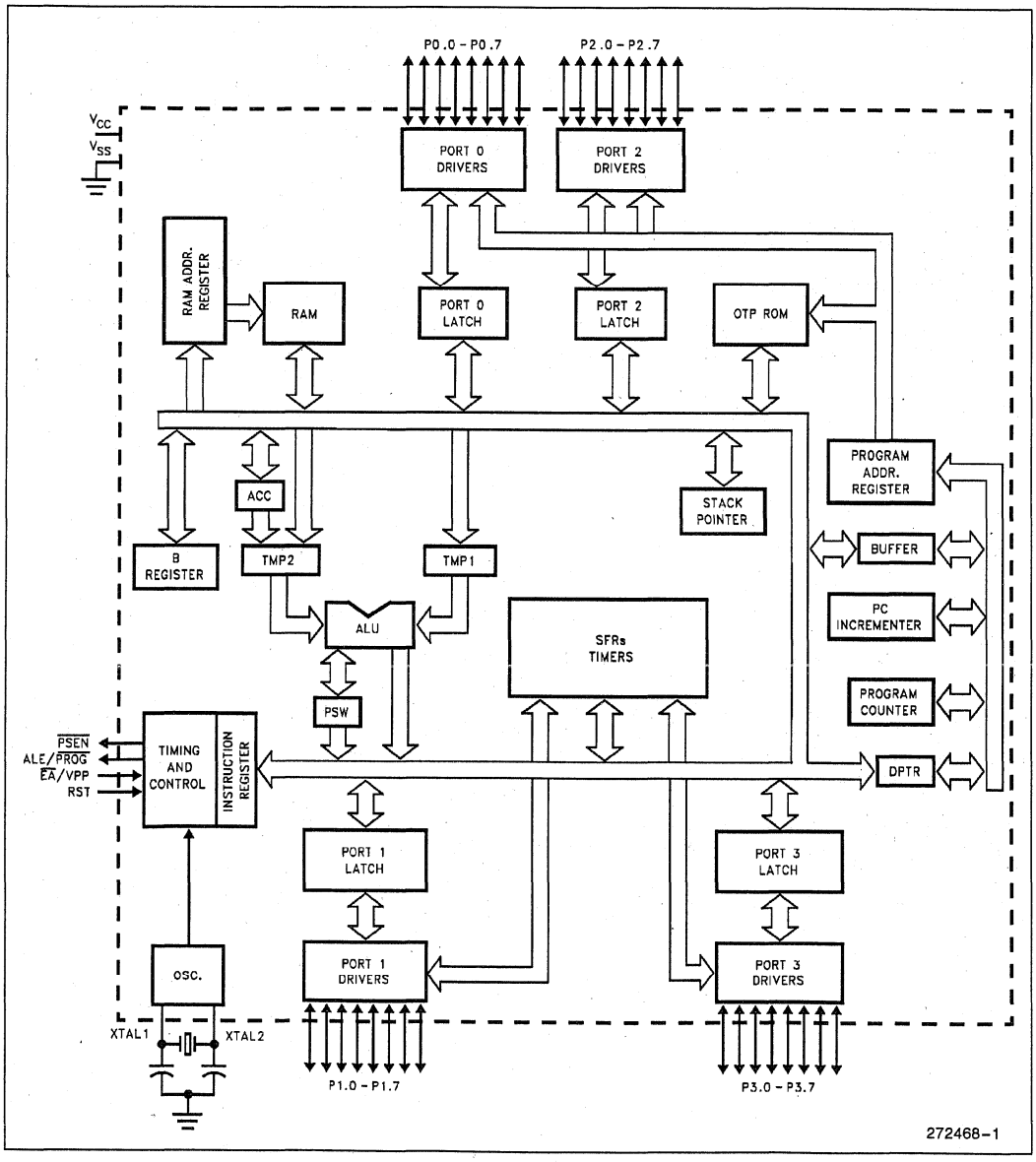


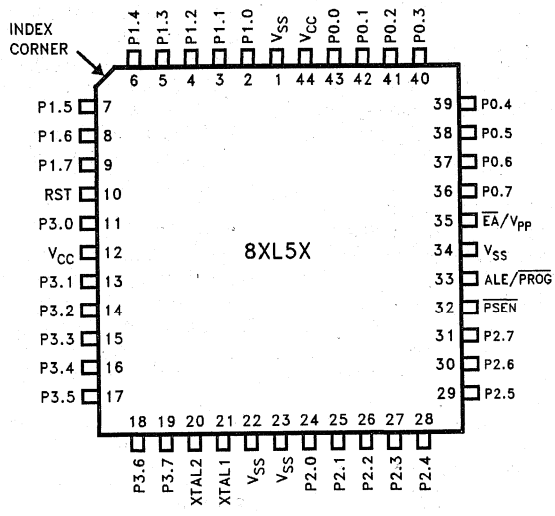
Figure 1. 8XL5X Block Diagram

PROCESS INFORMATION

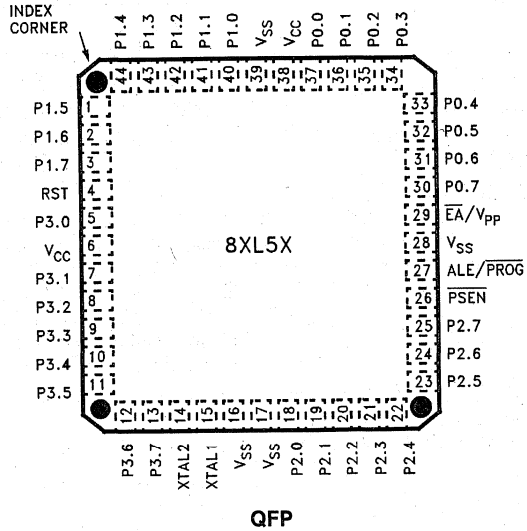
The 8XL52/8XL54/8XL58 is manufactured on the CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

Part	Prefix	Package Type
8XL5X	N	44-Pin PLCC (OTP)
	S	44-Pin QFP (OTP)



PLCC



QFP

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several inputs.

Port 0 also receives the code bytes during OTP ROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive several inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XL5X:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock Out
P1.1	T2EX (Timer/ Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during OTP ROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive several inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during OTP ROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive several inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH2} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during OTP ROM programming for the 87L5X.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XL5X is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ must be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during OTP ROM programming.

XTAL1: Input to the inverting oscillator amplifier.

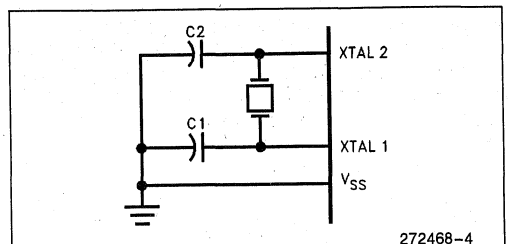
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

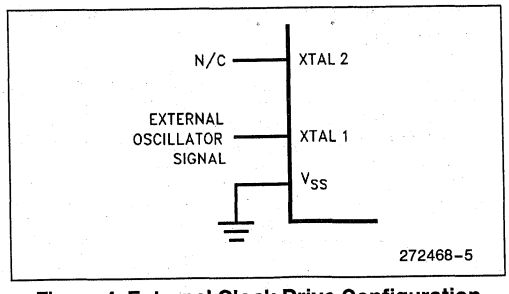


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XL5X either hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The 8XL5X will operate from 2.7V to 3.6V with a frequency range of 3.5 MHz to 16 MHz (Express)/20 MHz (Commercial). Operating beyond these specifications could cause improper device functionality.
- All V_{CC} and V_{SS} pins must be connected. Please refer to Figure 2, Pin Connections, for the specific pins.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XL5X without the 8XL5X having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XL5X is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, #270646, and Application Note AP-252 (Embedded Applications Handbook), #270648, "Designing with the 80C51BH."

8XL5X EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 2.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

Table 2. Prefix Identification

Prefix	Package Type	Temperature Range
N	PLCC	Commercial
S	QFP	Commercial
TN	PLCC	Extended
TS	QFP	Extended

NOTE:
Contact your distributor or local sales office to match the EXPRESS prefix with the proper device.

EXAMPLES:
N87L51FC indicates 87L51FC in a PLCC package and specified for commercial temperature range, without burn-in.

TN87L51FC indicates 87L51FC in a PLCC package and specified for extended temperature range with burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} per I/O Pin ..... 15 mA
Power Dissipation..... 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	2.7	3.6	V

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except XTAL1, RST)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, RST)	−0.5	0.2 V_{CC} − 0.1	V	
V_{IH}	Input High Voltage (Except XTAL1, RST, $\overline{EA}$)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{EA}$)	V_{CC} − 1.0	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Note 4) (Ports 1, 2 and 3)		0.4	V	I_{OL} = 1.6 mA (Note 1)
V_{OL1}	Output Low Voltage (Note 4) (Port 0, ALE/$\overline{PSEN}$)		0.4	V	I_{OL} = 3.2 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$	V_{CC} − 0.7		V	I_{OH} = −30 μA (Note 2)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	I_{OH} = −1.0 mA (Note 2)
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)		−50	μA	V_{IN} = 0.4V
I_{LI}	Input Leakage Current (Port 0)		±10	μA	0 < V_{IN} < V_{CC}

DC CHARACTERISTICS (Over Operating Conditions)

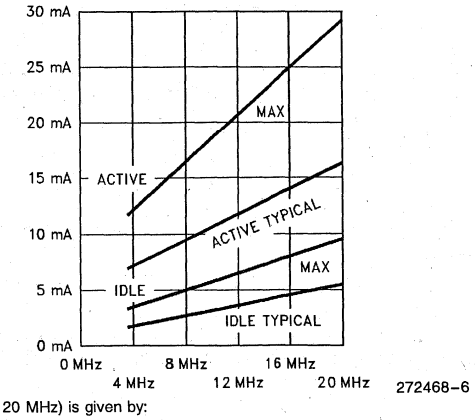
All parameter values apply to all devices unless otherwise indicated. (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		−350	μA	V_{IN} = 1.4V
RRST	RST Pulldown Resistor	40	225	KΩ	
I_{CC}	Power Supply Current Active Mode at 16 MHz Idle Mode at 16 MHz Power-Down Mode		 25 8 30	 mA mA μA	(Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitance loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for power down is 2V.
4. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
Running the device with $\overline{EA}$ at a higher voltage than V_{CC} sinks additional currrent.



I_{CC} Max at other frequencies (3.5 MHz to 20 MHz) is given by:
Active Mode
I_{CC} MAX = 1.1 × FREQ + 7.6
Idle Mode
I_{CC} MAX = 0.4 × FREQ + 1.8
Where FREQ is in MHz, I_{CC}MAX is given in mA.

Figure 5. I_{CC} vs Frequency

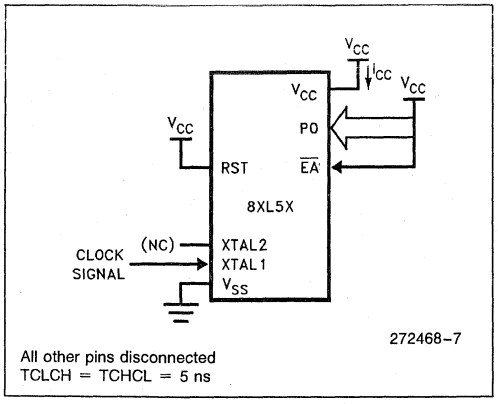


Figure 6. I_{CC} Test Condition, Active Mode

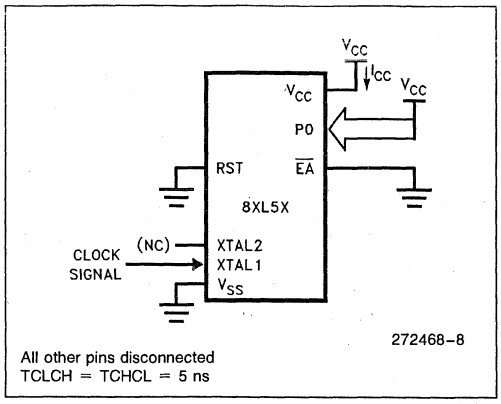


Figure 7. I_{CC} Test Condition Idle Mode

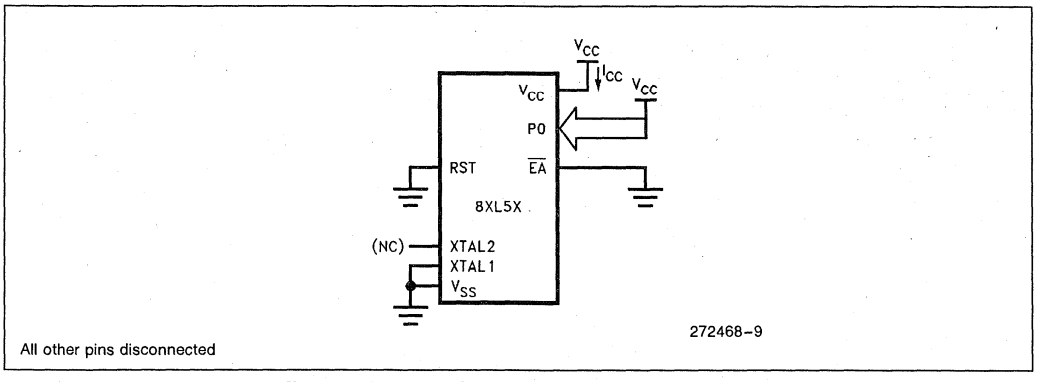


Figure 8. I_{CC} Test Condition, Power Down Mode.
V_{CC} = 2.7V to 3.6V.

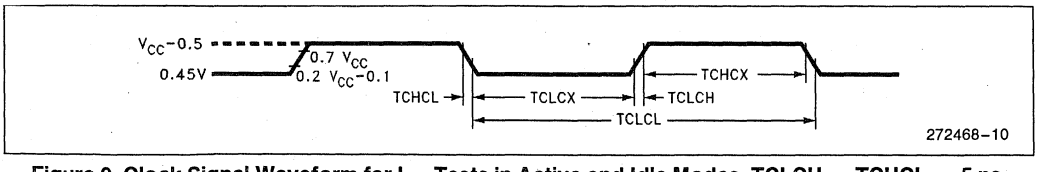


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XL5X refers to 8XL5X and 8XL5X-1.

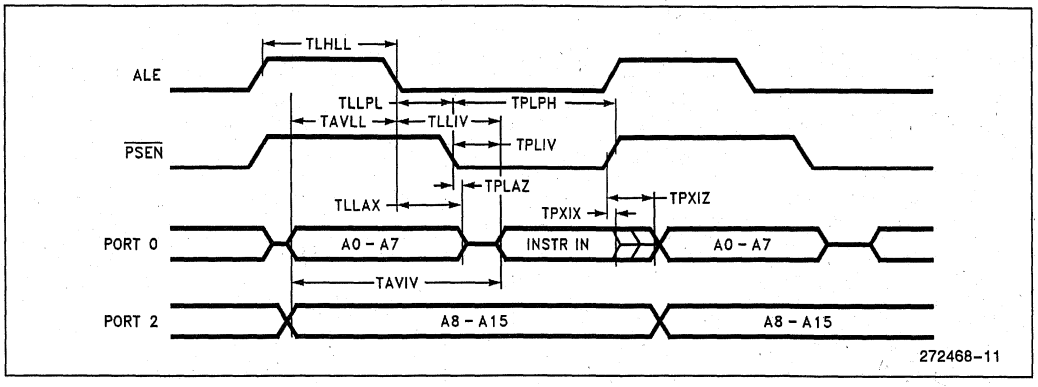
Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 8XL5X 8XL5X-1 8XL5X-20					 3.5 3.5 3.5	 12 16 20	 MHz MHz MHz
TLHLL	ALE Pulse Width	127		60		2 TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	43		10		TCLCL − 40		ns
TLLAX	Address Hold After ALE Low	53		20		TCLCL − 30		ns
TLLIV	ALE Low to Valid Instruction In 8XL5X 8XL5X-20		 234		 125		 4 TCLCL − 100 4 TCLCL − 75	 ns ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		20		TCLCL − 30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		105		3 TCLCL − 45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In 8XL5X 8XL5X-20		 145		 60		 3 TCLCL − 105 3 TCLCL − 90	 ns ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		0		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

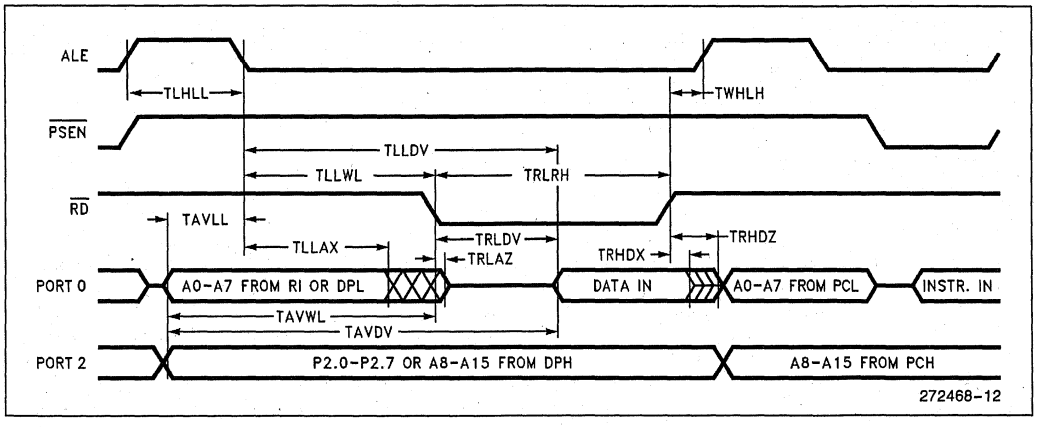
All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TPXIZ	Input Instruction Float After $\overline{PSEN}$ 8XL5X 8XL5X-20		 59		 30		 TCLCL − 25 TCLCL − 20	 ns ns
TAVIV	Address to Valid Instruction In		312		145		5 TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		200		6 TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		200		6 TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In 8XL5X 8XL5X-20		 252		 155		 5 TCLCL − 165 5 TCLCL − 95	 ns ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		40		2 TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In 8XL5X 8XL5X-20		 517		 310		 8 TCLCL − 150 8 TCLCL − 90	 ns ns
TAVDV	Address to Valid Data In 8XL5X 8XL5X-20		 585		 360		 9 TCLCL − 165 9 TCLCL − 90	 ns ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	100	200	3 TCLCL − 50	3 TCLCL + 50	ns
TAVWL	Address Valid to $\overline{WR}$ Low 8XL5X 8XL5X-20	 203		 110		 4 TCLCL − 130 4 TCLCL − 90		 ns ns
TQVWX	Data Valid before $\overline{WR}$ 8XL5X 8XL5X-20	 33		 15		 TCLCL − 50 TCLCL − 35		 ns ns
TWHQX	Data Hold after $\overline{WR}$ 8XL5X 8XL5X-20	 33		 10		 TCLCL − 50 TCLCL − 40		 ns ns
TQVWH	Data Valid to $\overline{WR}$ High 8XL5X 8XL5X-20	 433		 280		 7 TCLCL − 150 7 TCLCL − 70		 ns ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	10	90	TCLCL − 40	TCLCL + 40	ns

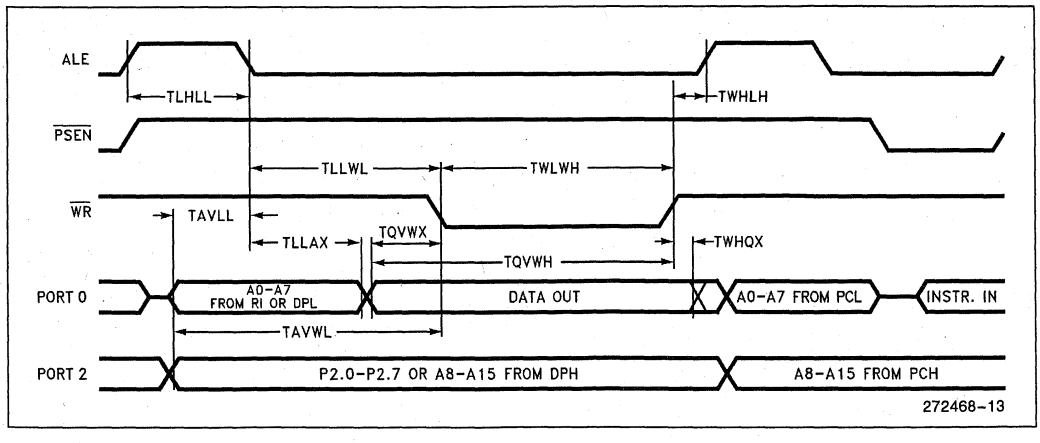
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

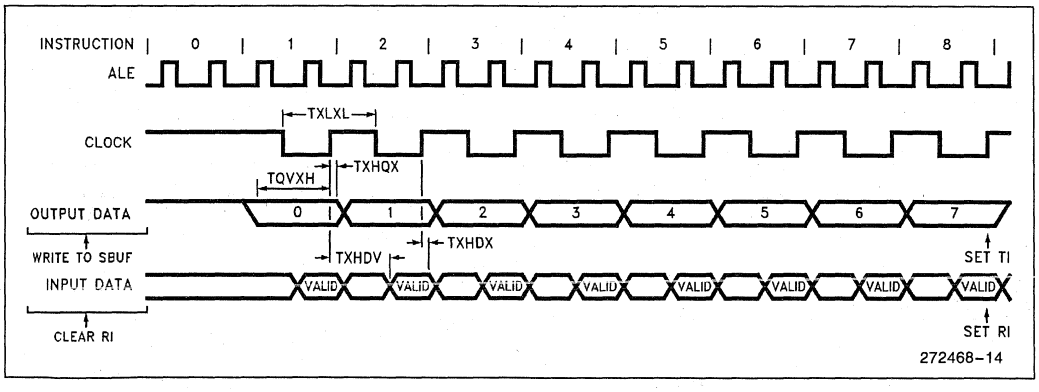


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.600		12 TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		367		10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge							
	8XL5X	50				2 TCLCL − 117		ns
	8XL5X-20			50		2 TCLCL − 50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		367		10 TCLCL − 133	ns

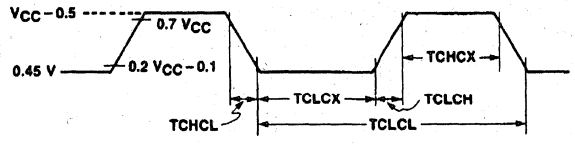
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

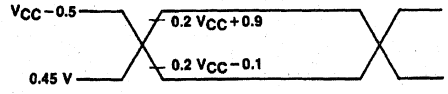
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XL5X 8XL5X-1 8XL5X-20	 3.5 3.5 3.5	 12 16 20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



272468-15

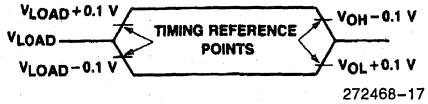
AC TESTING INPUT, OUTPUT WAVEFORMS



272468-16

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272468-17

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA (-L, $I_{OL}/I_{OH} = \pm 10$ mA).

PROGRAMMING THE OTP ROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal OTP ROM locations.) The address of an OTP ROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, RST $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 3. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed OTP ROM location. The setup is shown in Figure 10.

Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

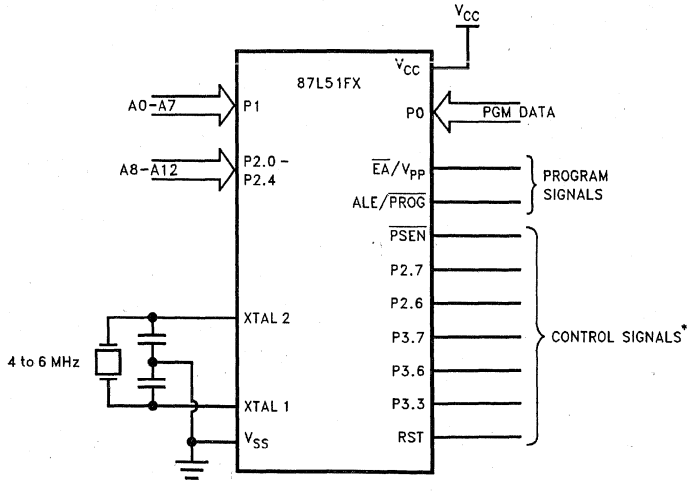
NOTE:

- $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.

Table 3. OTP ROM Programming Modes

(H = 2.7V to 3.6V; H1 = 5V ±10%)

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7	V_{CC}
Program Code Data		H1	L	⊓	12.75V	L	H1	H1	H1	H1	H1
Verify Code Data		H	L	H	H	L	L	L	H	H	H
Program Encryption Array Address 0–3FH		H1	L	⊓	12.75V	L	H1	H1	L	H1	H1
Program Lock Bits	Bit 1	H1	L	⊓	12.75V	H1	H1	H1	H1	H1	H1
	Bit 2	H1	L	⊓	12.75V	H1	H1	H1	L	L	H1
	Bit 3	H1	L	⊓	12.75V	H1	L	H1	H1	L	H1
Read Signature Byte		H	L	H	H	L	L	L	L	L	H



*See Table 2 for proper input on these pins

Figure 10. Programming the OTP ROM

PROGRAMMING ALGORITHM

Refer to Table 3 and Figures 10 and 11 for address, data, and control signals set up. To program the 87L5X the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse, ALE/$\overline{PROG}$ 5 times for the OTP ROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 8XL5X.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

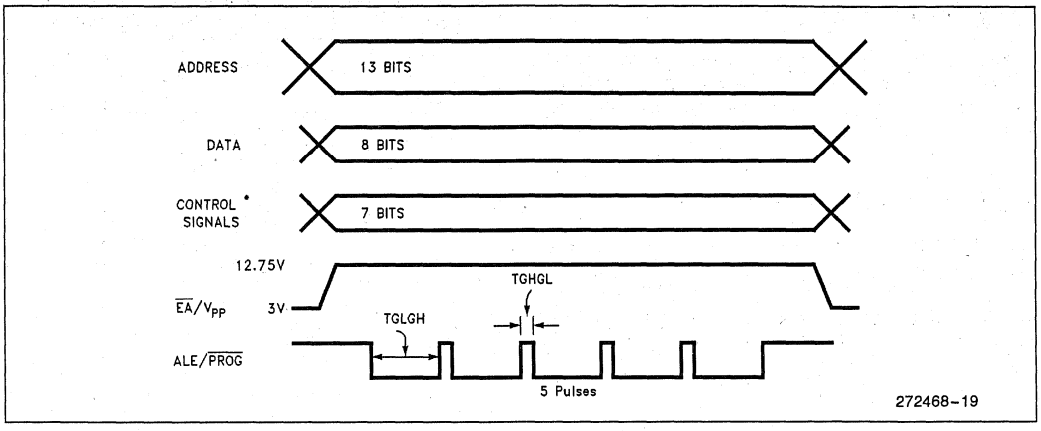


Figure 11. Programming Signals Waveforms

ROM and OTP ROM Lock System

The 87L5X program lock system, when programmed, protects the onboard program against software piracy.

The 80L5X has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 4. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87L5X has a 3-level program lock system and a 64-byte encryption array. Since this is an OTP ROM device, all locations are user-programmable. See Table 4.

Encryption Array

Within the OTP ROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 3 (Programming the OTP ROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Table 4. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the OTP ROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

Program Lock Bits

The 8XL5X has 3 programmable lock bits that when programmed according to Table 4 will provide different levels of protection for the on-chip code and data.

Reading the Signature Bytes

The 87L5X/80L5X has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for OTP ROM verify, but activate the control lines provided in Table 3 for Read Signature Byte.

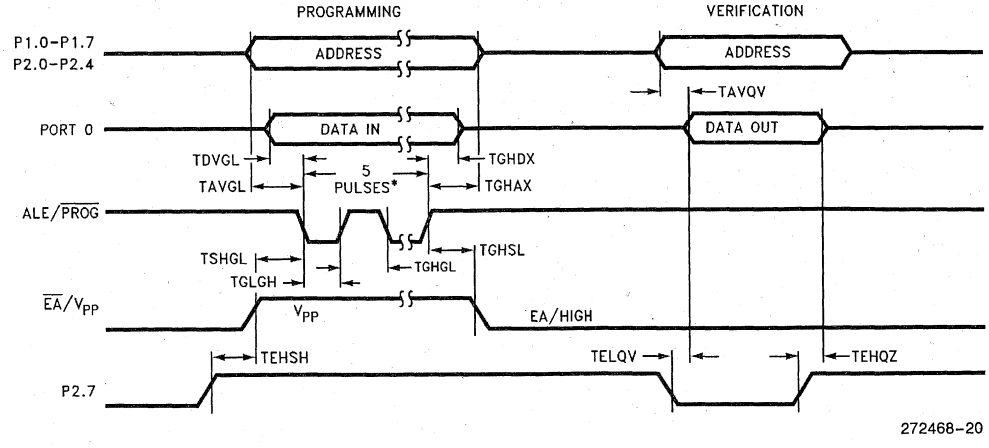
Location	Device	Contents
30H	All	89H
31H	All	58H
60H	80L52	30
	87L52	B0
	80L54	31
	87L54	B1
	80L58	32
	87L58	B2

OTP ROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 2.7V to 3.6V; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 (ENABLE) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	100	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

OTP ROM PROGRAMMING AND VERIFICATION WAVEFORMS



NOTE:
*5 pulses for the OTP ROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel Packaging Handbook (Order Number 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
N	46°C/W	16°C/W	All
S	87°C/W	18°C/W	52
	96°C/W	24°C/W	54
	90°C/W	22°C/W	58

DATA SHEET REVISION HISTORY

This is the first issue of this data sheet.

8XL51FA/FB/FC LOW VOLTAGE CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLERS

Commercial/Express

87L51FA/83L51FA/80L51FA/87L51FB/83L51FB/87L51FC/83L51FC

- High Performance CHMOS OTP ROM/ROM/CPU
- Low Voltage Operation
- 20 MHz Commercial/16 MHz Express Operation
- Three 16-Bit Timer/Counters
- Programmable Counter Array with:
  - — High Speed Output,
  - — Compare/Capture,
  - — Pulse Width Modulator,
  - — Watchdog Timer Capabilities
- Up/Down Timer/Counter
- Three Level Program Lock System
- 8K/16K/32K On-Chip Program Memory
- 256 Bytes of On-Chip Data RAM
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 7 Interrupt Sources
- Four Level Interrupt Priority
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS® 51 Microcontroller Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode
- Extended Temperature Range (−40°C to +85°C)

MEMORY ORGANIZATION

ROM Device	OTP ROM Version	ROMLESS Version	ROM/ OTP ROM Bytes	RAM Bytes
83L51FA	87L51FA	80L51FA	8K	256
83L51FB	87L51FB	80L51FA	16K	256
83L51FC	87L51FC	80L51FA	32K	256

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 8XL51FA/8XL51FB/8XL51FC is a single-chip control oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS® 51 microcontroller family, the 8XL51FA/8XL51FB/8XL51FC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 microcontroller products.

The 8XL51FX is a 3V version of current 8XC51FX and will operate from 2.7V to 3.6V at a frequency range of 3.5 MHz to 16 MHz (Express)/20 MHz (Commercial).

For the remainder of this document, the 8XL51FA, 8XL51FB, 8XL51FC will be referred to as the 8XL51FX, unless information applies to a specific device.

December 1996

Order Number: 272356-004

	Standard	−1	−20*
80L51FA	X	X	X
83L51FA	X	X	X
87L51FA	X	X	X
83L51FB	X	X	X
87L51FB	X	X	X
83L51FC	X	X	X
87L51FC	X	X	X

NOTE:
Standard 3.5 MHz to 12 MHz; 2.7V to 3.6V
−1 3.5 MHz to 16 MHz; 2.7V to 3.6V
−20* 3.5 MHz to 20 MHz; 2.7V to 3.6V
*Only available for commercial standard temperature range, not available at express temperature range.

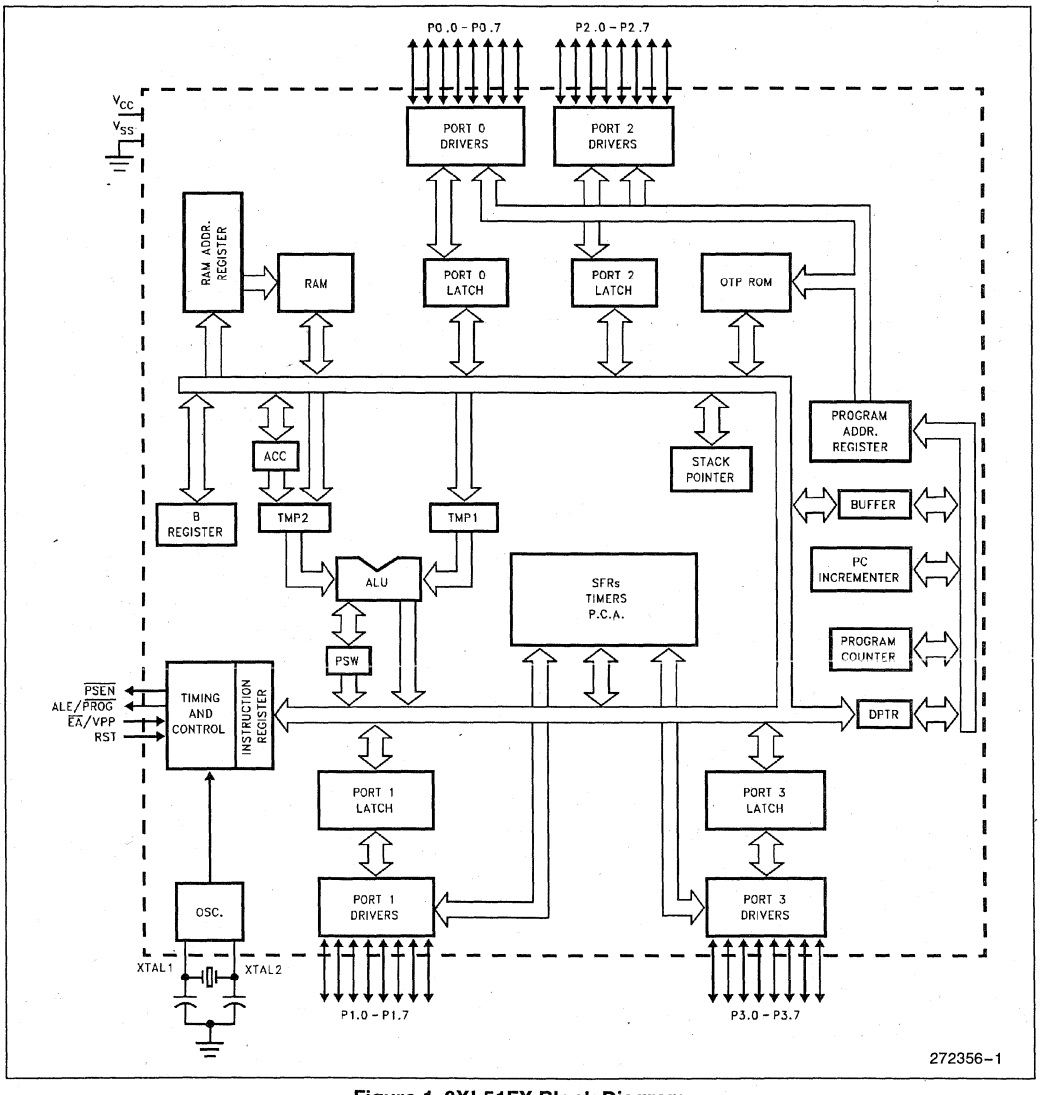


Figure 1. 8XL51FX Block Diagram

PROCESS INFORMATION

The 8XL51FA/8XL51FB/8XL51FC is manufactured on the CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

Part	Prefix	Package Type
8XL51FX	N	44-Pin PLCC (OTP)
	S	44-Pin QFP (OTP)

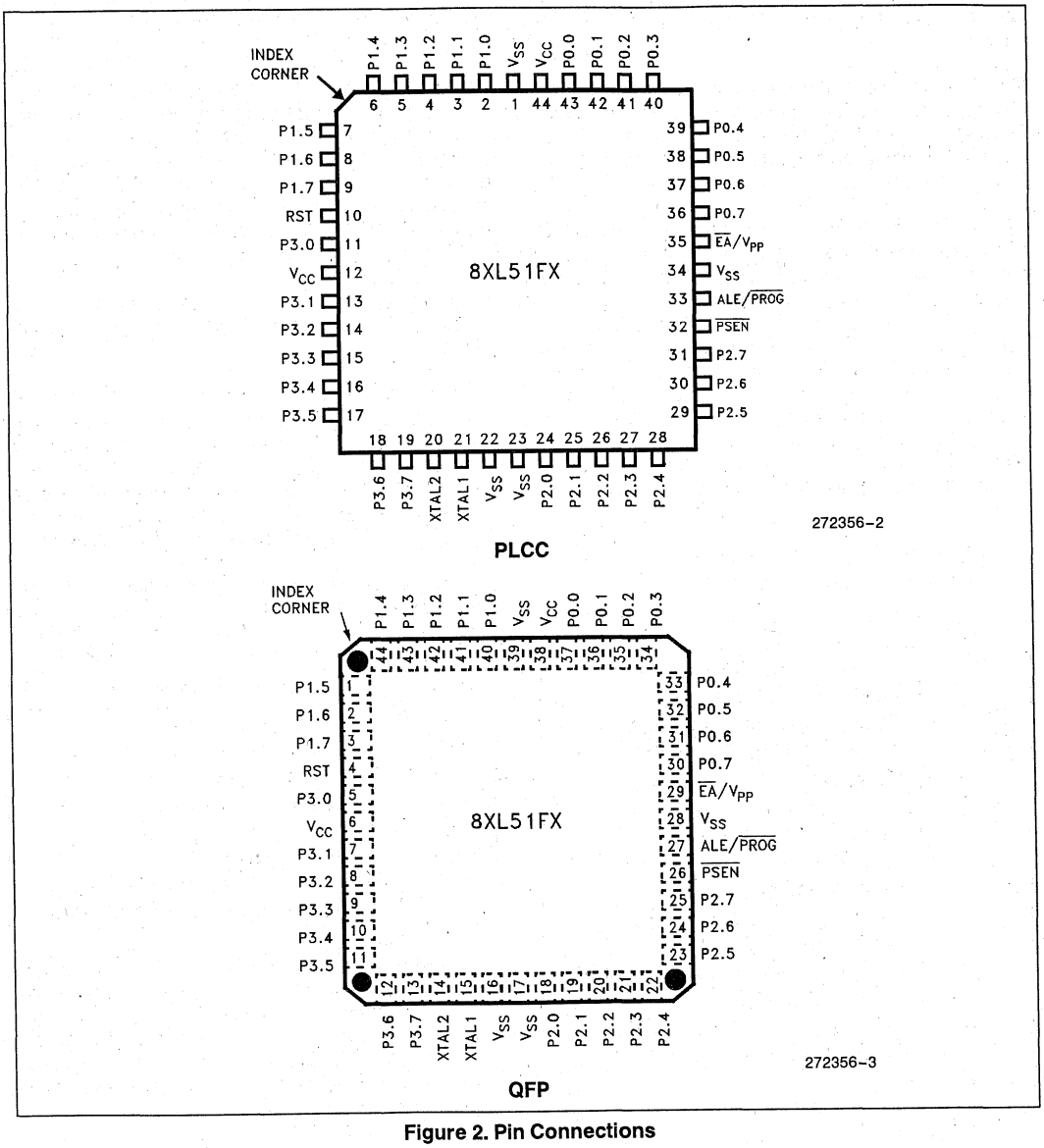


Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several inputs.

Port 0 also receives the code bytes during OTP ROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive several inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XL51FX:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during OTP ROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive several inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during OTP ROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive several inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS 51 microcontroller family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH2} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during OTP ROM programming for the 87L51FX.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XL51FX is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ must be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during OTP ROM programming.

XTAL1: Input to the inverting oscillator amplifier.

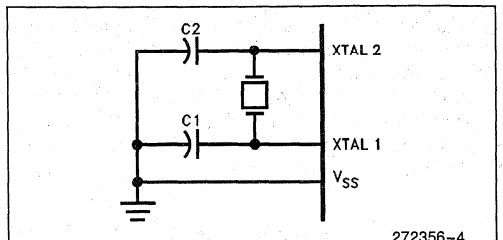
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

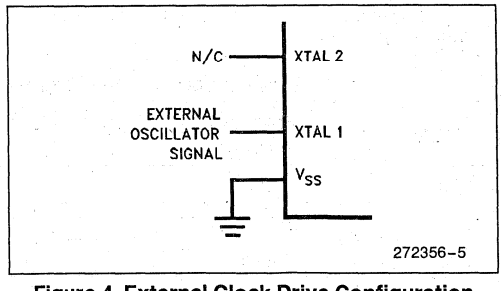


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XL51FX either hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

- The 8XL51FX will operate from 2.7V to 3.6V with a frequency range of 3.5 MHz to 16 MHz (Express)/20 MHz (Commercial). Operating beyond these specifications could cause improper device functionality.
- All V_{CC} and V_{SS} pins must be connected. Please refer to Figure 2, Pin Connections, for the specific pins.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XL51FX without the 8XL51FX having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XL51FX is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, #270646, and Application Note AP-252 (Embedded Applications Handbook), #270648, "Designing with the 80C51BH."

8XL51FX EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS-51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 2.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

Table 2. Prefix Identification

Prefix	Package Type	Temperature Range
N	PLCC	Commercial
S	QFP	Commercial
TN	PLCC	Extended
TS	QFP	Extended

NOTE:
Contact your distributor or local sales office to match the EXPRESS prefix with the proper device.

EXAMPLES:
N87L51FC indicates 87L51FC in a PLCC package and specified for commercial temperature range, without burn-in.

TN87L51FC indicates 87L51FC in a PLCC package and specified for extended temperature range with burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	2.7	3.6	V

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except XTAL1, RST)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, RST)	−0.5	0.2 V_{CC} − 0.1	V	
V_{IH}	Input High Voltage (Except XTAL1, RST, $\overline{EA}$)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{EA}$)	V_{CC} − 1.0	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Note 4) (Ports 1, 2 and 3)		0.4	V	I_{OL} = 1.6 mA (Note 1)
V_{OL1}	Output Low Voltage (Note 4) (Port 0, ALE/$\overline{PSEN}$)		0.4	V	I_{OL} = 3.2 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$	V_{CC} − 0.7		V	I_{OH} = −30 µA (Note 2)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4		V	I_{OH} = −1.0 mA (Note 2)
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)		−50	µA	V_{IN} = 0.4V
I_{LI}	Input Leakage Current (Port 0)		±10	µA	0 < V_{IN} < V_{CC}

DC CHARACTERISTICS (Over Operating Conditions)

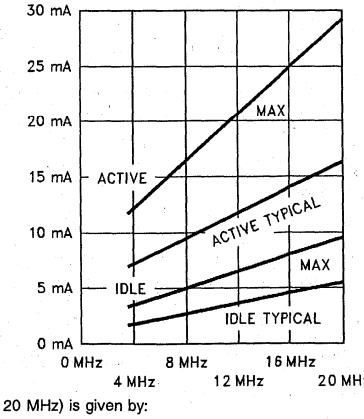
All parameter values apply to all devices unless otherwise indicated. (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		−350	μA	V_{IN} = 1.4V
RRST	RST Pulldown Resistor	40	225	KΩ	
I_{CC}	Power Supply Current Active Mode at 16 MHz Idle Mode at 16 MHz Power-Down Mode		 25 8 30	 mA mA μA	(Note 3)

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitance loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for power down is 2V.
4. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
Running the device with $\overline{EA}$ at a higher voltage than V_{CC} sinks additional currrent.



I_{CC} Max at other frequencies (3.5 MHz to 20 MHz) is given by:
Active Mode
I_{CC} MAX = 1.1 × FREQ + 7.6
Idle Mode
I_{CC} MAX = 0.4 × FREQ + 1.8
Where FREQ is in MHz, I_{CC} MAX is given in mA.

Figure 5. I_{CC} vs Frequency

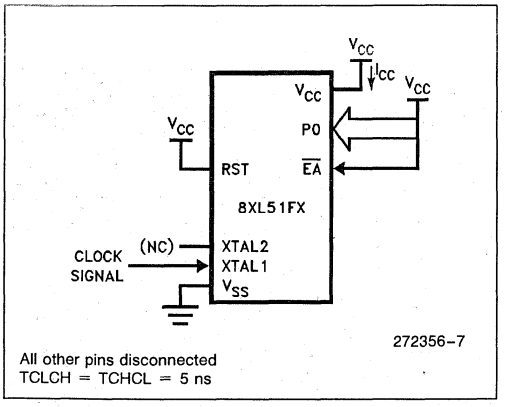


Figure 6. I_{CC} Test Condition, Active Mode

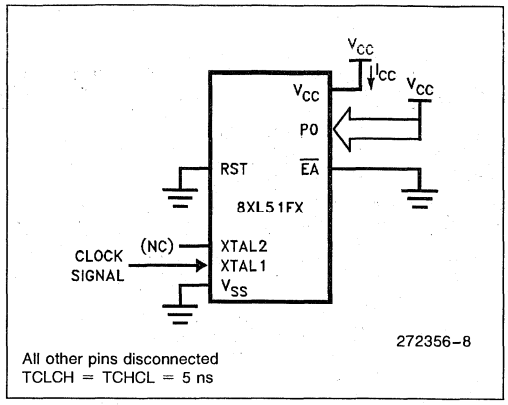


Figure 7. I_{CC} Test Condition Idle Mode

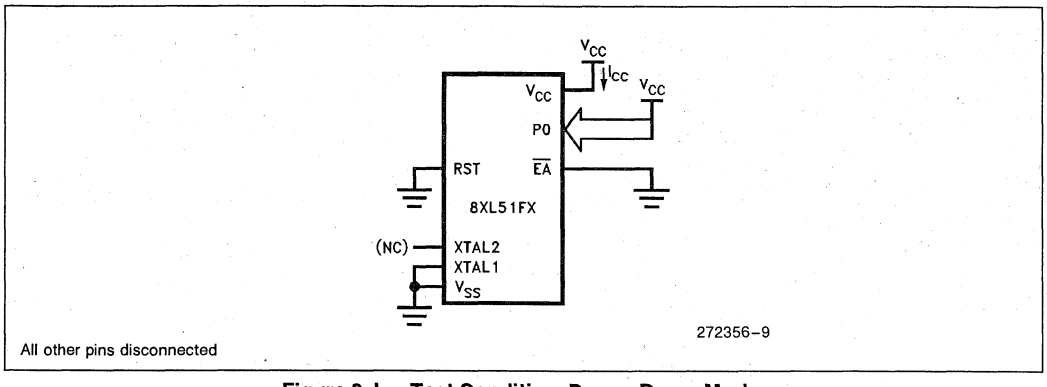


Figure 8. I_{CC} Test Condition, Power Down Mode.
V_{CC} = 2.7V to 3.6V.

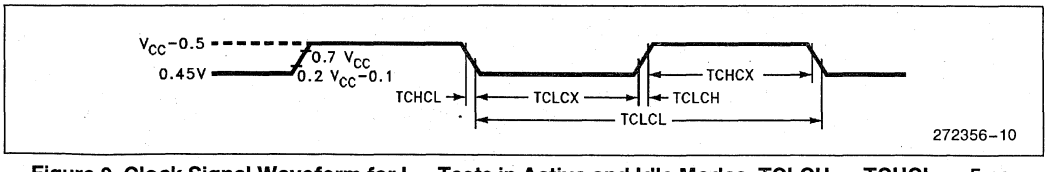


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ signal
T: Time
V: Valid
W: $\overline{WR}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XL51FX refers to 8XL51FX and 8XL51FX-1.

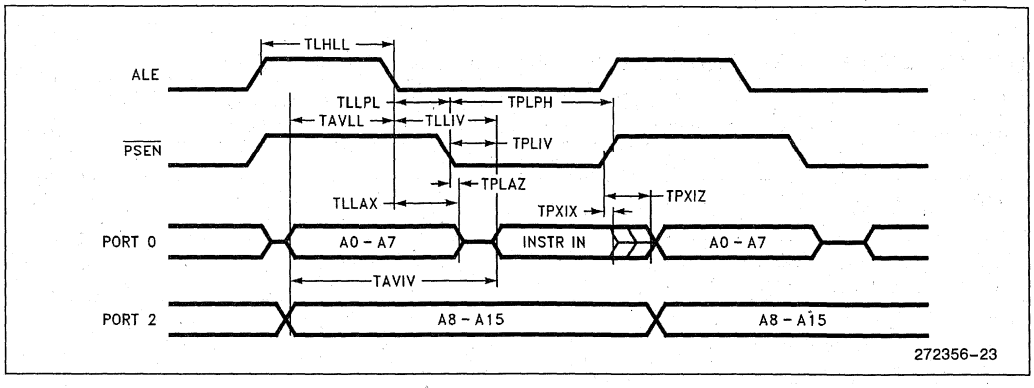
Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 8XL51FX 8XL51FX-1 8XL51FX-20					 3.5 3.5 3.5	 12 16 20	 MHz MHz MHz
TLHLL	ALE Pulse Width	127		60		2 TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	43		10		TCLCL − 40		ns
TLLAX	Address Hold After ALE Low	53		20		TCLCL − 30		ns
TLLIV	ALE Low to Valid Instruction In 8XL51FX 8XL51FX-20		 234		 125		 4 TCLCL − 100 4 TCLCL − 75	 ns ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	53		20		TCLCL − 30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		105		3 TCLCL − 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In 8XL51FX 8XL51FX-20		 145		 60		 3 TCLCL − 105 3 TCLCL − 90	 ns ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		0		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

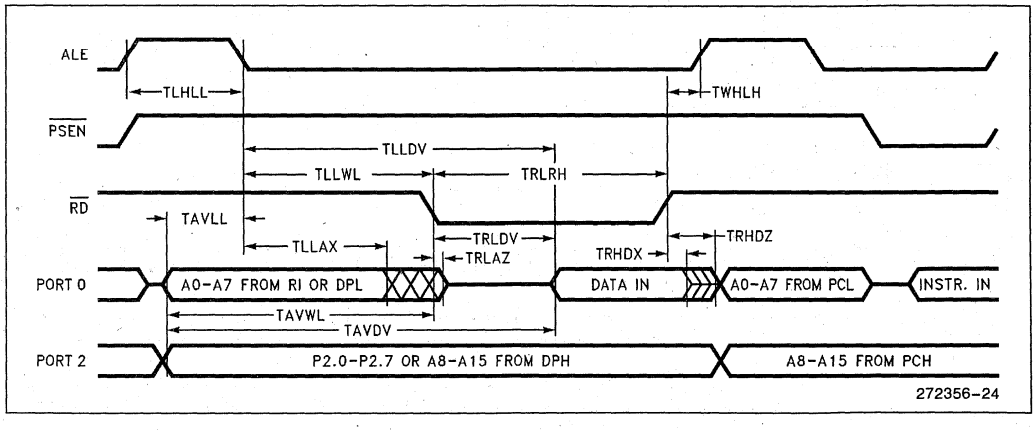
All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TPXIZ	Input Instruction Float After $\overline{PSEN}$							
	8XL51FX		59				TCLCL − 25	ns
	8XL51FX-20				30		TCLCL − 20	ns
TAVIV	Address to Valid Instruction In		312		145		5 TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		200		6 TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		200		6 TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In							
	8XL51FX		252				5 TCLCL − 165	ns
	8XL51FX-20				155		5 TCLCL − 95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		40		2 TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In							
	8XL51FX		517				8 TCLCL − 150	ns
	8XL51FX-20				310		8 TCLCL − 90	ns
TAVDV	Address to Valid Data In							
	8XL51FX		585				9 TCLCL − 165	ns
	8XL51FX-20				360		9 TCLCL − 90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	100	200	3 TCLCL − 50	3 TCLCL + 50	ns
TAVWL	Address Valid to $\overline{WR}$ Low							
	8XL51FX	203				4 TCLCL − 130		ns
	8XL51FX-20			110		4 TCLCL − 90		ns
TQVWX	Data Valid before $\overline{WR}$							
	8XL51FX	33				TCLCL − 50		ns
	8XL51FX-20			15		TCLCL − 35		ns
TWHQX	Data Hold after $\overline{WR}$							
	8XL51FX	33				TCLCL − 50		ns
	8XL51FX-20			10		TCLCL − 40		ns
TQVWH	Data Valid to $\overline{WR}$ High							
	8XL51FX	433				7 TCLCL − 150		ns
	8XL51FX-20			280		7 TCLCL − 70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	10	90	TCLCL − 40	TCLCL + 40	ns

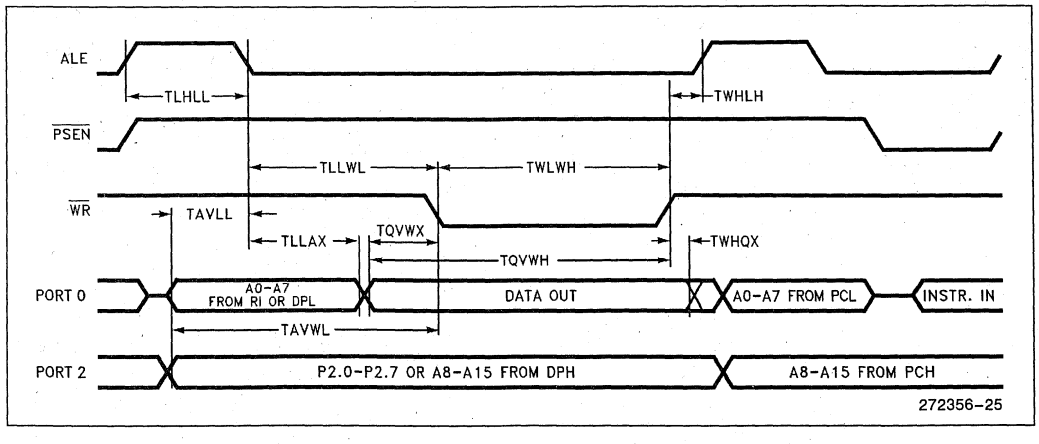
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

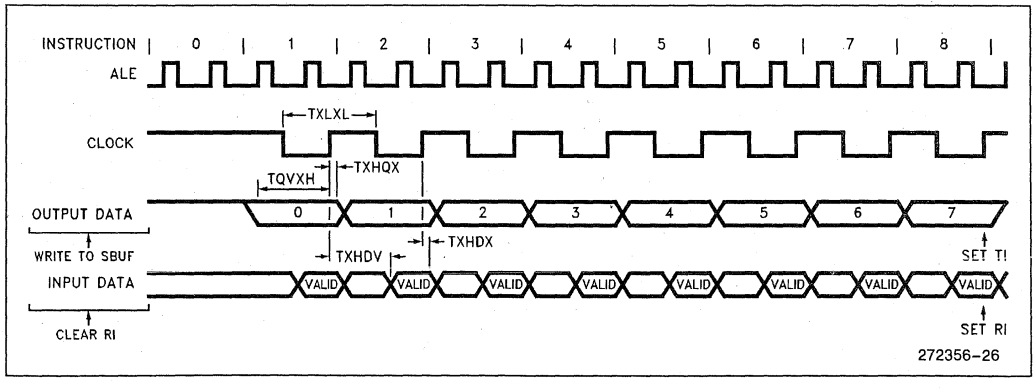


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.600		12 TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		367		10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge							
	8XC5X	50				2 TCLCL − 117		ns
	8XC5X-20			50		2 TCLCL − 50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		367		10 TCLCL − 133	ns

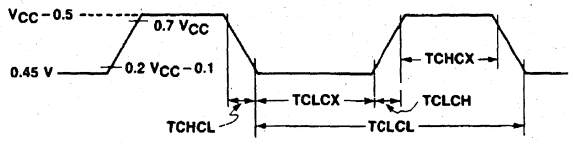
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

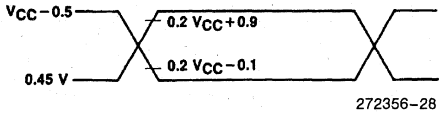
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XL51FX 8XL51FX-1 8XL51FX-20	 3.5 3.5 3.5	 12 16 20	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



272356-27

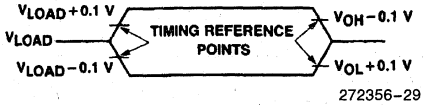
AC TESTING INPUT, OUTPUT WAVEFORMS



272356-28

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272356-29

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA (-L, $I_{OL}/I_{OH} = \pm 10$ mA).

PROGRAMMING THE OTP ROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal OTP ROM locations.) The address of an OTP ROM location to be programmed is applied to Port 1 and pins P2.0 - P2.4 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 and 3 pins, RST $\overline{PSEN}$, and $\overline{EA}/V_{PP}$ should be held at the "Program" levels indicated in Table 3. ALE/$\overline{PROG}$ is pulsed low to program the code byte into the addressed OTP ROM location. The setup is shown in Figure 10.

Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. Then $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low, and then $\overline{EA}/V_{PP}$ is returned to a valid high voltage. The voltage on the $\overline{EA}/V_{PP}$ pin must be at the valid $\overline{EA}/V_{PP}$ high level before a verify is attempted. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

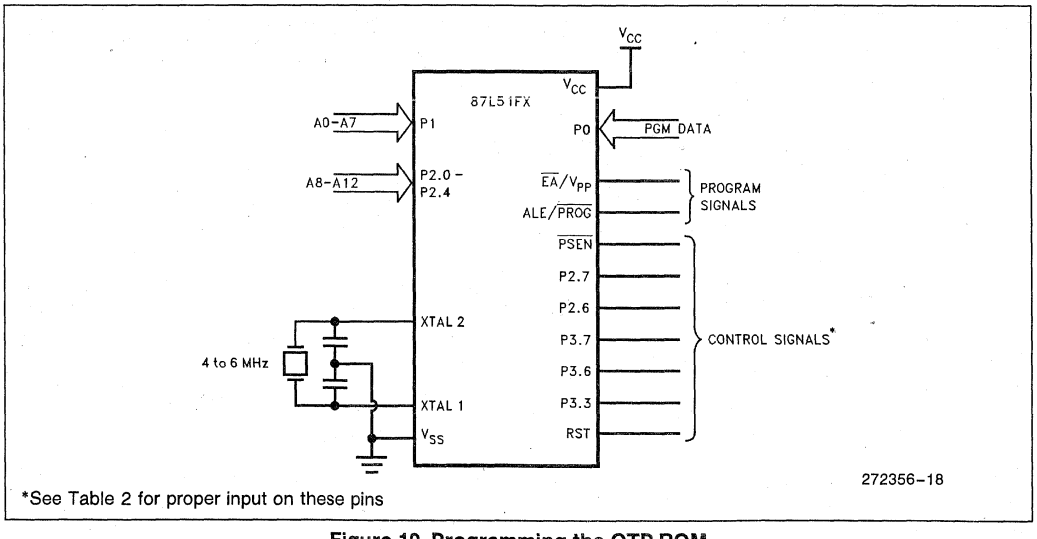
NOTE:

- $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.

Table 3. OTP ROM Programming Modes

(H = 2.7V to 3.6V; H1 = 5V ±10%)

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7	V_{CC}
Program Code Data		H1	L	⊓	12.75V	L	H1	H1	H1	H1	H1
Verify Code Data		H	L	H	H	L	L	L	H	H	H
Program Encryption Array Address 0–3FH		H1	L	⊓	12.75V	L	H1	H1	L	H1	H1
Program Lock Bits	Bit 1	H1	L	⊓	12.75V	H1	H1	H1	H1	H1	H1
	Bit 2	H1	L	⊓	12.75V	H1	H1	H1	L	L	H1
	Bit 3	H1	L	⊓	12.75V	H1	L	H1	H1	L	H1
Read Signature Byte		H	L	H	H	L	L	L	L	L	H



*See Table 2 for proper input on these pins

Figure 10. Programming the OTP ROM

PROGRAMMING ALGORITHM

Refer to Table 3 and Figures 10 and 11 for address, data, and control signals set up. To program the 87L51FX the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse, ALE/$\overline{PROG}$ 5 times for the OTP ROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87L51FX.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

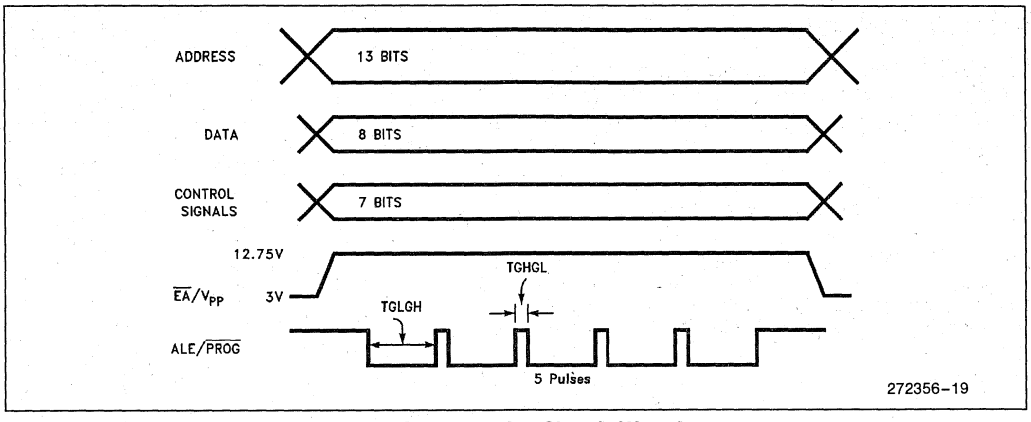


Figure 11. Programming Signals Waveforms

ROM and OTP ROM Lock System

The 87L51FX program lock system, when programmed, protects the onboard program against software piracy.

The 83L51FX has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 4. If program protection is desired, the user submits the encryption table with their code, and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87L51FX has a 3-level program lock system and a 64-byte encryption array. Since this is an OTP ROM device, all locations are user-programmable. See Table 4.

Encryption Array

Within the OTP ROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 3 (Programming the OTP ROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Table 4. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the OTP ROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

Program Lock Bits

The 87L51FX has 3 programmable lock bits that when programmed according to Table 4 will provide different levels of protection for the on-chip code and data.

Reading the Signature Bytes

The 87L51FX/83L51FX has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for OTP ROM verify, but activate the control lines provided in Table 3 for Read Signature Byte.

Location	Device	Contents
30H	All	89H
31H	All	58H
60H	83L51FA	70H
	87L51FA	F0H
	83L51FB	71H
	87L51FB	F1H
	83L51FC	72H
	87L51FC	F2H

8XC51RA/RB/RC
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Commercial/Express

87C51RA/83C51RA/80C51RA/87C51RB/83C51RB/87C51RC/83C51RC

*See Table 1 for Proliferation Options

- High Performance CHMOS EPROM/ ROM/CPU
- 24 MHz Operation
- 512 Bytes of On-Chip Data RAM
- Dedicated Hardware Watchdog Timer (One-Time Enabled with Reset-Out)
- Three 16-Bit Timer/Counters
- Programmable Clock Out
- Up/Down Timer/Counter
- Three Level Program Lock System
- 8K/16K/32K On-Chip Program Memory
- Improved Quick Pulse Programming Algorithm
- Boolean Processor
- 32 Programmable I/O Lines
- 6 Interrupt Sources
- Programmable Serial Channel with:
  - Framing Error Detection
  - Automatic Address Recognition
- TTL and CMOS Compatible Logic Levels
- 64K External Program Memory Space
- 64K External Data Memory Space
- MCS® 51 Compatible Instruction Set
- Power Saving Idle and Power Down Modes
- ONCE (On-Circuit Emulation) Mode
- Four-Level Interrupt Priority
- Extended Temperature Range (−40°C to +85°C)

MEMORY ORGANIZATION

ROMless Device	ROM Device	EPROM Version	ROM/EPROM Bytes	RAM Bytes
80C51RA	83C51RA	87C51RA	8K	512
80C51RA	83C51RB	87C51RB	16K	512
80C51RA	83C51RC	87C51RC	32K	512

These devices can address up to 64 Kbytes of external program/data memory.

The Intel 8XC51RA/8XC51RB/8XC51RC is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS 51 family of controllers, the 8XC51RA/8XC51RB/8XC51RC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 family of products. The 8XC51RA/8XC51RB/8XC51RC is an enhanced version of the 8XC52/8XC54/8XC58. The added features make it an even more powerful microcontroller for applications that require 512 bytes of on-chip data RAM and dedicated hardware WatchDog Timer with reset-out features.

Throughout this document 8XC51RX will refer to the 8XC51RA, 8XC51RB and 8XC51RC unless information applies to a specific device.

For a detailed description of 8XC51RA/RB/RC, refer to the 8XC51RA/RB/RC Hardware Description, order number 272668.

December 1996

Order Number: 272659-003

Table 1. Proliferations Options

	Standard*1	-1	-20	-24
80C51RA	X	X	X	X
83C51RA	X	X	X	X
87C51RA	X	X	X	X
83C51RB	X	X	X	X
87C51RB	X	X	X	X
83C51RC	X	X	X	X
87C51RC	X	X	X	X

NOTES:
*1 3.5 MHz to 12 MHz; 5V ±20%
-1 3.5 MHz to 16 MHz; 5V ±20%
-20 3.5 MHz to 20 MHz; 5V ±20%
-24 3.5 MHz to 24 MHz; 5V ±10%

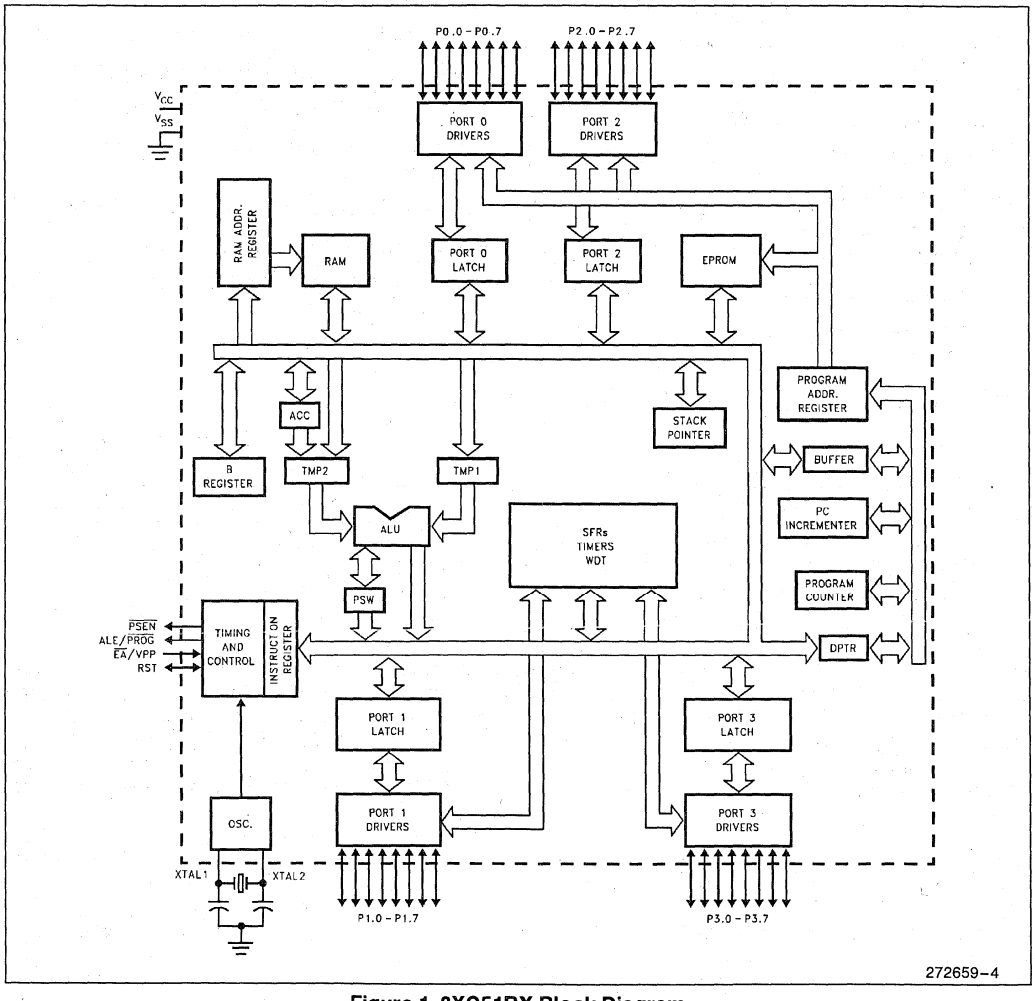


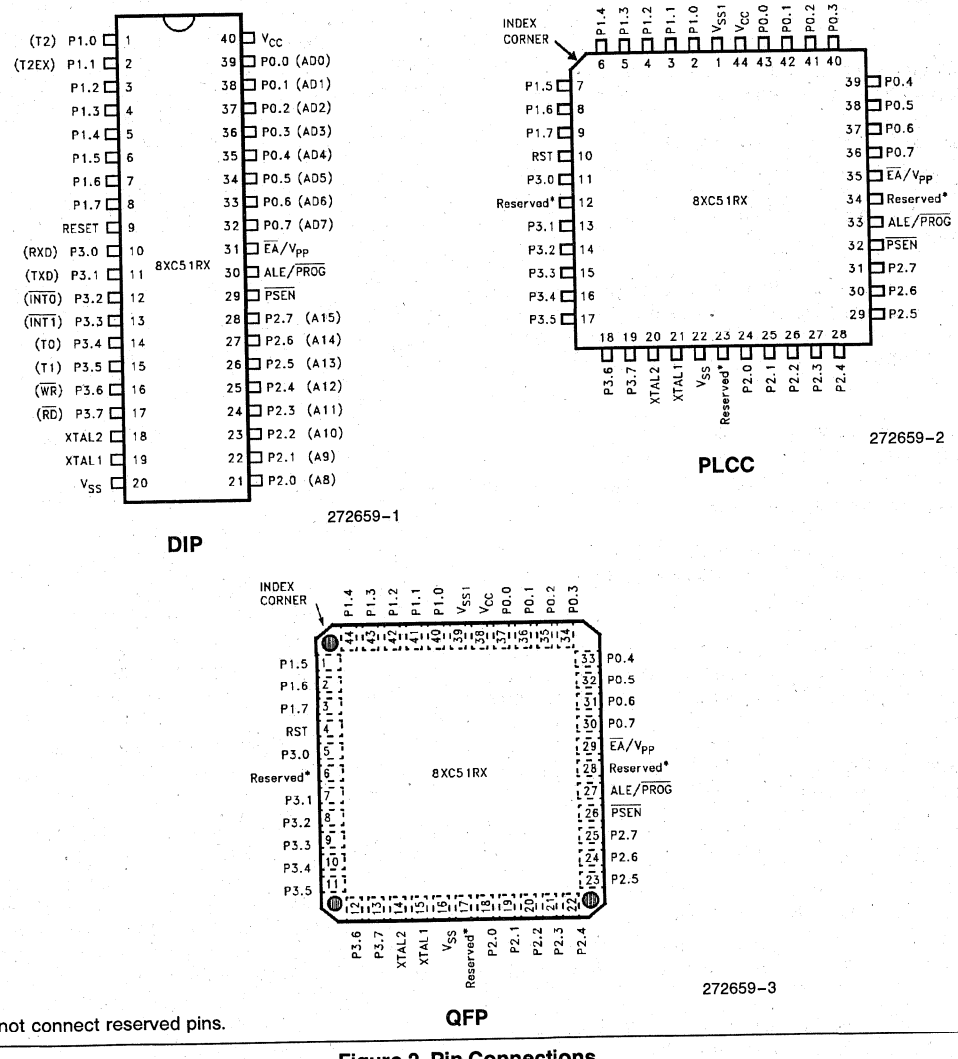
Figure 1. 8XC51RX Block Diagram

PROCESS INFORMATION

This device is manufactured on the CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order No. 210997.

PACKAGES

Part	Prefix	Package Type
8XC51RX	P	40-Pin Plastic DIP (OTP)
8XC51RX	N	44-Pin PLCC (OTP)
8XC51RX	S	44-Pin QFP (OTP)



*Do not connect reserved pins.

Figure 2. Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (not on DIP). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is not a substitute for the V_{SS} pin (pin 22). (Connection not necessary for proper operation.)

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 8XC51RX:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the 8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset I/O. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IHI} voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}. After a WatchDog Timer overflow, this RST pin will drive an output high pulse at a minimum V_{OH2} for 96 x T_{OSC} duration while the internal reset signal is active.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to ex-

ternal memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51RX.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51RX is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if any of the Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

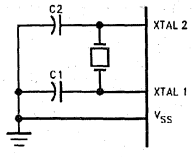
This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers", Order No. 230659.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

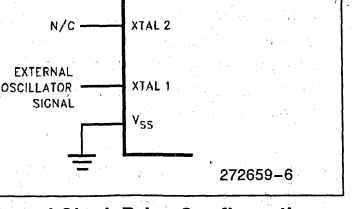


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Mode will be exited if the chip is reset or if an enabled interrupt occurs.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51RX either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level, and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DEDICATED HARDWARE WATCHDOG TIMER (One-Time Enabled with Reset-Out)

The 8XC51RX contains a dedicated WatchDog Timer (WDT) to allow recovery from software or hardware upset. WDT is disabled upon power-up. To enable the WDT, user must write 1EH and E1H in sequence to WDTRST Special Function Register. Once the WDT is enabled, the 14-bit counter will increment every machine cycle. While the oscillator is running, the WDT will be incrementing and cannot be disabled. The counter is reset by writing 1EH and E1H in sequence to the WDTRST. If the counter is not reset before it reaches 3FFFH (16383D), the chip will be forced into reset sequence and the WDT will be disabled as upon power-up. During this reset, the chip will drive an output Reset-High pulse for the duration of 96 x T_{OSC} at the RST pin. The duration of the Reset-High pulse works out to 6.00 μs @ 16 MHz.

While in the Idle mode the WDT continues to count. If the user does not wish to exit the Idle mode with a reset, then the processor must periodically "woken up" to service the WDT. In Power Down mode, the WDT stops counting and holds its current value.

DESIGN CONSIDERATION

- The window on the D87C51RX must be covered by an opaque label. Otherwise, the DC and AC characteristics may not be met, and the device may be functionally impaired.
- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, (Order No. 270645) and Application Note AP-252 (Embedded Applications Handbook, Order No. 270648), "Designing with the 80C51BH."

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51RX without the 8XC51RX having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51RX is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

8XC51RX EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the MCS 51 family of microcontrollers. These EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range with or without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic for a minimum time of 168 hours at 125°C with V_{CC} = 6.9V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 3.

For the extended temperature range option, this data sheet specifies the parameters which deviate from their commercial temperature range limits.

Table 3. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
P	Plastic	Commercial	No
N	PLCC	Commercial	No
S	QFP	Commercial	No
TP	Plastic	Extended	No
TN	PLCC	Extended	No
TS	QFP	Extended	No
LP	Plastic	Extended	Yes
LN	PLCC	Extended	Yes
LS	QFP	Extended	Yes

NOTE:
Contact distributor or local sales office to match EXPRESS prefix with proper device.

EXAMPLES:
P80C51RA indicates 80C51RA in a plastic package and specified for commercial temperature range, without burn-in.
TS87C51RC indicates 87C51RC in a QFP package and specified for extended temperature range, without burn-in.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on EA/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage			
	All Others	4.0	6.0	V
	8XC51RX-24	4.5	5.5	V
f_{OSC}	Oscillator Frequency			
	8XC51RX	3.5	12	MHz
	8XC51RX-1	3.5	16	MHz
	8XC51RX-20	3.5	20	MHz
	8XC51RX-24	3.5	24	MHz

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA
		V_{CC} − 0.7			V	I_{OH} = −30 μA
		V_{CC} − 1.5			V	I_{OH} = −60 μA

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

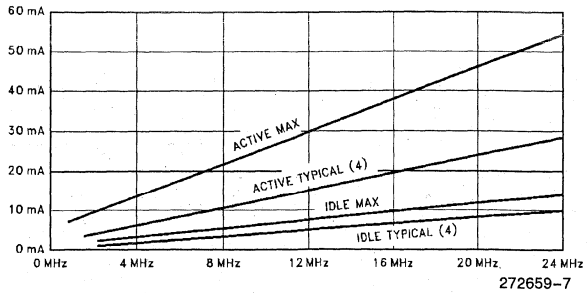
All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$V_{CC}-0.3$			V	$I_{OH} = -200\ \mu A$
		$V_{CC}-0.7$			V	$I_{OH} = -3.2$ mA
		$V_{CC}-1.5$			V	$I_{OH} = -7.0$ mA
V_{OH2}	Output High Voltage (RST)	$0.5\ V_{CC}$			V	$I_{OH} = -800\ \mu A$
		$0.75\ V_{CC}$			V	$I_{OH} = -300\ \mu A$
		$0.9\ V_{CC}$			V	$I_{OH} = -80\ \mu A$
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−50	μA	$V_{IN} = 0.45V$
I_{LI}	Input leakage Current (Port 0)			±10	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)					
	Commercial			−675	μA	$V_{IN} = 2V$
	Express			−775	μA	
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current:					(Note 3)
	Active Mode					
	at 12 MHz (Figure 5)		15	30	mA	
	at 16 MHz			38	mA	
	at 20 MHz			47	mA	
	at 24 MHz			56	mA	
	Idle Mode					
	at 12 MHz (Figure 5)		5	7.5	mA	
	at 16 MHz			9.5	mA	
	at 20 MHz			11.5	mA	
	at 24 MHz			13.5	mA	
	Power Down Mode		5	75	μA	

NOTES:

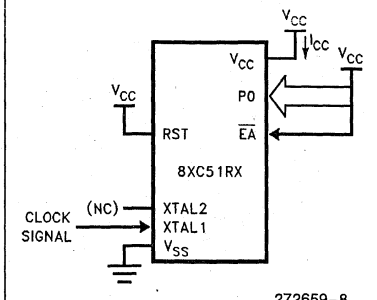
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



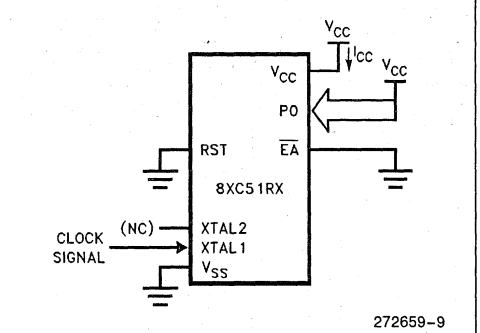
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = 2.2 × Freq + 3.1
Idle Mode
I_{CC} Max = 0.5 × Freq + 1.5
Where Freq is in MHz, I_{CC} Max is given in mA.

Figure 5. I_{CC} vs Frequency



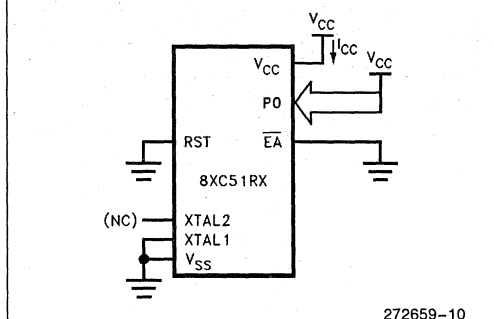
All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 6. I_{CC} Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition Idle Mode



All other pins disconnected

Figure 8. I_{CC} Test Condition, Power Down Mode V_{CC} = 2.0V to 6.0V

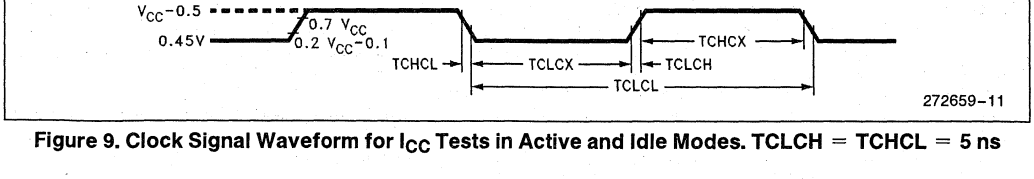


Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC CHARACTERISTICS (Over Operating Conditions, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

All parameter values apply to all devices unless otherwise indicated. In this table, 8XC51RX refers to 8XC51RX and 8XC51RX-1. 8XC51RX-24 refers to 8XC51RX-20 and 8XC51RX-24.

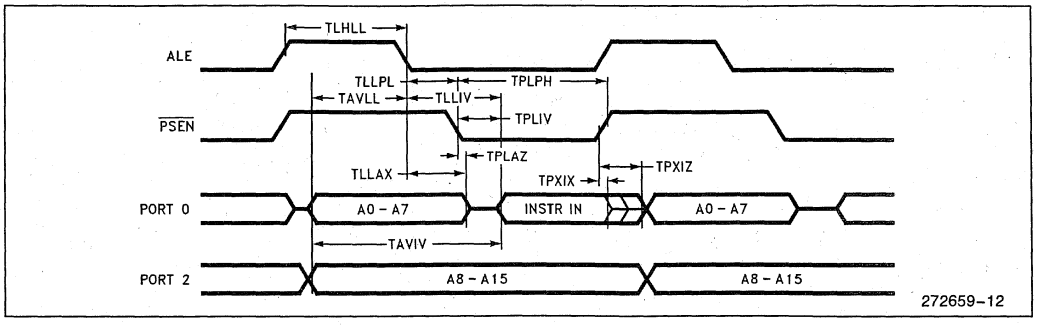
Symbol	Description	12 MHz Oscillator		20 MHz Oscillator		24 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 8XC51RX 8XC51RX-1 8XC51RX-20 8XC51RX-24							 3.5 3.5 3.5 3.5	 12 16 20 24	 MHz MHz MHz MHz
TLHLL	ALE Pulse Width	127		60		43		2 TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	43		10		12		TCLCL − 40		ns
TLLAX	Address Hold After ALE Low	53		20		12		TCLCL − 30		ns
TLLIV	ALE Low to Valid Instruction In 8XC51RX 8XC51RX-24		 234		 125		 91		 4 TCLCL − 100 4 TCLCL − 75	 ns ns
TLLPL	ALE Low to $\overline{\text{PSEN}}$ Low	53		20		12		TCLCL − 30		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	205		105		80		3 TCLCL − 45		ns
TPLIV	$\overline{\text{PSEN}}$ Low to Valid Instruction In 8XC51RX 8XC51RX-24		 145		 60		 35		 3 TCLCL − 105 3 TCLCL − 90	 ns ns
TPXIX	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		0		0		ns

EXTERNAL MEMORY CHARACTERISTICS (Continued)

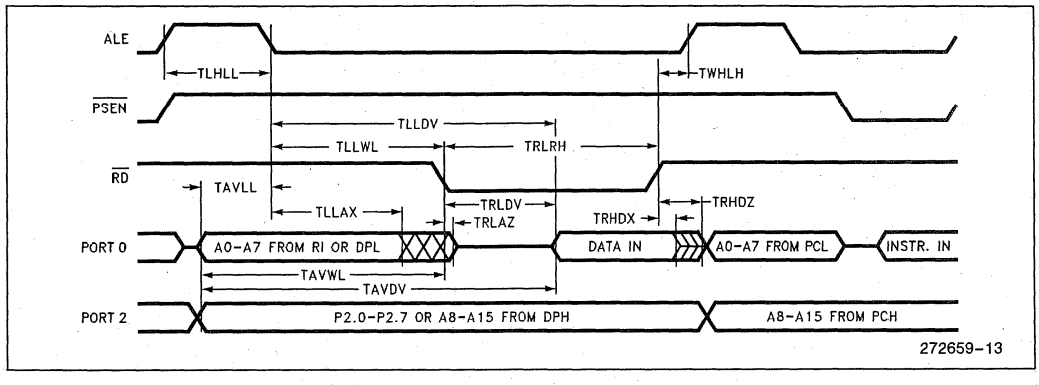
All parameter values apply to all devices unless otherwise indicated.

Symbol	Description	12 MHz Oscillator		20 MHz Oscillator		24 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
TPXIZ	Input Instruction Float After $\overline{PSEN}$									
	8XC51RX		59						TCLCL−25	ns
	8XC51RX-24				30		21		TCLCL−20	ns
TAVIV	Address to Valid Instruction In		312		145		103		5 TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		200		150		6 TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		200		150		6 TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In									
	8XC51RX		252						5 TCLCL−165	ns
	8XC51RX-24				155		113		5 TCLCL−95	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		40		23		2 TCLCL−60	ns
TLLDV	ALE Low to Valid Data In									
	8XC51RX		517						8 TCLCL−150	ns
	8XC51RX-24				310		243		8 TCLCL−90	ns
TAVDV	Address to Valid Data In									
	8XC51RX		585						9 TCLCL−165	ns
	8XC51RX-24				360		285		9 TCLCL−90	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	100	200	75	175	3 TCLCL−50	3 TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low									
	8XC51RX	203						4 TCLCL−130		ns
	8XC51RX-24			110		77		4 TCLCL−90		ns
TQVWX	Data Valid before $\overline{WR}$									
	8XC51RX	33						TCLCL−50		ns
	8XC51RX-20			15				TCLCL−35		ns
	8XC51RX-24					12		TCLCL−30		ns
TWHQX	Data Hold after $\overline{WR}$									
	8XC51RX	33						TCLCL−50		ns
	8XC51RX-20			10				TCLCL−40		ns
	8XC51RX-24					7		TCLCL−30		ns
TQVWH	Data Valid to $\overline{WR}$ High									
	8XC51RX	433						7 TCLCL−150		ns
	8XC51RX-24			280		222		7 TCLCL−70		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High									
	8XC51RX	43	123	10	90			TCLCL−40	TCLCL+40	ns
	8XC51RX-24					12	71	TCLCL−30	TCLCL+30	

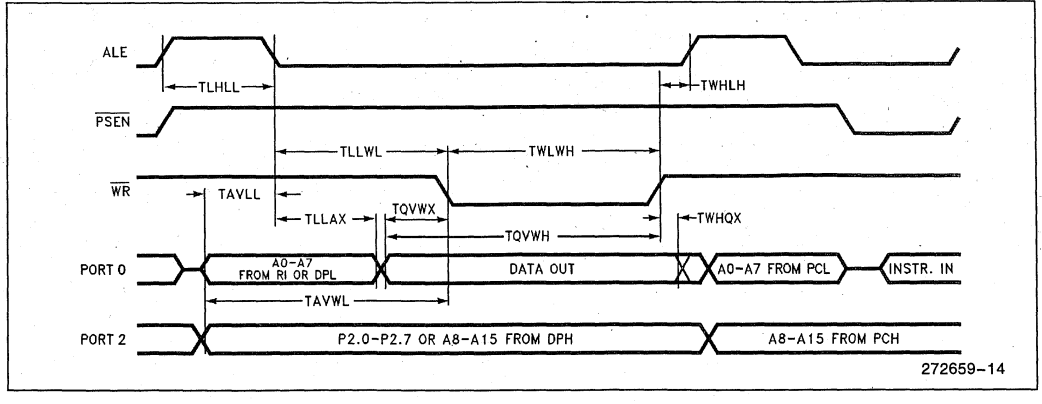
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

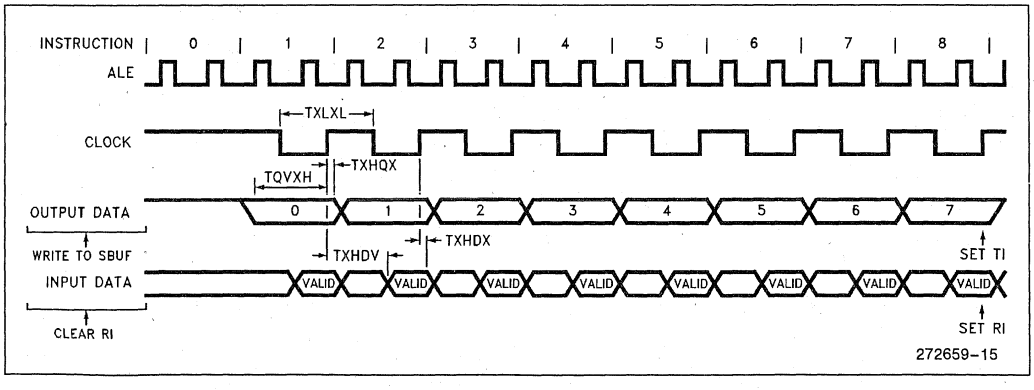


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		20 MHz Oscillator		24 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.600		0.500		12 TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		367			284	10 TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge									
	8XC51RX	50						2 TCLCL − 117		ns
	8XC51RX-24			50		34		2 TCLCL − 50		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		367		284		10 TCLCL − 133	ns

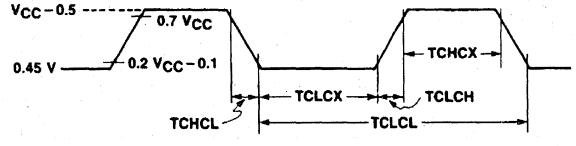
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

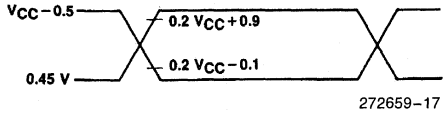
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 8XC51RX 8XC51RX-1 8XC51RX-20 8XC51RX-24	 3.5 3.5 3.5 3.5	 12 16 20 24	MHz
TCHCX	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCX	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
TCLCH	Rise Time 8XC51RX 8XC51RX-24		 20 10	 ns ns
TCHCL	Fall Time20 8XC51RX 8XC51RX-24		 20 10	ns ns ns

EXTERNAL CLOCK DRIVE WAVEFORM



272659-16

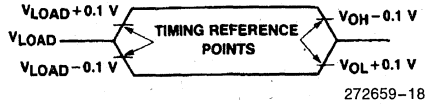
AC TESTING INPUT, OUTPUT WAVEFORMS



272659-17

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



272659-18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} = \pm 20$ mA.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 4. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTES:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5 respectively for A0–A13.

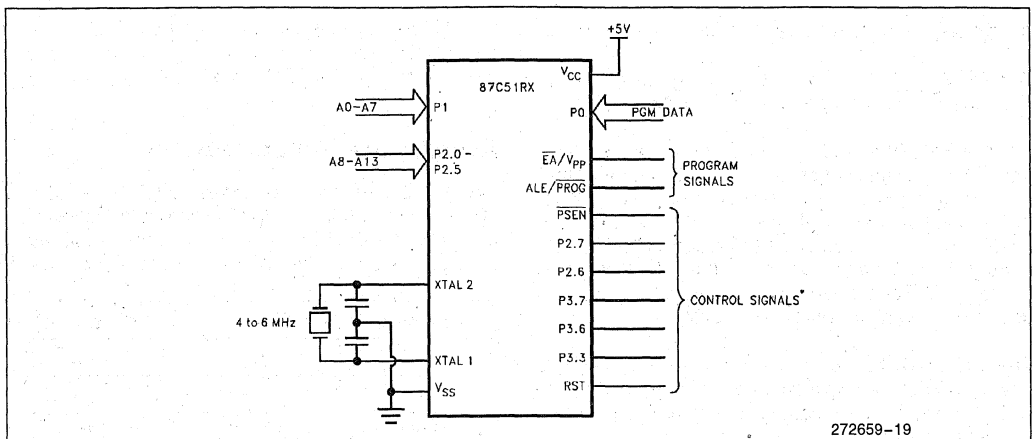
DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$

Table 4. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L



*See Table 4 for proper input on these pins

Figure 10. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 4 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51RX the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C51RX.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

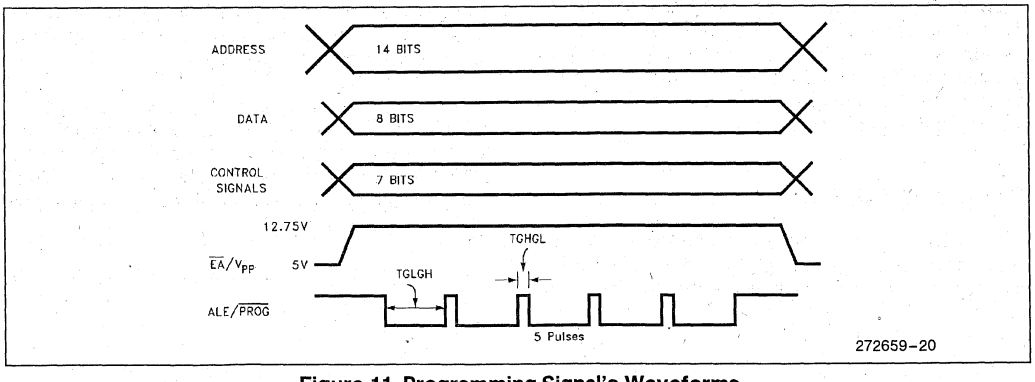


Figure 11. Programming Signal's Waveforms

ROM and EPROM Lock System

The program lock system, when programmed, protects the onboard program against software piracy.

The 83C51RX has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 5. If program protection is desired. the user submits the encryption table with their code. and both the lock-bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51RX has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 5.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 4 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

Program Lock Bits

The 87C51RX has 3 programmable lock bits that when programmed according to Table 5 will provide different levels of protection for the on-chip code and data.

If any program lock bits were programmed, erasing the EPROM will not erase the program lock bits and programming of the EPROM is disabled.

Reading the Signature Bytes

The 8XC51RX has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 4 for Read Signature Byte.

Location	Device	Contents
30H	All	89H
31H	All	58H
60H	87C51RC	C2H
	87C51RB	C1H
	87C51RA	C0H
	83C51RC	42H/C2H
	83C51RB	41H/C1H
	83C51RA	40H/C0H

Erasure Characteristics (Windowed Packages Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

Table 5. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

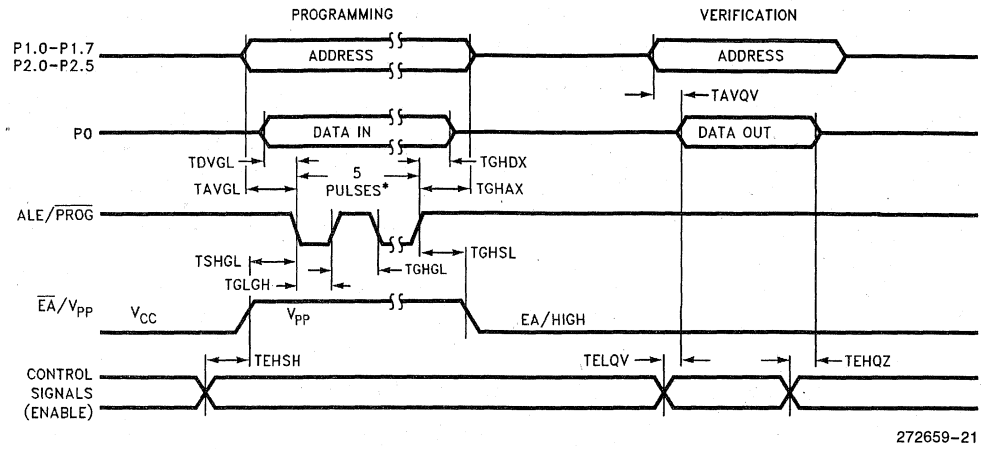
NOTE:
Any other combination of the lock bits is not defined.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

Thermal Impedance

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and applications. See the Intel Packaging Handbook (Order Number 240800) for a description of Intel's thermal impedance test methodology.

Package	θ_{JA}	θ_{JC}	Device
P	45°C/W	16°C/W	All
N	46°C/W	16°C/W	All
S	87°C/W	18°C/W	51RA
	96°C/W	24°C/W	51RB
	90°C/W	22°C/W	51RC

DATA SHEET REVISION HISTORY

Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this datasheet (272659-002) and the previous version (272659-001):

1. ADVANCE INFORMATION datasheet replaces PRODUCT PREVIEW datasheet.
2. I_{TL} (Commercial) changed from -650 µA to -675 µA.
3. I_{TL} (Express) changed from -750 µA to -775 µA.
4. 8XC51RX-24, V_{CC} changed from 5V ±20% to 5V ±10%.
5. Remove all CERDIP package types (prefix D, TD, LD).

INTEL CORPORATION, 2200 Mission College Blvd., Santa Clara, CA 95052; Tel. (408) 765-8080

INTEL CORPORATION (U.K.) Ltd., Swindon, United Kingdom; Tel. (0793) 696 000

INTEL JAPAN k.k., Ibaraki-ken; Tel. 029747-8511

8XC51GB
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Commercial/Express

87C51GB—8 Kbytes OTP/8 Kbytes Internal Program Memory
83C51GB—8 Kbytes Factory Programmable ROM
80C51GB—CPU with RAM and I/O
8XC51GB—3.5 MHz to 12 MHz ±20% V_{CC}
8XC51GB-1—3.5 MHz to 16 MHz ±20% V_{CC}

- 8 Kbytes On-Chip ROM/OTP ROM
- 256 Bytes of On-Chip Data RAM
- Two Programmable Counter Arrays with:
  - — 2 x 5 High Speed Input/Output Channels Compare/Capture
  - — Pulse Width Modulators
  - — Watchdog Timer Capabilities
- Three 16-Bit Timer/Counters with
  - — Four Programmable Modes:
  - — Capture, Baud Rate Generation (Timer 2)
- Dedicated Watchdog Timer
- 8-Bit, 8-Channel A/D with:
  - — Eight 8-Bit Result Registers
  - — Four Programmable Modes
- Programmable Serial Channel with:
  - — Framing Error Detection
  - — Automatic Address Recognition
- Serial Expansion Port
- Programmable Clock Out
- Extended Temperature Range: (−40°C to +85°C)
- 48 Programmable I/O Lines with 40 Schmitt Trigger Inputs
- 15 Interrupt Sources with:
  - — 7 External, 8 Internal Sources
  - — 4 Programmable Priority Levels
- Pre-Determined Port States on Reset
- High Performance CHMOS Process
- TTL and CHMOS Compatible Logic Levels
- Power Saving Modes
- 64K External Data Memory Space
- 64K External Program Memory Space
- Three Level Program Lock System
- ONCE (ON-Circuit Emulation) Mode
- Quick Pulse Programming Algorithm
- MCS® 51 Microcontroller Fully Compatible Instruction Set
- Boolean Processor
- Oscillator Fail Detect
- Available in 68-Pin PLCC

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside in the on-chip ROM. Also, the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 8XC51GB is a single-chip control oriented microcontroller which is fabricated on Intel's CHMOS III-E technology. The 8XC51GB is an enhanced version of the 8XC51FA and uses the same powerful instruction set and architecture as existing MCS 51 microcontroller products. Added features make it an even more powerful microcontroller for applications that require On-Chip A/D, Pulse Width Modulation, High Speed I/O, up/down counting capabilities and memory protection features. It also has a more versatile serial channel that facilitates multi-processor communications.

November 1994

Order Number: 272337-002

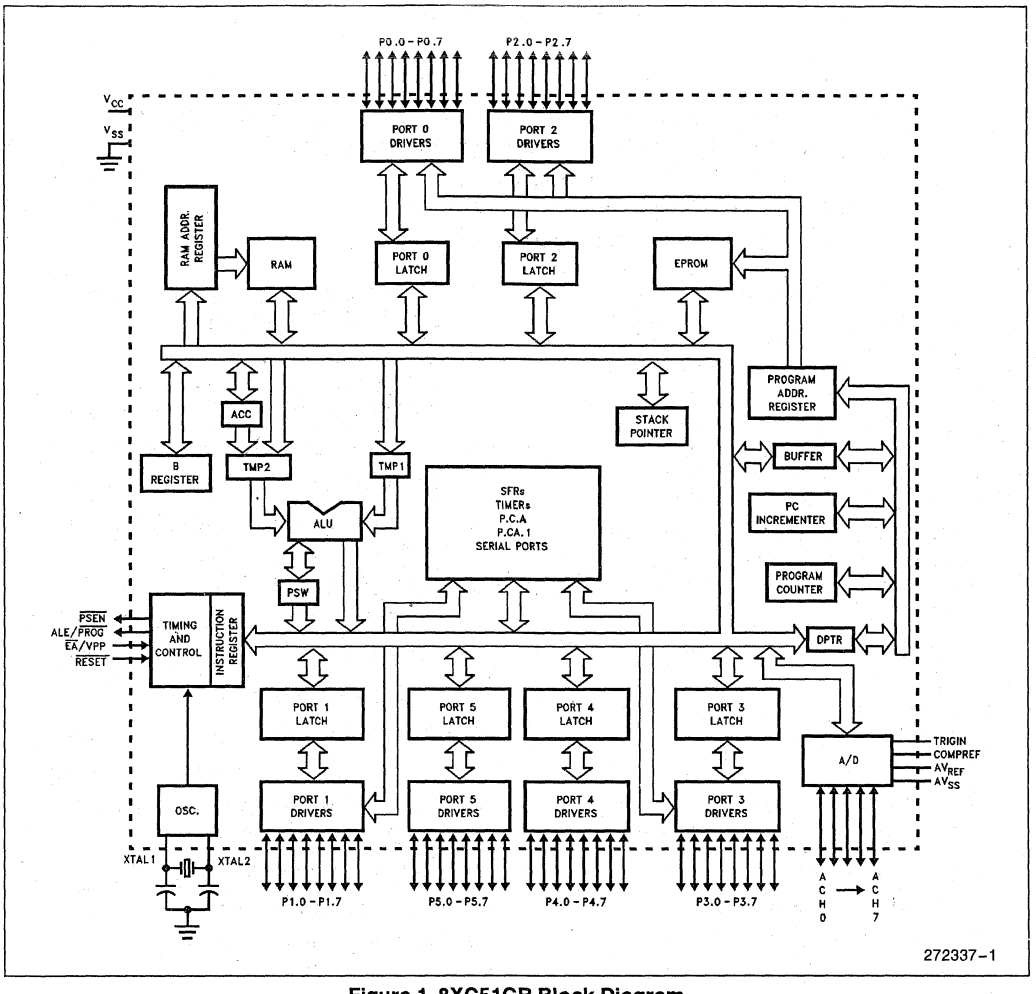


Figure 1. 8XC51GB Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0, a CHMOS III-E process. Additional process and reliability information is available in Intel's Components Quality and Reliability Handbook, Order No. 210997.

PACKAGES

Part	Prefix	Package Type
8XC51GB	N	68-Pin PLCC

PARALLEL I/O PORTS

The 8XC51GB contains six 8-bit parallel I/O ports. All six ports are bidirectional and consist of a latch, an output driver, and an input buffer. Many of the port pins have multiplexed I/O and control functions.

Port Pins as Outputs

Port 0 has open drain outputs when it is not serving as the external data bus. The internal pullup is active only when the pin is outputting a logic 1 during external memory access. An external pullup resistor is required on Port 0 when it is serving as an output port.

Ports 1, 2, 3, 4, and 5 have quasi-bidirectional outputs. A strong pullup provides a fast rise time when the pin is set to a logic 1. This pullup turns on for two oscillator periods to drive the pin high and then turns off. The pin is held high by a weak pullup.

Writing the P0, P1, P2, P3, P4 or P5 Special Function Register sets the corresponding port pins. All six port registers are bit addressable.

Port Pins as Inputs

The pins of all six ports are configured as inputs by writing a logic 1 to them. Since Port 0 is an open drain port, it provides a very high input impedance. Since pins of Port 1, 2, 3, 4 and 5 have weak pullups (which are always on), they source a small current when driven low externally. All ports except Port 0 have Schmitt trigger inputs.

Port States During Reset

Ports 0 and 3 reset asynchronously to a one and Ports 1, 2, 4, and 5 reset to a zero asynchronously.

PIN DESCRIPTIONS

The 8XC51GB will be packaged in the 68-lead PLCC package. Its pin assignment is shown in Figure 2.

V_{CC}: Supply Voltage.

V_{SS}: Circuit Ground.

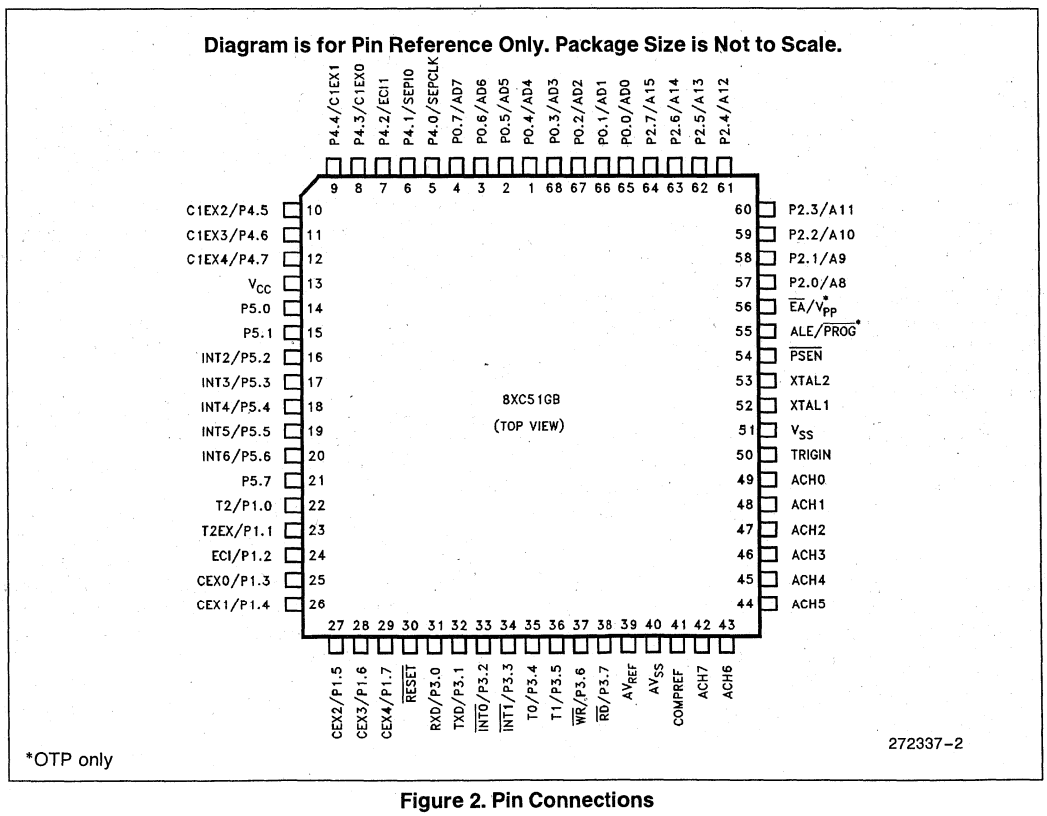


Figure 2. Pin Connections

ALTERNATE PORT FUNCTIONS

Ports 0, 1, 2, 3, 4 and 5 have alternate functions as well as their I/O function as described below.

Port Pin	Alternate Function
P0.0/AD0–P0.7/AD7	Multiplexed Address/Data for External Memory
P1.0/T2	Timer 2 External Clock Input/Clock-Out
P1.1/T2EX	Timer 2 Reload/Capture/Direction Control
P1.2/ECI	PCA External Clock Input
P1.3/CEX0–P1.7/CEX4	PCA Capture Input, Compare/PWM Output
P2.0/A8–P2.7/A15	High Byte of Address for External Memory
P3.0/RXD	Serial Port Input
P3.1/TXD	Serial Port Output
P3.2/$\overline{\text{INT0}}$	External Interrupt 0
P3.3/$\overline{\text{INT1}}$	External Interrupt 1
P3.4/T0	Timer 0 External Clock Input
P3.5/T1	Timer 1 External Clock Input
P3.6/$\overline{\text{WR}}$	Write Strobe for External Memory
P3.7/$\overline{\text{RD}}$	Read Strobe for External Memory
P4.0/SEPCLK	Clock Source for Serial Expansion Port
P4.1/SEPDAT	Data I/O for the Serial Expansion Port
P4.2/ECI1	PCA1 External Clock Input
P4.3/C1EX0–P4.7/C1EX4	PCA1 Capture Input, Compare/PWM Output
P5.2/INT2–P5.6/INT6	External Interrupt INT2–INT6

$\overline{\text{RST}}$: Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a voltage below V_{IL} max voltage is applied, whether the oscillator is running or not. An internal pullup resistor permits a power-on reset with only a capacitor connected to V_{SS}.

ALE/$\overline{\text{PROG}}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{\text{PROG}}$) is also the program pulse input during programming of the 87C51GB.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode and ICE mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{\text{PROG}}$ pin, and the pin will be referred to as the ALE/$\overline{\text{PROG}}$ pin.

$\overline{\text{PSEN}}$: Program Store Enable is the read strobe to external Program Memory.

When the 8XC51GB is executing code from external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external Data Memory.

$\overline{\text{EA}}$/V_{PP}: External Access enable. $\overline{\text{EA}}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 1FFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during programming (OTP only).

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

A/D CONVERTER

The 8XC51GB A/D converter has a resolution of 8 bits and an accuracy of ±1 LSB (±2 LSB for channels 0 and 1). The conversion time for a single channel is 20 μs at a clock frequency of 16 MHz with the sample and hold function included. Independent supply voltages are provided for the A/D. Also, the A/D operates both in Normal Mode or in Idle Mode.

The A/D has 8 analog input pins; ACH0 (A/D CHannel 0) . . . ACH7, 1 reference input pin; COMPREF (COMParison REFerence), 1 control input pin; TRIGIN (TRIGger IN), and 2 power pins; AVREF (Voltage REFerence) and analog ground (ANalog GrouND). In addition, the A/D has 8 conversion result registers; ADRES0 (A/D result for channel 0) . . . ADRES7, 1 comparison result register; ACMP (Analog Comparison), and 1 control register; ACON (A/D Control).

The control bit ACE (A/D Conversion Enable) in ACON controls whether the A/D is in operation or not. ACE = 0 idles the A/D. ACE = 1 enables A/D conversion. The control bit AIM (A/D Input mode) in ACON controls the mode of channel selection. AIM = 0 is the Scan Mode, and AIM = 1 is the Select Mode. The result registers ADRES4 . . . ADRES7 always contain the result of a conversion from the corresponding channels ACH4 . . . CH7. However, the result registers ADRES0 . . . ADRES3 depend on the mode selected. In the scan mode, ADRES0 . . . ADRES3 contain the values from ACH0 . . . ACH3. In the Select Mode, one of the four channels ACH0 . . . ACH3 is converted four times, and the four values are stored sequentially in locations ADRES0 . . . ADRES3. Its channel is selected by bits ACS1 and ACS0 (A/D Channel Select 1 and 0) in ACON.

PROGRAMMABLE COUNTER ARRAYS

The Programmable Counter Arrays (PCA–PCA1) are each made up of a Counter Module and five Register/Comparator Modules as shown below. The 16-bit output of the counter module is available to all five Register/Comparator Modules, providing one common timing reference. Each Register/Comparator Module is associated with a pin of Port 1 or Port 4 and is capable of performing input capture, output compare and pulse width modulation functions. The PCAs are exactly the same in function except for the addition of clock input sources on PCA1.

The PCA Counter and five Register/Comparator Modules each have a status bit in the CCON/C1CON Special Function Registers. These six status bits are set according to the selected modes of operation described below. The CCON/C1CON Register provides a convenient means to determine which of the six PCA/PCA1 interrupts has occurred. The EC Bit in the IE (Interrupt Enable) Special Function Register is a global interrupt enable for the PCA.

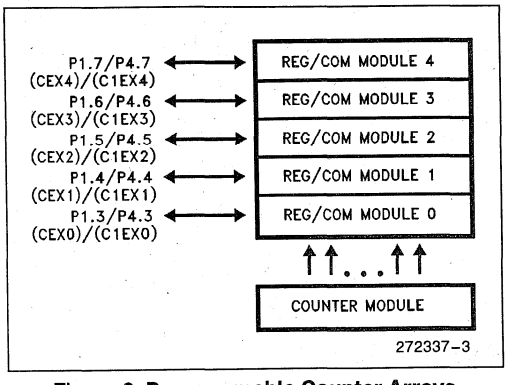
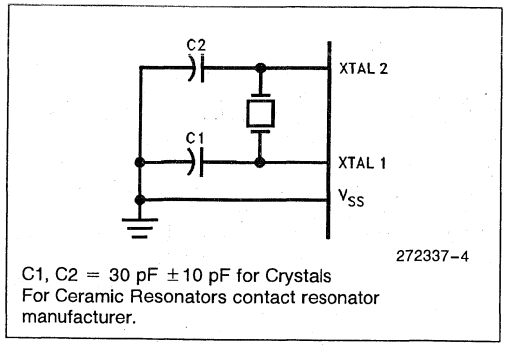


Figure 3. Programmable Counter Arrays

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers," Order No. 230659.

To drive the device from an external clock source, XTAL should be driven, while XTAL2 floats, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators contact resonator manufacturer.

Figure 4. Oscillator Connections

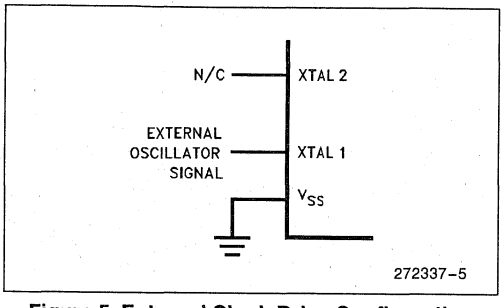


Figure 5. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during idle, peripherals continue to operate, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode. The Watchdog Timer continues to count in Idle Mode and must be serviced to prevent a device RESET while in Idle.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51GB either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt does not redefine the SFR's or change the on-chip RAM. An external interrupt will modify the interrupt associated SFR's in the same way an interrupt will in all other modes. The interrupt must be enabled and configured as level sensitive. To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level. The reset or external interrupt must be held active long enough for the oscillator to restart and stabilize. The Oscillator Fail Detect must be disabled prior to entering Power Down.

DESIGN CONSIDERATIONS

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.
- As $\overline{\text{RESET}}$ rises, the 8XC51GB will remain in reset for up to 5 machine cycles (60 oscillator periods) after $\overline{\text{RESET}}$ reaches V_{IH1}.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I (Order No. 270645), and Application Note AP-252 (Embedded Applications Handbook, Order No. 270648), "Designing with the 80C51BH."

ONCE MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 8XC51GB without removing it from the circuit. The ONCE Mode is invoked by:

1) Pulling ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Holding ALE low as $\overline{RESET}$ is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51GB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Watchdog Timer (WDT)

The 8XC51GB contains a dedicated Watchdog Timer (WDT) to allow recovery from a software or hardware upset. The WDT consists of a 14-bit counter which is cleared on Reset, and subsequently incremented every machine cycle. While the oscillator is running, the WDT will be incrementing and cannot be disabled. The counter may be reset by writing 1EH and E1H in sequence to the WDTRST Special Function Register. If the counter is not reset before it reaches 3FFFH (16383D), the chip will be forced into a reset sequence by the WDT. This works out to 12.28 ms @ 16 MHz. WDTRST is a write only register. The WDT does not force the external reset pin low.

While in Idle mode the WDT continues to count. If the user does not wish to exit Idle with a reset, then the processor must be periodically "woken up" to service the WDT. In Power Down mode, the WDT stops counting and holds its current value.

Serial Expansion Port (SEP)

The Serial Expansion Port is a half-duplex synchronous serial interface with the following features:

Four Clock Frequencies— XTAL/12, 24, 48, 96.

Four Interface Modes— High/Low/Falling/Rising Edges.

Interrupt Driven.

Oscillator Fail Detect (OFD)

The Oscillator Fail Detect circuitry triggers a reset if the oscillator frequency is lower than the OFD trigger frequency. It can be disabled by software by writing E1H followed by 1EH to the OFDCON register. Before going into Power Down Mode, the OFD must be disabled or it will force the GB out of Power Down. The OFD has the following features.

OFD Trigger Frequency: Below 20 KHz, the 8XC51GB will be held in reset. Above 400 KHz, the 8XC51GB will not be held is reset.

Functions in Normal and Idle Modes.

Reactivated by Reset (or External Interrupt Zero/One Pins) after Software Disable.

8XC51GB EXPRESS

The Intel EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C. The 87C51GB EXPRESS is packaged in the 68-lead PLCC package. In order to designate a part as an EXPRESS part, a "T" is added as a prefix to the part number. TN87C51GB denotes an EXPRESS part in a PLCC package.

All AC and DC parameters in this data sheet apply to the EXPRESS devices.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ....0°C to +70°C

Storage Temperature .....−65°C to +150°C

Voltage on EA/V_{PP} Pin to V_{SS} .....0V to +13.0V*

I_{OL} per I/O Pin .....15 mA

Voltage on Any Other Pin to V_{SS} .....−0.5V to +6.5V

Power Dissipation.....1.5W (Based on Package heat transfer limitations, not device power consumption)

*OTP only.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias			
	Commercial	0	+70	°C
	Express	−40	+85	°C
V_{CC}	Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency			
	8XC51GB	3.5	12	MHz
	8XC51GB-1	3.5	16	MHz

DC CHARACTERISTICS (Over Operating Conditions)

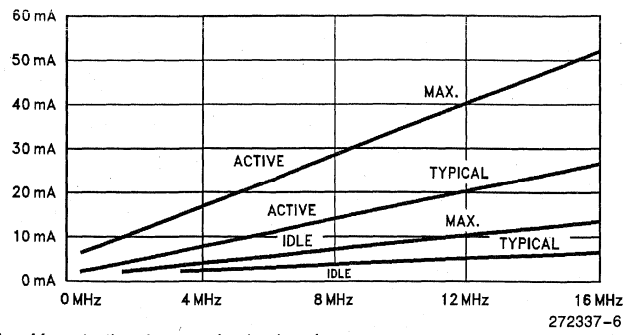
Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (except Port 2 and $\overline{EA}$)	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage (Port 2)	−0.5		0.2 V_{CC} − 0.3	V	
V_{IL2}	Input Low Voltage ($\overline{EA}$)	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (except XTAL1 and $\overline{RST}$)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, $\overline{RST}$)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3, 4 and 5)			0.3	V	I_{OL} = 100 μA (2,3)
				0.45	V	I_{OL} = 1.6 mA (2,3)
				1.0	V	I_{OL} = 3.5 mA (2,3)
V_{OL1}	Output Low Voltage (Port 0, $\overline{PSEN}$, ALE)			0.3	V	I_{OL} = 200 μA (2,3)
				0.45	V	I_{OL} = 3.2 mA (2,3)
				1.0	V	I_{OL} = 7.0 mA (2,3)

DC CHARACTERISTICS (Over Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{OH}	Output High Voltage (Ports 1, 2, 3, 4 and 5, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −10 μA (4)
		V_{CC} − 0.7			V	I_{OH} = −30 μA (4)
		V_{CC} − 1.5			V	I_{OH} = −60 μA (4)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	V_{CC} − 0.3			V	I_{OH} = −200 μA
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, 4, 5)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3, 4, 5)			−650	μA	V_{IN} = 2.0V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
RRST	RST Pullup Resistor	50		300	kΩ	
C_{IO}	Pin Capacitance		10		pF	Freq = 1 MHz T_A = 25°C
I_{PD}	Power Down Current			50	μA	(5)
I_{DL}	Idle Mode Current			18	mA	(5)
I_{CC}	Operating Current @16 MHz			50	mA	(5)
I_{REF}	A/D Converter Reference Current			5	mA	

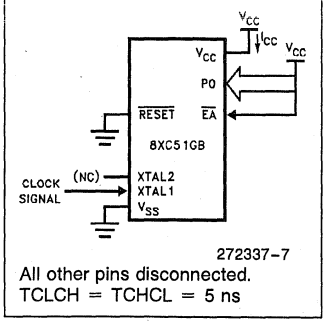
NOTES:

1. Typical values are obtained using V_{CC} = 5.0V, T_A = 25°C, and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per Port Pin: 10 mA
   Maximum I_{OL} per 8-Bit Port—
   Port 0: 26 mA
   Ports 1–5: 15 mA
   Maximum Total I_{OL} for All Outputs Pins: 101 mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
5. See Figures 6–10 for test conditions. Minimum V_{CC} for Power Down is 2V.



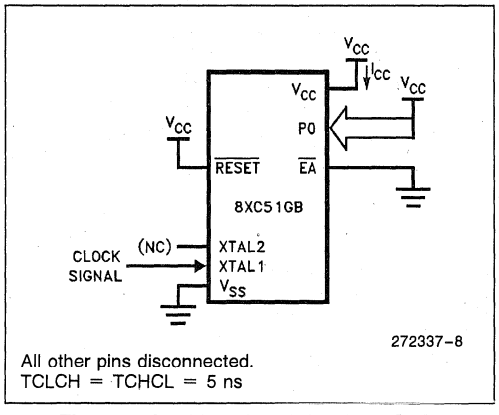
I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (Osc Freq × 3) + 4
Idle Mode
I_{CC} Max = (Osc Freq × 0.5) + 4
Where Osc Freq is in MHz, I_{CC} is in mA. $T_{CLCH} = T_{CHCL} = 5$ ns

Figure 6. I_{CC} vs Frequency



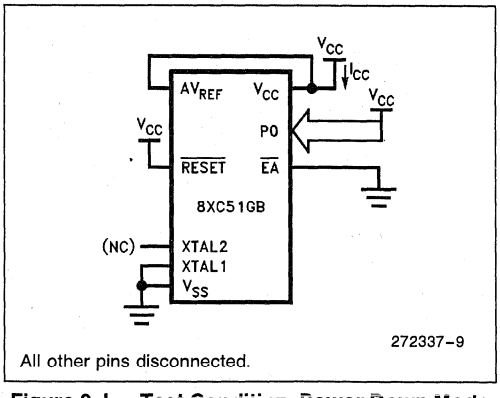
All other pins disconnected.
TCLCH = TCHCL = 5 ns

Figure 7. I_{CC} Test Condition, Active Mode



All other pins disconnected.
TCLCH = TCHCL = 5 ns

Figure 8. I_{CC} Test Condition Idle Mode



All other pins disconnected.

Figure 9. I_{CC} Test Condition, Power Down Mode
V_{CC} = 2.0V to 5.5V

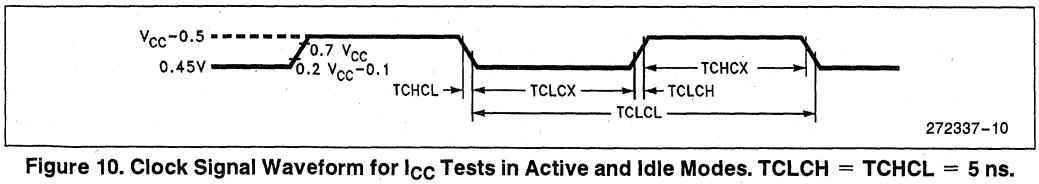


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for:

A: Address
C: Clock
D: Input Data
H: Logic Level HIGH
I: Instruction (Program Memory Contents)
L: Logic Level LOW, or ALE
P: $\overline{PSEN}$
Q: Output Data
R: $\overline{RD}$ Signal
T: Time
V: Valid
W: $\overline{WR}$ Signal
X: No Longer a Valid Logic Level
Z: Float

For Example:

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{PSEN}$ Low

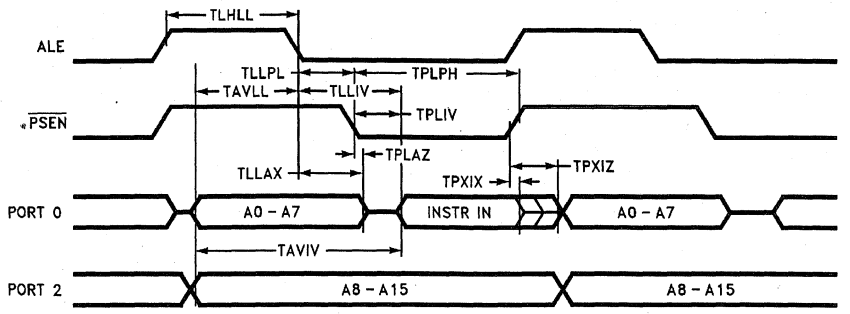
AC SPECIFICATIONS

Over Operating Conditions, Load Capacitance on Port 0, ALE, and $\overline{PSEN}$ = 100 pF, Load Capacitance on all other outputs = 80 pF

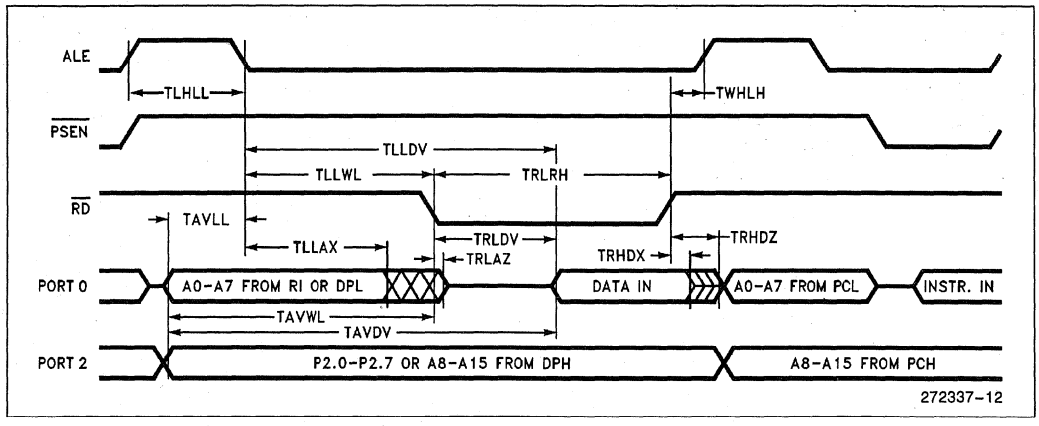
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc.		Variable Osc.		Units
		Min	Max	Min	Max	
1/TCLCL	Osc. Freq.			3.5	16	MHz
TLHLL	ALE Pulse Width	127		2TCLCL − 40		ns
TAVLL	ADDR Valid to ALE Low	43		TCLCL − 40		ns
TLLAX	ADDR Hold after ALE Low	53		TCLCL − 30		ns
TLLIV	ALE Low to Valid Inst. IN		234		4TCLCL − 100	ns
TLLPL	ALE LOW to $\overline{PSEN}$ LOW	53		TCLCL − 30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL − 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		145		3TCLCL − 105	ns
TPXIX	Input Instr. Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr. Float after $\overline{PSEN}$		59		TCLCL − 25	ns
TAVIV	ADDR to Valid Instr. In		312		5TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to ADDR Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL − 165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		107		2TCLCL − 60	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL − 150	ns
TAVDV	ADDR to Valid Data In		585		9TCLCL − 165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL − 50	3TCLCL + 50	ns
TAVWL	ADDR Valid to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL − 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL − 50		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL − 50		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7 TCLCL − 150		ns
TRLAZ	$\overline{RD}$ Low to Addr Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL − 40	TCLCL + 40	ns

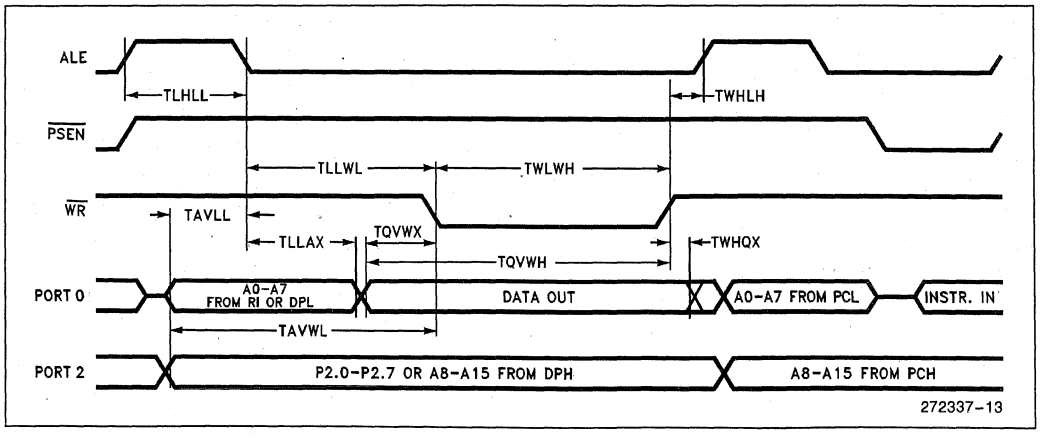
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

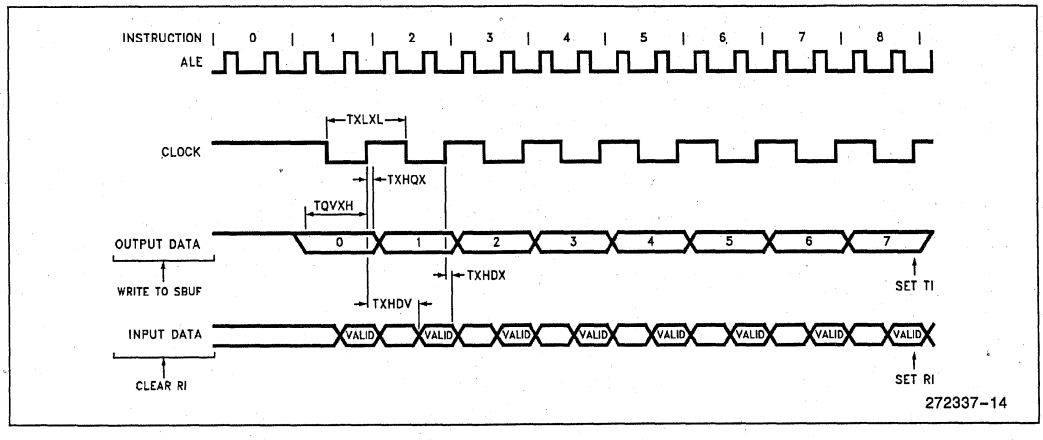


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions, Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL − 117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL − 133	ns

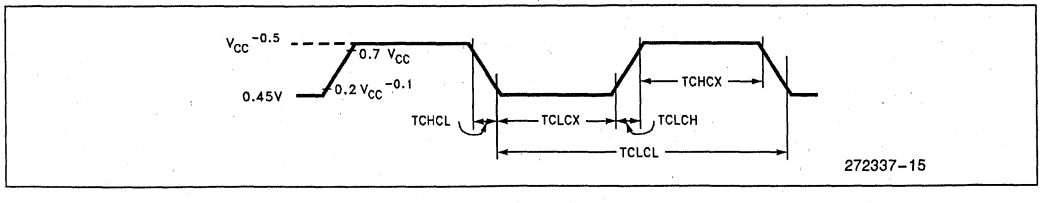
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM

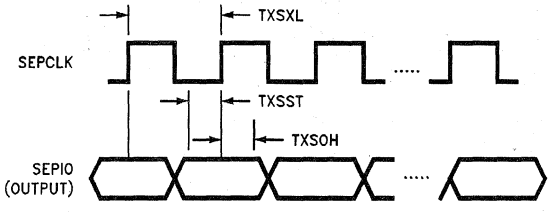


SEP AC TIMING SPECIFICATIONS

Test Conditions: Over Operating Conditions, Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXSXL	SEPCLK Cycle Time	1		12 TCLCL		μs
TXSST	Output Data Setup to SEPCLK	435		6 TCLCL − 65		ns
TXSOH	Output Data Hold after SEPCLK	445		6 TCLCL − 55		ns
TXSIH	Input Data Hold after SEPCLK Sampling Edge	210		2 TCLCL + 43		ns
TXSDV	Input Data Valid to SEPCLK Sampling Edge		947		12 TCLCL − 53	ns

SEP Waveform (SEPS1 = 0; SEPS0 = 0; CLKPOL = 0; CLKPH = 0)



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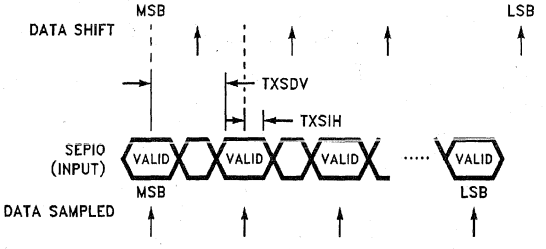
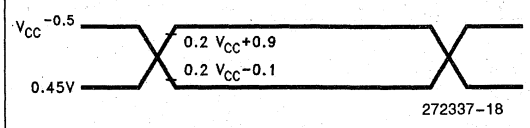


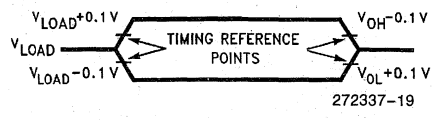
272337-17

AC TESTING INPUT, OUTPUT WAVEFORMS



AC inputs during testing are driven at V_{CC} − 0.5V for a Logic "1" and 0.5V for a Logic "0". Timing measurements are made at V_{IH} for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

A TO D CHARACTERISTICS

The absolute conversion accuracy is dependent on the accuracy of AV_{REF}. The specifications given below assume adherence to the Operating Conditions section of this data sheet. Testing is done at AV_{REF} = 5.12V, and V_{CC} = 5.0V.

OPERATING CONDITIONS

V_{CC} ..... 4.0V to 6.0V
AV_{REF} ..... 4.5V to 5.5V
V_{SS}, AV_{SS} 0V
ACH0–7 ..... AV_{SS} to V_{REF}
T_A ..... 0°C to +70°C Ambient
FOSC (STD Version) ..... 3.5 MHz to 12 MHz
FOSC (-1 Version) ..... 3.5 MHz to 16 MHz

A/D CONVERTER SPECIFICATIONS T_A = 0°C to +70°C

Parameter	Min	Typ*	Max	Units**	Notes
Resolution	256 8		256 8	Levels Bits	
Absolute Error (Ch 2–7)	0		±1	LSB	
Absolute Error (Ch 0 and 1)	0		±2	LSB	
Full Scale Error		±1		LSB	
Zero Offset Error		±1		LSB	
Non-Linearity	0		±1	LSB	
Differential Non-Linearity	0		±1	LSB	
Channel-to-Channel Matching	0		±1	LSB	
Repeatability		±0.25		LSB	

A/D CONVERTER SPECIFICATIONS T_A = 0°C to +70°C (Continued)

Parameter	Min	Typ*	Max	Units**	Notes
Temperature Coefficients:					
Offset		0.003		LSB/°C	
Full Scale		0.003		LSB/°C	
Differential Non-Linearity		0.003		LSB/°C	
Input Capacitance		3		pF	
Off Isolation	−60			dB	(8, 9)
Feedthrough		−60		dB	(8)
V_{CC} Power Supply Rejection		−60		dB	(8)
Input Resistance to Sample-and-Hold Capacitor	750		1.2K	Ω	
DC Input Leakage	0		3.0	μA	

NOTES:
*These values are expected for most parts at 25°C
**AN "LSB" as used here, has a value of approximately 20 mV.
8. DC to 100 KHz
9. Multiplexer Break-Before-Make Guaranteed.
10. There is no indication when a single A/D conversion is complete. Please refer to the 8XC51GB Hardware Description on how to read a single A/D conversion.
11. T_{CY} = 12 TCLCL

A/D Conversion Time		Notes
Per Channel	26 T_{CY}	(10, 11)
8 Conversions	208 T_{CY}	(11)

PROGRAMMING THE OTP

The part must be running with a 4 MHz to 6 MHz oscillator. The address of a location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

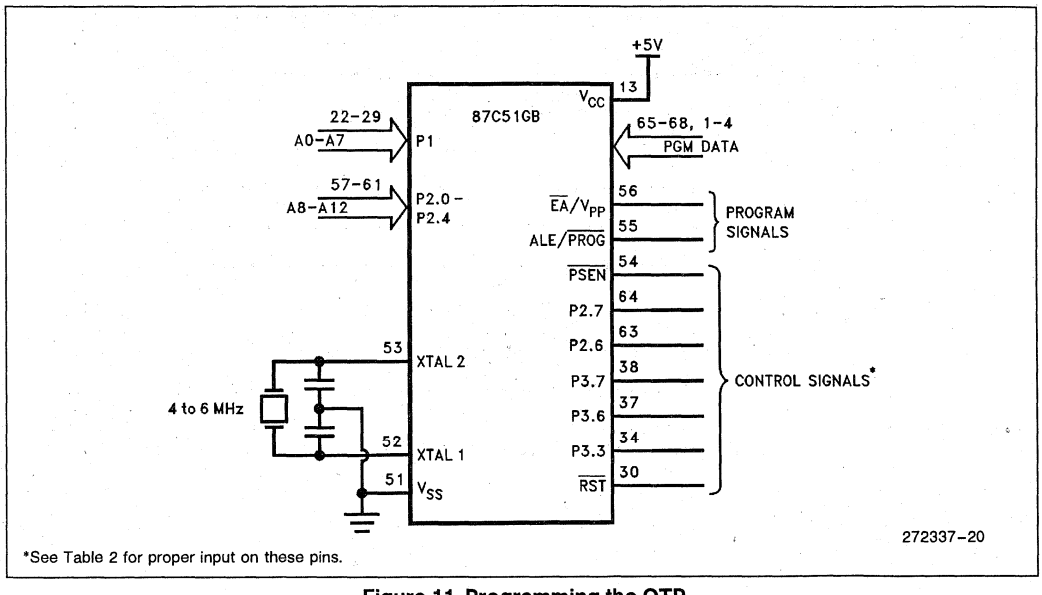
DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.4, respectively for A0–A12.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: $\overline{RST}$, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$



*See Table 2 for proper input on these pins.

Figure 11. Programming the OTP

Table 2. OTP Programming Modes

Mode		$\overline{RST}$	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		L	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		L	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		L	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	L	L	⊓	12.75V	H	H	H	H	H
	Bit 2	L	L	⊓	12.75V	H	H	H	L	L
	Bit 3	L	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		L	H	H	H	L	L	L	L	L

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 11 and 12 for address, data, and control signals set up. To program the 87C51GB the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the OTP array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte that is programmed, or after a block of bytes that is programmed. In either case a complete verify of the array will ensure that it has been programmed correctly.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled. Refer to the Program Lock section in this data sheet.

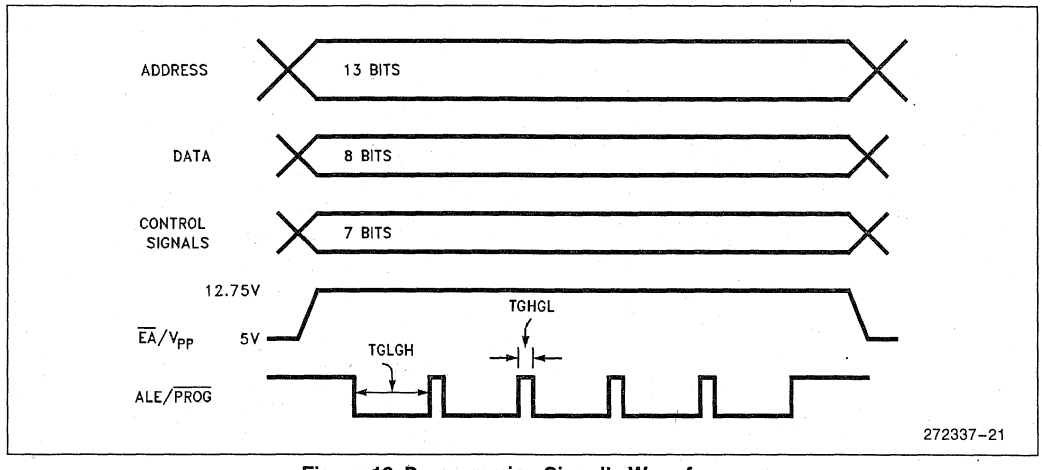


Figure 12. Programming Signal's Waveforms

ROM and EPROM Lock System

The 87C51GB and the 83C51GB program lock systems, when programmed, protect the on-board program against software piracy.

The 83C51GB has a one-level program lock system and a 64-byte encryption table. See line 2 of Table 3. If program protection is desired, the user submits the encryption table with their code, and both the lock bit and encryption array are programmed by the factory. The encryption array is not available without the lock bit. For the lock bit to be programmed, the user must submit an encryption table.

The 87C51GB has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user programmable. See Table 3.

Encryption Array

Within the programmable array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 2.

When using the encryption array feature, one important factor needs to be considered. If a code byte has the value 0FFH, verification of the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason it is strongly recommended that all unused code bytes be programmed with some value other than 0FFH, and not all of them the same value. This practice will ensure the maximum possible program protection.

Program Lock Bits

The 87C51GB has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code **and data.** The 83C51GB has 1 program lock bit. See line 2 of Table 3.

Reading the Signature Bytes

The 8XC51GB has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents	
	87C51GB	83C51GB
30H	89H	89H
31H	58H	58H
60H	EBH	EBH/6BH

Table 3. Program Lock Bits and the Features

*Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed).
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

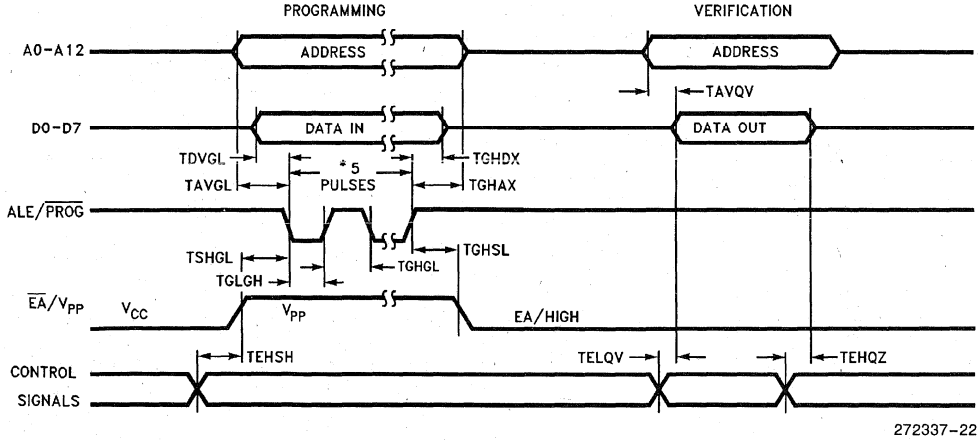
*Any other combination of lock bits is not defined.

OTP PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ± 20%; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

PROGRAMMING AND VERIFICATION WAVEFORMS



272337-22

*25 Pulses for Encryption Table and Lock Bits.

A/D Glossary of Terms

Absolute Error—The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

Actual Characteristic—The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An actual characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversions under the same conditions.

Break-Before-Make—The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected (e.g., the converter will not short inputs together).

Channel-to-Channel Matching—The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

Characteristic—A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

Code—The digital value output by the converter.

Code Center—The voltage corresponding to the midpoint between two adjacent code transitions.

Code Transition—The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

Code Width—The voltage corresponding to the difference between two adjacent code transitions.

Crosstalk—See "Off-Isolation".

DC Input Leakage—Leakage current to ground from an analog input pin.

Differential Non-Linearity—The difference between the ideal and actual code widths of the terminal based characteristic.

Feedthrough—Attenuation of a voltage applied on the selected channel of the A/D Converter after the sample window closes.

Full Scale Error—The difference between the expected and actual input voltage corresponding to the full scale code transition.

Ideal Characteristic—A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

Input Resistance—The effective series resistance from the analog input pin to the sample capacitor.

LSB—Least Significant Bit—The voltage corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For an 8-bit converter with a reference voltage of 5.12V, one LSB is 20 mV. Note that this is different than digital LSBs since an uncertainty of two LSBs, when referring to an A/D converter, equals 40 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 80 mV).

Monotonic—The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

No Missed Codes—For each and every output code, there exists a unique input voltage range which produces that code only.

Non-Linearity—The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristic.

Off-Isolation—Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

Repeatability—The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

Resolution—The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

Sample Delay—The delay from receiving the start conversion signal to when the sample window opens.

Sample Delay Uncertainty—The variation in the sample delay.

Sample Time—The time that the sample window is open.

Sample Time Uncertainty—The variation in the sample time.

Sample Window—Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

Successive Approximation—An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

Temperature Coefficients—Change in the stated variable per degree centrigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of temperature drift.

Terminal Based Characteristic—An actual characteristic which has been rotated and translated to remove zero offset and full scale error.

V_{CC} Rejection—Attenuation of noise on the V_{CC} line to the A/D converter.

Zero Offset—The difference between the expected and actual input voltage corresponding to the first code transition.

DATA SHEET REVISION SUMMARY

The following differences exist between this datasheet and the previous version (270869-003):

1. Merged 87C51GB Express (270889-001).
2. New order number 272337-001.

The following differences exist between the 270869-003 data sheet and the previous version (270869-002):

1. Changed data sheet status from "Advance Information" to "Preliminary" and updated associated notices.
2. Added 83C51GB throughout.
3. Added Package and Process Information.
4. Clarified ±2 LSB accuracy for channels 0 and 1 in A/D Converter Section.
5. Added "ROM and EPROM Lock System" section and added 83C51GB to "Program Lock Bits" section.
6. Modified Signature Bytes Table.

The following differences exist between the 270869-002 data sheet and the previous version (270869-001):

1. Changed data sheet status from "Product Preview" to "Advance Information" and updated associated notices.
2. Asynchronous port reset was added to $\overline{\text{RESET}}$ pin description.
3. ALE disable paragraph was added to ALE pin description.
4. C_1, C_2 guidelines clarified in Figure 4.
5. Operating Conditions heading was added.
6. Maximum I_{OL} per I/O pin was added to Absolute Maximum Ratings.
7. VT_+, VT_-, V_{HYS}, V_{OL2}, and V_{TL} removed.
8. V_{OL} value for ALE included with V_{OL1}.
9. V_{IL1} and V_{IL2} added.
10. RRST minimum changed from 40K to 50K. RRST maximum changed from 225K to 300K.
11. I_{PD} maximum changed from 200 μA to 50 μA.
12. I_{DL} maximum changed from 15 mA to 18 mA.
13. Typical values for I_{PD}, I_{DL}, I_{CC}, and I_{REF} removed.
14. Note 3 (page 9) was reworded.
15. SEP AC Timings added.
16. A/D Absolute Error for Channels 0 and 1 changed to ±2 LSB.
17. T_{CY} clarified.
18. Encryption array paragraph was added.
19. Corrected pin numbers on Figure 11 to reflect PLCC package.

8XC51SL/LOW VOLTAGE 8XC51SL KEYBOARD CONTROLLER

80C51SL — CPU with RAM and I/O; V_{CC} = 5V ±10%

81C51SL — 16K ROM Preprogrammed with SystemSoft Keyboard Controller and Scanner Firmware. V_{CC} = 5V ±10%.

83C51SL — 16K Factory Programmed ROM. V_{CC} = 5V ±10%.

87C51SL — 16K OTP ROM. V_{CC} = 5V ±10%.

Low Voltage 80C51SL—CPU with RAM and I/O; V_{CC} = 3.3V ±0.3V

Low Voltage 81C51SL— 16K ROM Preprogrammed with SystemSoft Keyboard Controller and Scanner Firmware. V_{CC} = 3.3V ±0.3V.

Low Voltage 83C51SL— 16K Factory Programmed ROM. V_{CC} = 3.3V ±0.3V.

Low Voltage 87C51SL— 16K OTP ROM. V_{CC} = 3.3V ±0.3V.

- **Proliferation of 8051 Architecture**
- **Complete 8042 Keyboard Control Functionality**
- **8042 Style Host Interface**
- **Optional Hardware Speedup of GATEA20 and RCL**
- **Local 16 x 8 Keyboard Switch Matrix Support**
- **Two Industry Standard Serial Keyboard Interfaces; Supported via Four High Drive Outputs**
- **5 LED Drivers**
- **Low Power CHMOS Technology**
- **4-Channel, 8-Bit A/D**
- **Interface for up to 32 Kbytes of External Memory**
- **Slew Rate Controlled I/O Buffers Used to Minimize Noise**
- **256 Bytes Data RAM**
- **Three Multifunction I/O Ports**
- **10 Interrupt Sources with 6 User-Definable External Interrupts**
- **2 MHz–16 MHz Clock Frequency**
- **100-Pin PQFP (8XC51SL)**
  100-Pin SQFP (Low Voltage 8XC51SL)

The 8XC51SL, based on Intel's industry-standard MCS® 51 microcontroller family, is designed for keyboard control in laptop and notebook PCs. The highly integrated keyboard controller incorporates an 8042-style UPI host interface with expanded memory, keyboard scan, and power management. The 8XC51SL supports both serial and scanned keyboard interfaces and is available in pre-programmed versions to reduce time to market. The Low Voltage 8XC51SL is the 3.3V version optimized for even further power savings. Throughout the remainder of this document, both devices will generally be referred to as 51SL.

The 8XC51SL is a pin-for-pin compatible replacement for the 8XC51SL-BG. It does, however have some additional functionality. Those additional functions are as follows:

1. 16K OTP ROM: The 8XC51SL-BG had only 8K of ROM.
2. New Register Set: The 8XC51SL adds a second set of host interface registers available for use in supporting power management. This required an additional address line (A1) for decoding. To accommodate this, one V_{CC} pin was removed. However, in order to maintain compatibility with the -BG version, an enable bit for this new register set was added in configuration register 1. This allows the 8XC51SL to be drop in compatible to existing 8XC51SL-BG designs; no software modifications required.

NOTE:
The changes made to the V_{CC} pins require that all three V_{CC} pins be properly connected. Failing to do so could result in high leakage current and possible damage to the device.

November 1994

Order Number: 272271-002

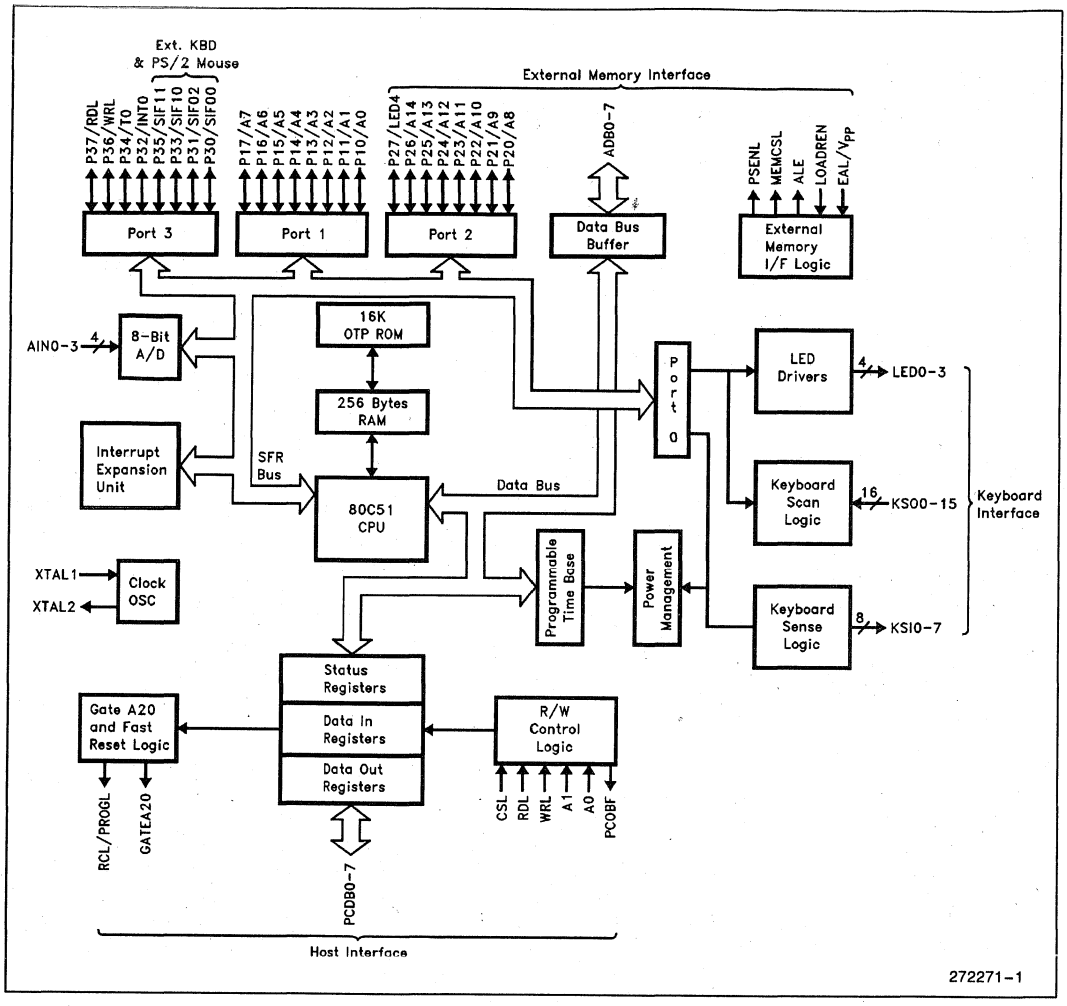


Figure 1. Block Diagram

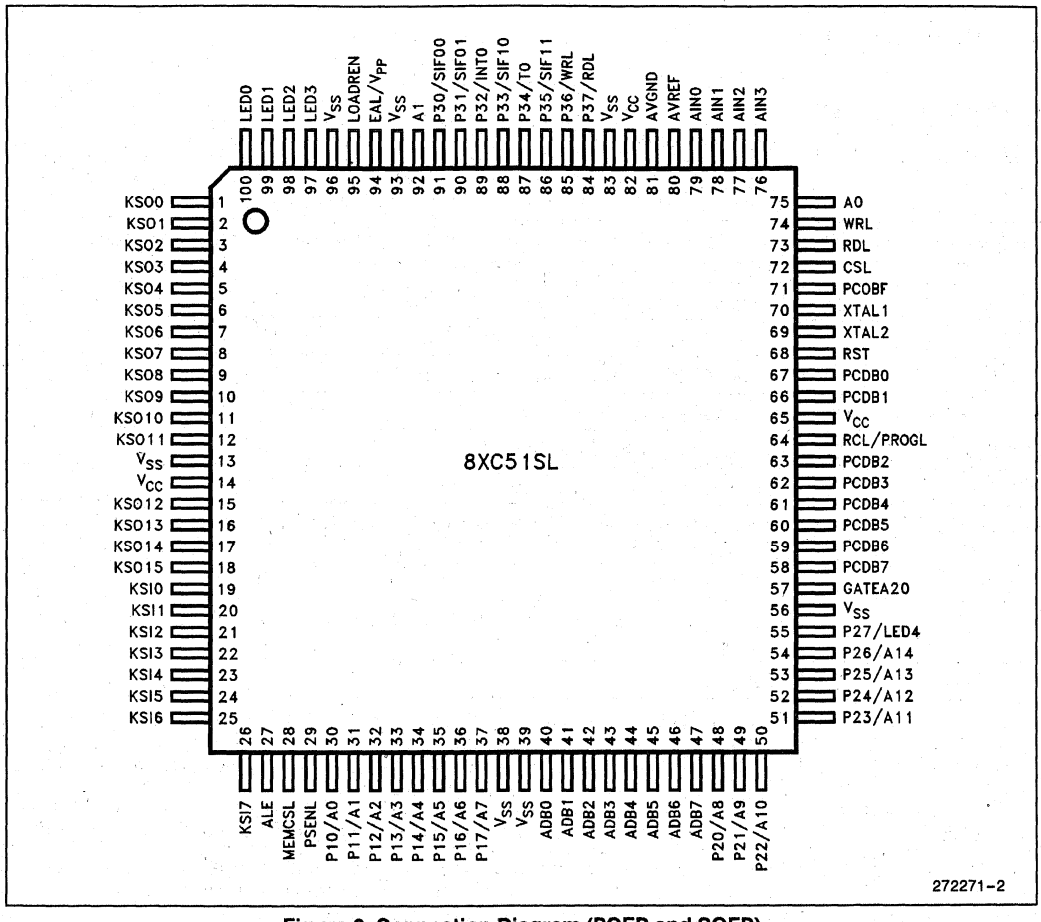


Figure 2. Connection Diagram (PQFP and SQFP)

PACKAGES

Part	Prefix	Suffix	Package Type
8XC51SL	KU	AH	100-Pin PQFP
Low Voltage 8XC51SL	SB	AL	100-Pin SQFP

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Symbol	Type	Description
V_{SS}		Circuit ground potential.
V_{CC}		Supply voltage during normal, Idle, and Power-Down operation; nominally +5V ±10% for 8XC51SL, +3.3V ± 0.3V for Low Voltage 8XC51SL.
PCDB0–7	I/O	Host interface data bus. An 8-bit bidirectional port for data transfers between the host processor and the keyboard controller.
WRL	I	The active-low, host-interface write signal.
RDL	I	The active-low, host-interface read signal.
CSL	I	The active-low, host-interface chip select.
A0–A1	I	Host-Interface Address select inputs.
PCOBF	O	The active-high, host-interface Output Buffer Full interrupt.
GATEA20	O	Gate A20 control signal output.
RCL/PROGL	O	Host reset—active low. This pin is also the program pulse input during EPROM programming.
LED0–3	O	LED output drivers.
KSI0–7	I	Keyboard input scan lines (input Port 0). Schmitt inputs with 5K–20K pull-up resistors.
KSO0–15	O	Keyboard output scan lines.
PORT 1 P10/A0– P17/A7	I/O	Port 1 is a general-purpose, 8-bit bidirectional port with internal pull-ups. It also supports the following user-selectable functions: P10–P16 are available for connection to dedicated keyboard inputs. A0–A7 output the low-order address byte (refer to LOADREN signal).
LOADREN	I	Low address enable. When set high, address bits A0–A7 are output on P10–P17.
PORT2 P20–6/A8–14 P27/LED4	I/O	Port 2 is a general-purpose, 8-bit bidirectional port with internal pull-ups on P20–6/A8–14. It also supports the following user-selectable functions: P20–6/A8–14 output the high-order address byte. P27/LED4 is available as a fifth LED output driver (by writing to the port bit 7).
PORT 3 P30/SIF00 P31/SIF01 P32/INT0 P33/SIF10 P34/T0 P35/SIF11 P36/WRL P37/RDL	I/O	Port 3 is a general-purpose, 8-bit bidirectional port. P32/INT0, P34/T0, P36/WRL, and P37/RDL have internal pull-ups. P30/SIF00, P31/SIF01, P33/SIF10, and P35/SIF11 are high-drive open-drain outputs. It also supports the following user-selectable functions: A high-drive, open-drain output to support an external serial keyboard interface (typically CLK); RXD (8051 UART serial input port); SIF0INTL (serial interface interrupt 0). A high-drive, open-drain output to support an external serial keyboard interface (typically DATA); TXD (8051 UART serial output port). INT0L (external interrupt 0). A high-drive, open-drain output to support an external serial keyboard interface (typically mouse CLK); SIF1INTL (external interrupt 1). AUXOBF1 (output buffer full—mouse support); T0 (Timer/Counter 0 external input). A high-drive, open-drain output to support an external serial keyboard interface (typically mouse DATA); T1 (Timer/Counter 1 external input). WRL (external data memory write strobe); inactive at addresses 7FF0–7FFFH. AUXOBF2 (output buffer full interrupt); INT2L (external interrupt); RDL (external data memory read strobe); inactive at addresses 7FF0–FFFFH.

PIN DESCRIPTIONS (Continued)

Table 1. Pin Descriptions (Continued)

Symbol	Type	Description
XTAL1	I	Input to the on-chip oscillator.
XTAL2	O	Output from the on-chip oscillator.
AVGND		Analog ground potential.
AVREF		Analog supply voltage; nominally +5V ±10% for 8XC51SL, +3.3V ±0.3V for Low Voltage 8XC51SL.
AIN0–3	I	A/D Analog input channels.
ADB0–7	I/O	External address/data bus. Multiplexes the low-address byte and data during external memory accesses.
EAL/V_{PP}	I	External address input. When held high, the 51SL CPU executes out of internal Program Memory unless the program counter exceeds 3FFFH. When held low, the 51SL CPU always executes out of external memory. EAL is latched on the falling edge of RST. This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.
ALE	O	Address Latch Enable output pulse latches the low address byte during external memory access. ALE is output at a constant rate of 1/6 the oscillator frequency, whether or not there are accesses to external memory. One ALE pulse is skipped during the execution of a MOVX instruction. ALE is disabled during Idle mode and can also be disabled via Configuration register 1 control.
PSENL	O	Program Store Enable is the read strobe to external program memory. PSENL is qualified with RDL and A15 for use with an external Flash memory. PSENL is not active when the device executes out of internal program memory.
MEMCSL	I/O	External Memory Chip Select for code space address 4000H and above, when EAL is inactive (i.e., high). For EAL low, MEMCSL is active. Goes inactive during Idle mode and Power-Down mode. If external memory interfacing is not required, MEMCSL can be configured as a general purpose I/O (controlled via Configuration register 1).
RST	I	Resets the keyboard controller. Hold RST high for two machine cycles.

8XC51SL/LOW VOLTAGE 8XC51SL PIN CHARACTERISTICS

Table 2. Pin Characteristics

Pin No.	Pin Name	Type	Term	Reset	PD Mode
1	KSO0	O	OD	TRI	HOLD
2	KSO1	O	OD	TRI	HOLD
3	KSO2	O	OD	TRI	HOLD
4	KSO3	O	OD	TRI	HOLD
5	KSO4	O	OD	TRI	HOLD
6	KSO5	O	OD	TRI	HOLD
7	KSO6	O	OD	TRI	HOLD
8	KSO7	O	OD	TRI	HOLD
9	KSO8	O	OD	TRI	HOLD
10	KSO9	O	OD	TRI	HOLD
11	KSO10	O	OD	TRI	HOLD
12	KSO11	O	OD	TRI	HOLD
13	V_{SS}				
14	V_{CC}				
15	KSO12	O	OD	TRI	HOLD
16	KSO13	O	OD	TRI	HOLD
17	KSO14	O	OD	TRI	HOLD
18	KSO15	O	OD	L	HOLD
19	KSI0	I	5K–20K PU		NC
20	KSI1	I	5K–20K PU		NC
21	KSI2	I	5K–20K PU		NC
22	KSI3	I	5K–20K PU		NC
23	KSI4	I	5K–20K PU		NC
24	KSI5	I	5K–20K PU		NC
25	KSI6	I	5K–20K PU		NC
26	KSI7	I	5K–20K PU		NC
27	ALE	O		L	L
28	MEMCSL	O		L (EAL = 0)	H
29	PSENL	O		L	L
30	P10/A0	I/O	PU	WH	HOLD
31	P11/A1	I/O	PU	WH	HOLD
32	P12/A2	I/O	PU	WH	HOLD
33	P13/A3	I/O	PU	WH	HOLD
34	P14/A4	I/O	PU	WH	HOLD
35	P15/A5	I/O	PU	WH	HOLD
36	P16/A6	I/O	PU	WH	HOLD
37	P17/A7	I/O	PU	WH	HOLD

8XC51SL/LOW VOLTAGE 8XC51SL PIN CHARACTERISTICS (Continued)

Table 2. Pin Characteristics (Continued)

Pin No.	Pin Name	Type	Term	Reset	PD Mode
38	V_{SS}				
39	V_{SS}				
40	ADB0	I/O		TRI	TRI
41	ADB1	I/O		TRI	TRI
42	ADB2	I/O		TRI	TRI
43	ADB3	I/O		TRI	TRI
44	ADB4	I/O		TRI	TRI
45	ADB5	I/O		TRI	TRI
46	ADB6	I/O		TRI	TRI
47	ADB7	I/O		TRI	TRI
48	P20/A8	I/O	PU	WH	HOLD
49	P21/A9	I/O	PU	WH	HOLD
50	P22/A10	I/O	PU	WH	HOLD
51	P23/A11	I/O	PU	WH	HOLD
52	P24/A12	I/O	PU	WH	HOLD
53	P25/A13	I/O	PU	WH	HOLD
54	P26/A14	I/O	PU	WH	HOLD
55	P27/LED4	I/O	OD	TRI	HOLD
56	V_{SS}				
57	GATEA20	O		WH	HOLD
58	PCDB7	I/O		TRI	TRI
59	PCDB6	I/O		TRI	TRI
60	PCDB5	I/O		TRI	TRI
61	PCDB4	I/O		TRI	TRI
62	PCDB3	I/O		TRI	TRI
63	PCDB2	I/O		TRI	TRI
64	RCL/PROGL	O		WH	HOLD
65	V_{CC}				
66	PCDB1	I/O		TRI	TRI
67	PCDB0	I/O		TRI	TRI
68	RST	I			
69	XTAL2	O			H
70	XTAL1	I			
71	PCOBF	O		L	HOLD
72	CSL	I			
73	RDL	I			
74	WRL	I			

8XC51SL/LOW VOLTAGE 8XC51SL PIN CHARACTERISTICS (Continued)

Table 2. Pin Characteristics (Continued)

Pin No.	Pin Name	Type	Term	Reset	PD Mode
75	A0	I			
76	AIN3	I			
77	AIN2	I			
78	AIN1	I			
79	AIN0	I			
80	AVREF				
81	AVGND				
82	V_{CC}				
83	V_{SS}				
84	P37/RDL	I/O	PU	WH	HOLD
85	P36/WRL	I/O	PU	WH	HOLD
86	P35/SIF11	I/O	OD	TRI	HOLD
87	P34/T0	I/O	PU	WH	HOLD
88	P33/SIF10	I/O	OD	L	HOLD
89	P32/INT0	I/O	PU	WH	HOLD
90	P31/SIF01	I/O	OD	TRI	HOLD
91	P30/SIF00	I/O	OD	L	HOLD
92	A1	I			
93	V_{SS}				
94	EAL	I			
95	LOADREN	I			
96	V_{SS}				
97	LED3	O	OD	TRI	HOLD
98	LED2	O	OD	TRI	HOLD
99	LED1	O	OD	TRI	HOLD
100	LED0	O	OD	TRI	HOLD

NOTES:
1. During Power Down mode all floating I/O pins or inputs without internal pullups should be driven.
2. PU = Pulled Up, OD = Open Drain, WH = Weak High, TRI = Tri-State.

PORT STRUCTURES AND OPERATION

All three 51SL ports are bidirectional. Each consists of a latch (Special Function Registers P1 through P3), an output driver, and an input buffer. Port 0 of the 51SL CPU does not connect to the package pins. It is used internally to drive the keyboard scan logic.

The output drivers of ports 1 and 2 can be used in accesses to external memory. The 51SL provides the LOADREN signal to facilitate external memory interfaces. When the LOADREN signal is high, Port 1 outputs the low byte of the external memory address. If LOADREN is tied low, then the Port 1 signals continue to emit the P1 SFR content. Port 2 outputs the upper seven bits of the high byte of the external address when the address is 15 bits wide and either EAL is tied low or EAL is tied high and Bit 0 (ADDREN) of configuration register 1 is set. Otherwise, the Port 2 pins continue to emit the P2 SFR content.

I/O Configurations

All port pins with the exception of P27/LED4, P30/SIF00, P31/SIF01, P33/SIF10, and P35/SIF11 have fixed internal pullups and therefore are called "quasi-bidirectional ports". When configured as inputs, the pins are pulled high by the pullups and will source current when externally pulled low.

During a 15-bit external program memory access, Port 2 outputs the high address byte. In the 80C51 the Port 2 drivers use the strong pullup during the entire time that they are emitting a "1" on a Port 2 bit. In this instance, the 80C51 weak quasi-bidirectional pullup condition that normally occurs after two oscillator periods does not occur. Port 1 and Port 2 of the 51SL emulate the quasi-bidirectional pullup condition during program memory access, not this extended strong pullup condition.

POWER MANAGEMENT

The 51SL uses low power CHMOS and provides for two further power savings modes, available when inactive: Idle mode, typically between keystrokes; and Power Down mode, upon command from the host. A four channel, eight-bit A/D converter is also included for power management (i.e., battery voltage/temperature monitoring, etc.).

Idle Mode

Idle mode is initiated by an instruction that sets the PCON.0 bit (SFR address 87H) in the 51SL. In Idle mode, the internal clock signal to the 51SL CPU is gated off, but not to the interrupt timer and Serial Port functions. The 51SL status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data. The port pins hold the logic levels they had when Idle mode was activated. ALE and PSENL are held high. If an A/D conversion is in process when Idle mode is entered, any conversion results may contain erroneous data. Idle mode is exited via a hardware reset, or an enable interrupt.

Power Down Mode

Power Down mode is initiated by an instruction that sets bit PCON.1 in the 51SL CPU. When the 51SL enters Power Down mode, all internal clocks, including the 51SL core clock, are turned off. If an external crystal is used, the internal oscillator is turned off. MEMCSL, the external memory select signal, goes inactive unless it is configured as a general purpose I/O (i.e., unless bit 3 of configuration register 1 is a "1"). ALE and PSENL are both forced low. RAM contents are preserved.

Power Down mode can only be exited via a reset. This reset may occur either from the RST pin, or an internally generated reset. See the 51SL Hardware Description (Order No. #272268) for a detailed description of this reset.

HOST INTERFACE

The 51SL host interface is functionally compatible with the 8042 style UPI interface. It consists of the PCDB0–7 data bus; the RDL, WRL, A0 and CSL control signals; and the Keyboard Status register, Input Data register, and Output Data register. In addition, a second address line, A1, has been added to decode a second set of registers for power management functions. These registers are identical to the keyboard registers. The host interface also includes a PCOBF interrupt, GATEA20, and host reset (RCL) outputs. Two additional OBF signals, AUXOBF1 and AUXOBF2 are available through firmware configuration of P34/T0 and P37/RDL respectively.

KEYBOARD SCAN

The interface to the keyboard scan logic includes 16 slew-rate-controlled, open drain scan out lines (KSO0–15) and eight Schmitt trigger sense lines (KSI0–7) with internal pullup resistors. KSI0–7 connect directly to Port 0 of the 51SL CPU. The 16 scan out lines are controlled by the four low order bits of Port 0. Together KSO0–15 and KSI0–7 form a keyboard matrix.

EXTERNAL KEYBOARD AND MOUSE INTERFACE

Industry standard PC-AT compatible keyboards employ a two wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the 51SL provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The 51SL has four high-drive, open-drain, bidirectional port pins that can be used for external serial interfaces, such as ISA external keyboard and PS/2-type mouse interfaces. They are P30/SIF00, P31/SIF01, P33/SIF10, and P35/SIF11. P33/SIF10 is connected to the firmware configurable level/edge sensitive INTL interrupt pin of the 51SL CPU. P30/SIF00 is connected to the edge sensitive SIF0INTL interrupt pin of the 51SL CPU. Note that on the Low Voltage 8XC51SL these inputs are protected to 5.5V in order to provide compatibility with as many external keyboard and PS/2 mouse devices as possible.

DESIGN CONSIDERATIONS

The low voltage characteristics of the Low Voltage 8XC51SL have indicated that additional care should be taken in selection of the crystal used in the oscillator circuit. In particular, series resistance of a crystal seems to have the largest effect on start-up time and steady state amplitude. Consequently, the lower the series resistance the better, although medium to better quality crystals are generally more than adequate.

ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin to V_{SS} ... −0.5V to V_{CC} + 0.5V
Power Dissipation..... 1.0W**
**This value is based on the maximum allowable die temperature and the thermal resistance of the package.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

OPERATING CONDITIONS

8XC51SL: T_A (Under Bias) = 0°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V
Low Voltage 8XC51SL: T_A (Under Bias) = 0°C to +70°C, V_{CC} = +3.3V ± 0.3V, V_{SS} = 0V

8XC51SL DC Characteristics (Over Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except XTAL1, RST)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, RST)	−0.5	0.2 V_{CC} − 0.1		
V_{IH}	Input High Voltage (Except EAL, PCDB0–7, ADB0–7, XTAL1, RST, CSL, RDL, WRL, LOADREN, A0, A1)	2.4	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (EAL)	V_{CC} − 1.5	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (PCDB0–7, ADB00-7, XTAL1, RST, CSL, RDL, WRL, LOADREN, A0, A1)	0.7 V_{CC}	V_{CC} + 0.5	V	
R_P	Internal Port Resistors KSI0–7	5	20	KΩ	
V_{OL}	Output Low Voltage BP Pins(1) (Except P27/LED4)	−0.5	0.4	V	I_{OL} = 16 mA
V_{OL1}	Output Low Voltage P27/LED4, LED0–3	−0.5	0.8	V	I_{OL} = 12 mA
V_{OL2}	QB Pins(2), PCDB0–7, RCL, ADB0–7, GATEA20, KSO0–15, MEMCSL, ALE, PSENL, PCOBF	−0.5	0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage QB Pins, ALE, PSENL, PCOBF	2.4	V_{CC} + 0.5	V	I_{OH} = −60 μA
V_{OH1}	Outut High Voltage MEMCSL, PCDB0–7, ADB0–7	4.0	V_{CC} + 0.5	V	I_{OH} = −2.0 mA
V_{OH2}	Output High Voltage RCL, GATEA20	4.0	V_{CC} +0.5	V	I_{OH} = 60 μA

8XC51SL DC Characteristics (Over Operating Conditions) (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{IL}	Logical 0 Input Current QB(2) Pins		−50	μA	V_{IN} = 0.4V
I_{LI}	Input Leakage Current (BP and Pure Input Pins except for KSI0–7, XTAL1, and EAL)		±10	μA	0 < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current QB(2) Pins		−1	mA	V_{IN} = 2.0V
I_{CC}	Power Supply Current Active Mode at 16 MHz Idle Mode at 16 MHz Power-Down Mode		 38 15 TBD	 mA mA μA	

Low Voltage 8XC51SL DC Characteristics (Over Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except XTAL1, RST, KSI0–7)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, RST)	−0.5	0.2 V_{CC} − 0.1		
V_{IL2}	Input Low Voltage (KSI0–7)	−0.5	0.6		
V_{IH}	Input High Voltage (Except EAL, PCDB0–7, ADB0–7, XTAL1, RST) P30, P31, P33, P35)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (EAL)	V_{CC} − 1	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (PCDB0–7, ADB0–7, XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH3}	Input High Voltage (P30, P31, P33, P35)	2.0	5.5	V	
R_P	Internal Port Resistors KSI0–7	5	20	KΩ	
V_{OL}	Output Low Voltage BP Pins(1) (Except P27/LED4)	−0.5	0.4	V	I_{OL} = 16 mA
V_{OL1}	Output Low Voltage P27/LED4, LED0–3	−0.5	0.8	V	I_{OL} = 12 mA
V_{OL2}	Output Low Voltage QB Pins(2), PCDB0–7, RCL, ADB0–7, GATEA20, KSO0–15, MEMCSL, ALE, PSENL, PCOBF	−0.5	0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage QB Pins, ALE, PSENL, PCOBF	V_{CC} − 0.7	V_{CC} + 0.5	V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage MEMCSL, PCDB0–7, ADB0–7	2.4	V_{CC} + 0.5	V	I_{OH} = −2.0 mA
V_{OH2}	Output High Voltage RCL, GATEA20	2.4	V_{CC} +0.5	V	I_{OH} = 60 μA
I_{IL}	Logical 0 Input Current QB(2) Pins		−50	μA	V_{IN} = 0.4V
I_{LI}	Input Leakage Current (BP and Pure Input Pins except for KSI0–7, XTAL1, and EAL)		±10	μA	0 < V_{IN} < V_{CC}

Low Voltage 8XC51SL DC Characteristics (Over Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current QB(2) Pins		−650	μA	V_{IN} = 1.5V
I_{CC}	Power Supply Current Active Mode at 16 MHz Idle Mode at 16 MHz Power-Down Mode		 25 10 175	 mA mA μA	

NOTES:
1. Bidirectional (BP) pins include P27/LED4, P30/SIF00, P31/SIF01, P33/SIF10, P36/SIF11, MEMCSL, PCDB0–7, and ADB0–7.
2. Quasi-bidirectional (QB) pins include P20–6/A8–A14, P32/INT0, P34/T0, P36/WRL, P37/RDL and P10–7/A0–7.
3. Pure input pins include LOADREN, EAL, A0, A1, CSL, RDL, WRL, RST, AIN0–3, and XTAL1.

AC Characteristics

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has three or five characters. The first character is always "T" (for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. Table 3 lists the characters and their meanings.

Example

TAVLL = Time for Address Valid to ALE Low.

TLLPL = Time for ALE Low to PSEN Low.

Table 3. AC Symbol Characters

Char.	Meaning
A	Address
C	Clock
D	Input Data
H	Logic Level HIGH
I	Instruction (Program Memory Contents)
L	Logic Level LOW, or ALE
P	PSENL
Q	Output Data
R	RDL Signal
T	Time
V	Valid
W	WRL Signal
X	No Longer a Valid Logic Level
Z	Float

HOST-INTERFACE TIMING

All Outputs Loaded with 50 pF

Symbol	Parameter	Min	Max	Units
TAR	CSL, A0/A1 Setup to RD Low	0		ns
TRA	CSL, A0/A1 Hold after RDL High	0		ns
TAD	CSL, A0/A1 to Data Out Delay		50	ns
TAW	CSL, A0/A1 Setup to WRL Low	0		ns
TWA	CSL, A0/A1 Hold after WRL High	10		ns
TDW	Data Setup to WRL High	60		ns
TWD	Data Hold after WRL High	5		ns
TWW	Minimum Pulse Width of WRL	50		ns
TRR	RDL Pulse Width	50		ns
TRD	RDL Low to Data Out Delay		50	ns
TDF	RDL High to Data Float Delay		50	ns

EXTERNAL MEMORY TIMING

TCLCL = 1 Clock Period, All Outputs Loaded with 50 pF

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	2	16	MHz
TLHLL	ALE Pulse Width	2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	TCLCL−40		ns
TLLAX	Address Hold after ALE Low	TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		4TCLCL−100	ns
TLLPL	ALE Low to PSENL Low	TCLCL−30		ns
TPLPH	PSENL Pulse Width	3TCLCL−45		ns
TPLIV	PSENL Low to Valid Instruction In		3TCLCL−105	ns
TPXIX	Input Instruction Hold after PSENL High	0		ns
TPXIZ	Input Instruction Float after PSENL High		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		5TCLCL−105	ns
TPLAZ	PSENL Low to Address Float		10	ns
TRLRH	P37/RDL Pulse Width	6TCLCL−50		ns
TWLWH	P36/WRL Pulse Width	6TCLCL−50		ns
TRLDV	P37RDL Low to Valid Data In		5TCLCL−100	ns
TRHDX	Data Hold after P37/RDL	0		ns
TRHDZ	Data Float after P37/RDL		2TCLCL−50	ns
TLLDV	ALE Low to Valid Data In		8TCLCL−100	ns
TAVDV	Address to Valid Data In		9TCLCL−100	ns
TLLWL	ALE Low to P37/RDL or P36/WRL Low	3TCLCL−25	3TCLCL+25	ns
TAVWL	Address Valid to P36/WRL Low	4TCLCL−50		ns
TQVWX	Data Valid before P36/WRL	TCLCL−25		ns
TWHQX	Data Hold after P36/WRL	TCLCL−25		ns
TQVWH	Data Valid to P36/WRL High	7TCLCL−50		ns
TRLAZ	P37/RDL Low to Address Float		0	ns
TWHLH	P37/RDL or P36/WRL High to ALE High	TCLCL−25	TCLCL+25	ns

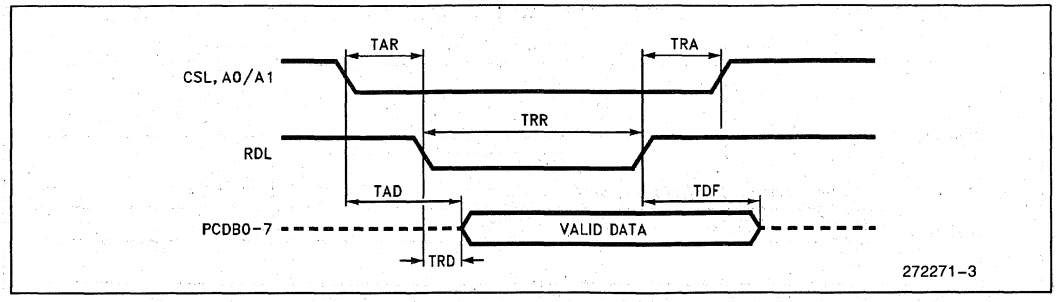


Figure 3. Host-Interface Read

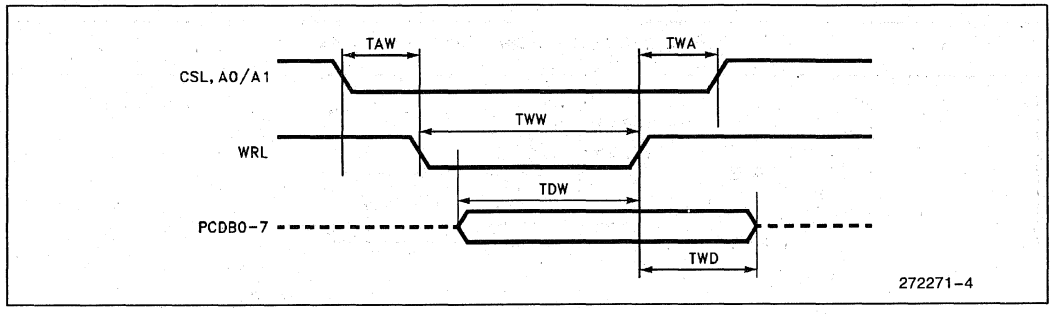


Figure 4. Host-Interface Write

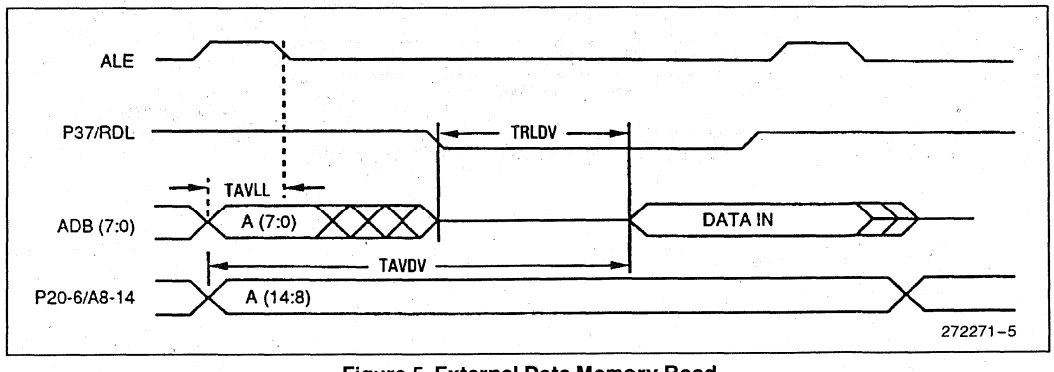


Figure 5. External Data Memory Read

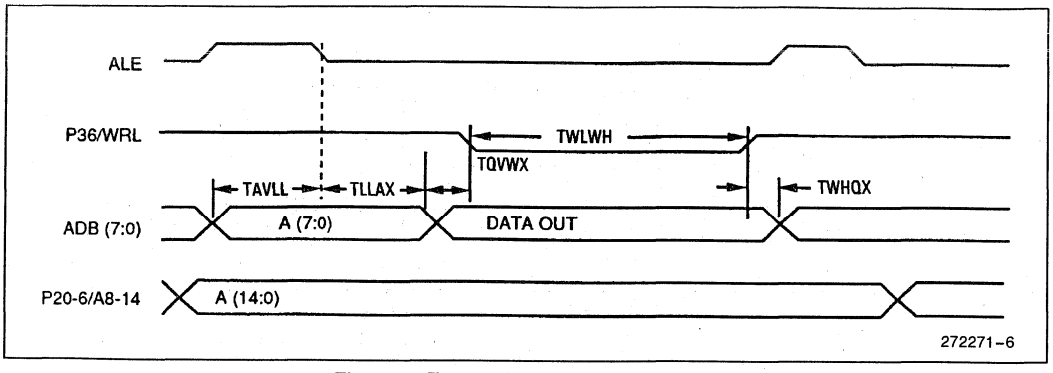


Figure 6. External Data Memory Write

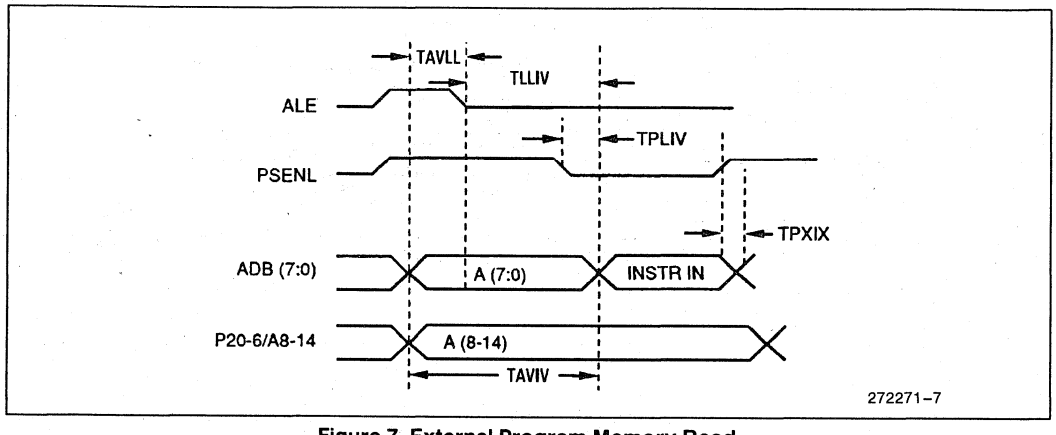


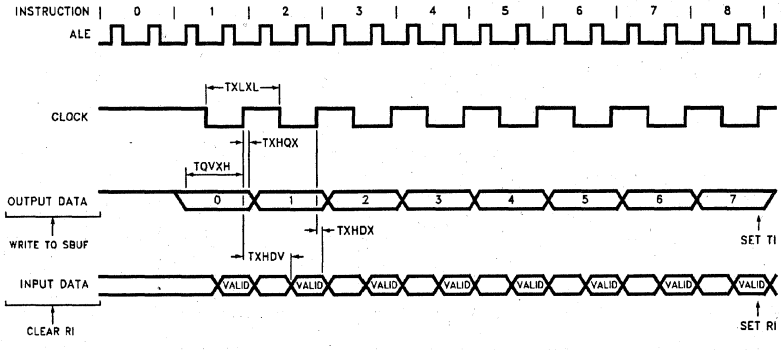
Figure 7. External Program Memory Read

SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: Over Operating Conditions, Load Capacitance = 50 pF

Symbol	Parameter	16 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	750		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	492		10TCLCL−133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		2TCLCL−117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		492		10TCLCL−133	ns

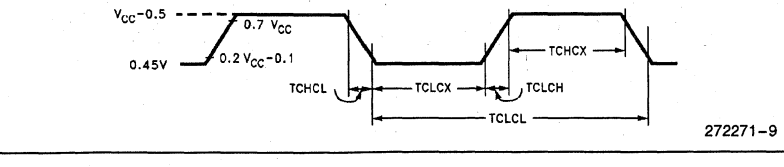
SHIFT REGISTER MODE TIMING WAVEFORMS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	2.0	16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



PROGRAMMING THE OTP

The part must be running with a 4 MHz to 6 MHz oscillator. The address of a location to be programmed is applied to address lines, while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 4. Normally EAL/V_{PP} is held at a logic high until just before RCL/PROGL is to be pulsed. The EAL/V_{PP} is raised to V_{PP}, RCL/PROGL is pulsed low and then EAL/V_{PP} is returned to V_{CC} (also refer to timing diagrams). Also, the LOADREN signal must be grounded when programming or verifying.

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

DEFINITION OF TERMS

ADDRESS LINES: P10–P17, P20–P25, respectively for A0–A13.

DATA LINES: ADB0–7.

CONTROL SIGNALS: RST, GATEA20, P26, P27, P32, P36, P37.

PROGRAM SIGNALS: RCL/PROGL, EAL/V_{PP}.

PROGRAMMING ALGORITHM

Refer to Table 4 and Figures 8 and 9 for address, data and control signals setup. To program the 87C51SL the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EAL/V_{PP} from V_{CC} to 12.75V ±0.25V.
5. Pulse RCL/PROGL 5 times.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

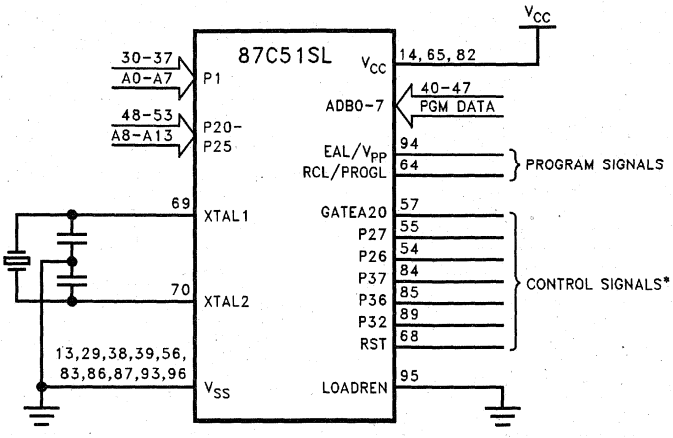
Table 4. OTP Programming Modes

Mode	RST	GATEA20	RCL/ PROGL	EAL/V_{PP}	P26	P27	P32	P36	P37
Program Code Data	H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data	H	L	H	H	L	L	L	H	H
Read Signature Byte	H	L	H	H	L	L	L	L	L

Note that in the above table, to program code data on the Low Voltage 87C51SL V_{CC} must be raised to 5V ±10%. In addition, all address lines, data lines, and control signals being driven to a "High" level must be raised to 5V ±10%. The RCL/PROGL signal must pulse between 0V and 5V ±10%.

To verify code data or read the signature bytes of the Low Voltage 87C51SL V_{CC} must be set to 3.3V ±0.3V. In addition, all address lines and control signals being driven to a "High" level must be raised to 3.3V ±0.3V.

For the standard (5V version) of the 87C51SL V_{CC} must always be at 5V ±10%, and all "High" voltages must meet the DC specs indicated in the DC Characteristics section of this document.



*See Table 4 for proper input on these pins.

Figure 8. Programming/Verifying the OTP

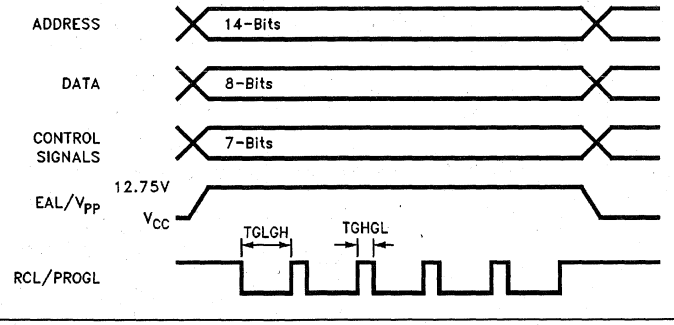


Figure 9. Programming Signal's Waveforms

PROGRAM VERIFY

Program verify may be done after each byte that is programmed, or after a block of bytes that is programmed. In either case a complete verify of the array will ensure that it has been programmed correctly.

READING THE SIGNATURE BYTES

The 8XC51SL and Low Voltage 8XC51SL each have three signature bytes in locations 30H, 31H, and 60H. To read these bytes, follow the procedure for EPROM verify, but activate the control lines provided in Table 4 for Read Signature Byte.

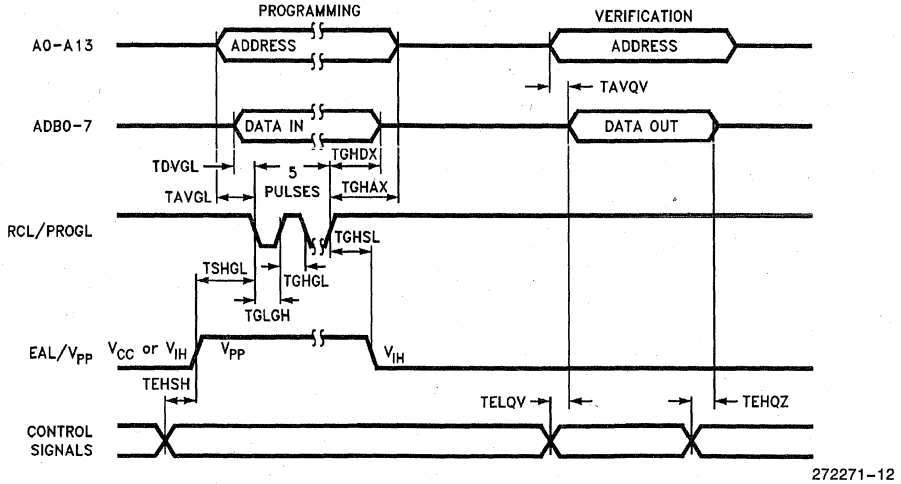
Location	Contents			
	87C51SL	83C51SL	Low Voltage 87C51SL	Low Voltage 83C51SL
30H	89H	89H	89H	89H
31H	58H	58H	58H	58H
60H	BBH	3BH	ABH	2BH

OTP PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_A = 21°C to 27°C; V_{CC} = 5V ± 10% for 87C51SL, 3.3V ± 0.3V for Low Voltage 87C51SL (verification only). V_{CC} for programming the Low Voltage 87C51SL must be 5.0V ±10%. V_{SS} = 0V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setp to PROGL Low	48TCLCL		
TGHAX	Address Hold after PROGL	48TCLCL		
TDVGL	Data Setup to PROGL Low	48TCLCL		
TGHDX	Data Hold after PROGL	48TCLCL		
TEHSH	(Enable) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to PROGL Low	10		µs
TGHSL	V_{PP} Hold after PROGL	10		µs
TGLGH	PROGL Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after Enable	0	48TCLCL	
TGHGL	PROGL High to PROGL Low	10		µs

PROGRAMMING AND VERIFICATION WAVEFORMS



A/D CHARACTERISTICS

The 51SL includes a four-channel, 8-bit A/D converter. This A/D, with eight bits of accuracy, uses successive approximation with a switch capacitor comparator. It is designed to be used for sampling static analog signals (i.e., ideally suited for power management tasks such as battery voltage monitoring, etc.). The nominal conversion rate is 20 μs at 16 MHz. The analog high and low voltage references are connected to AVREF and AVGND, respectively. The four input channels, AIN0–3 are connected from the package pins, unbuffered, to an analog multiplexer (on-chip). The absolute conversion accuracy is dependent upon the accuracy of AVREF. The specifications given assume adherence to the operating conditions section of this data sheet.

Testing is done at AVREF = 5.12V and V_{CC} = 5.0V for the 8XC51SL, and at AVREF = 3.2V and V_{CC} = 3.3V for the Low Voltage 8XC51SL.

OPERATING CONDITIONS

V_{CC}
- 8XC51SL .....4.5V to 5.5V
- Low Voltage 8XC51SL .....3.0V to 3.6V

AVREF
- 8XC51SL .....4.5V to 5.5V
- Low Voltage 8XC51SL .....3.0V to 3.6V

V_{SS}, AVSS 0V

AIN0–3 .....AVSS to AVREF

T_A .....0°C to +70°C Ambient

F_{OSC} .....2 MHz to 16 MHz

A/D CONVERTER SPECIFICATIONS (Over Operating Conditions)

Parameter	Min	Typ	Max	Units
Resolution	255 8		256 8	Levels Bits
Absolute Error	0		±1	LSB
Full Scale Error		±1		LSB
Zero Offset Error		±1		LSB
Non-Linearity Error	0		±1	LSB
Differential Non-Linearity Error	0		±1	LSB
Channel to Channel Matching	0		±1	LSB
Repeatability		±0.25		LSB
Temperature Coefficients Offset Full Scale Differential Non-Linearity		 0.003 0.003 0.003		 LSB/°C LSB/°C LSB/°C
Off Isolation	−60			dB
Feedthrough		−60		dB
V_{CC} Power Supply Rejection		−60		dB
Input Resistance	750		1.2K	Ω
Input Capacitance		3		pF
DC Input Leakage	0		3.0	μA

A/D Glossary of Terms

Absolute Error—The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

Actual Characteristic—The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An actual characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversions under the same conditions.

Break-Before-Make—The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected (e.g., the converter will not short inputs together).

Channel-to-Channel Matching—The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

Characteristic—A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

Code—The digital value output by the converter.

Code Center—The voltage corresponding to the midpoint between two adjacent code transitions.

Code Transition—The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

Code Width—The voltage corresponding to the difference between two adjacent code transitions.

Crosstalk—See "Off-Isolation".

DC Input Leakage—Leakage current to ground from an analog input pin.

Differential Non-Linearity—The difference between the ideal and actual code widths of the terminal based characteristic.

Feedthrough—Attenuation of a voltage applied on the selected channel of the A/D Converter after the sample window closes.

Full Scale Error—The difference between the expected and actual input voltage corresponding to the full scale code transition.

Ideal Characteristic—A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

Input Resistance—The effective series resistance from the analog input pin to the sample capacitor.

LSB—Least Significant Bit—The voltage corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For an 8-bit converter with a reference voltage of 5.12V, one LSB is 20 mV. Note that this is different than digital LSBs since an uncertainty of two LSBs, when referring to an A/D converter, equals 40 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 80 mV).

Monotonic—The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

No Missed Codes—For each and every output code, there exists a unique input voltage range which produces that code only.

Non-Linearity—The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristic.

Off-Isolation—Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

Repeatability—The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

Resolution—The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

Sample Delay—The delay from receiving the start conversion signal to when the sample window opens.

Sample Delay Uncertainty—The variation in the sample delay.

Sample Time—The time that the sample window is open.

Sample Time Uncertainty—The variation in the sample time.

Sample Window—Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

Successive Approximation—An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

Temperature Coefficients—Change in the stated variable per degree centrigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of temperature drift.

Terminal Based Characteristic—An actual characteristic which has been rotated and translated to remove zero offset and full scale error.

V_{CC} Rejection—Attenuation of noise on the V_{CC} line to the A/D converter.

Zero Offset—The difference between the expected and actual input voltage corresponding to the first code transition.

DATA SHEET REVISION SUMMARY

The following differences exist between this data sheet (272271-002) and the previous version (272271-001).

1. Data sheet status changed from "Product Preview" to "Advance Information".
2. Title page item number three describing the global interrupt enable change was removed.
3. Title page item number two was corrected to read " . . . was added in configuration register 1."
4. In the 8XC51SL DC Characteristics section:

   The V_{OH} test condition (I_{OH}) changed from −0.8 mA to −60 μA.

   The V_{OH1} test condition (I_{OH}) changed from −4.0 mA to −2.0 mA.

   V_{OH2} was added.

   The XTAL1 and EAL pins were added to the I_{LI} spec.

   The I_{TL} spec changed from −650 μA to −1 mA.

   The I_{CC} idle spec changed from 10 mA to 15 mA.

   The I_{CC} Power Down spec changed from 100 μA to TBD.
5. In the Low Voltage 8XC51SL DC Characteristics section:

   The V_{OH} spec changed from 2.4V to V_{CC} −0.7

   The V_{OH} test condition (I_{OH}) changed from −0.8 mA to −60 μA.

   V_{OH2} was added.

   Pins were clarified in the I_{LI} spec.

   The I_{TL} test condition (V_{IN}) was changed from TBD to 1.5V.

   The I_{CC} Power Down spec changed from 100 μA to 175 μA.
6. The load capacitance for all timing tables was changed to 50 pF.
7. In the Host Interface Timing Section TWD changed from 0 ns to 5 ns.
8. The External Memory Timing table changed as follows:

Spec.	Old	New
TLLIV	4TCLCL-50	4TCLCL-100
TPLIV	3TCLCL-50	3TCLCL-105
TPXIZ	TCLCL-15	TCLCL-25
TAVIV	5TCLCL-50	5TCLCL-105
TRLDV	5TCLCL-50	5TCLCL-100
TLLDV	8TCLCL-50	8TCLCL-100
TAVDV	9TCLCL-50	9TCLCL-100
TMVDV	9TCLCL-50	Removed
TMVIV	5TCLCL-50	Removed

9. In Figures 5 and 7 the MEMCSL waveforms were removed.
10. Clarification was added in the Programming Algorithm section.
11. In the A/D Converter Specifications section the minimum resolution was changed from 256 levels to 255 levels.
12. The Data Sheet Revision Summary was added.

PRODUCT PREVIEW

83C51KB
HIGH PERFORMANCE
KEYBOARD MICROCONTROLLER

- Direct Drive LED Outputs
  - Four Pins (P3.7:4)
  - 13 mA Typical Current Sink Capability
- 20 pF Cap On-chip for RC Resonator
  - Frequency Selectable (4-6 MHz)
- 8 Dedicated Key Scan Input (KSI) Pins
  - Schmitt-trigger Inputs
  - External Interrupt
  - Level Detect Interrupt Mode for Automatic Power-down Exit
- 16 Dedicated Key Scan Output (KSO) Pins with Quasi-bidirectional Port Drivers
  - No External Resistor Required
  - Located on P0.7:0 and P2.7:0
- 4-Kbyte On-chip ROM Memory
- 128-byte On-chip RAM Memory
- Clock/Data Drivers to Motherboard
  - Strong Pullup Drivers for Keyboard Cable Communication
  - 8X42 Compatible Interface
  - Selectable external interrupt for Clock
- ONCE mode (On-chip Emulation)
- Power-on Reset Mode
  - Automatic Operation
- 5 Volt D.C. Operation
- Reduces Manufacturing Cost by Reducing Overall Component Count
- Configurable Timer (16 bit or 2 by 8 Bit)
- Uses Industry Standard Design Tools
- Control Oriented Instruction Set
- Industry Standard Architecture

The 83C51KB is a highly integrated keyboard microcontroller for the standard and advanced desktop keyboard industry. The integration of external components into the microcontroller reduces overall keyboard control system manufacturing cost in terms of the number of components used, the amount of PCB space required, reduced inventory, and a reduction in required assembly activities. In addition, the integration reduces the number and amount of software routines needed for signal debounce and input status poll operation. There is a resultant reduction in CPU overhead as well as on-chip memory requirements. The 83C51KB product line is manufactured with Intel state of the art complimentary high-performance metallic oxide semiconductor (CHMOS) design rules.

Order Number: 272800-001

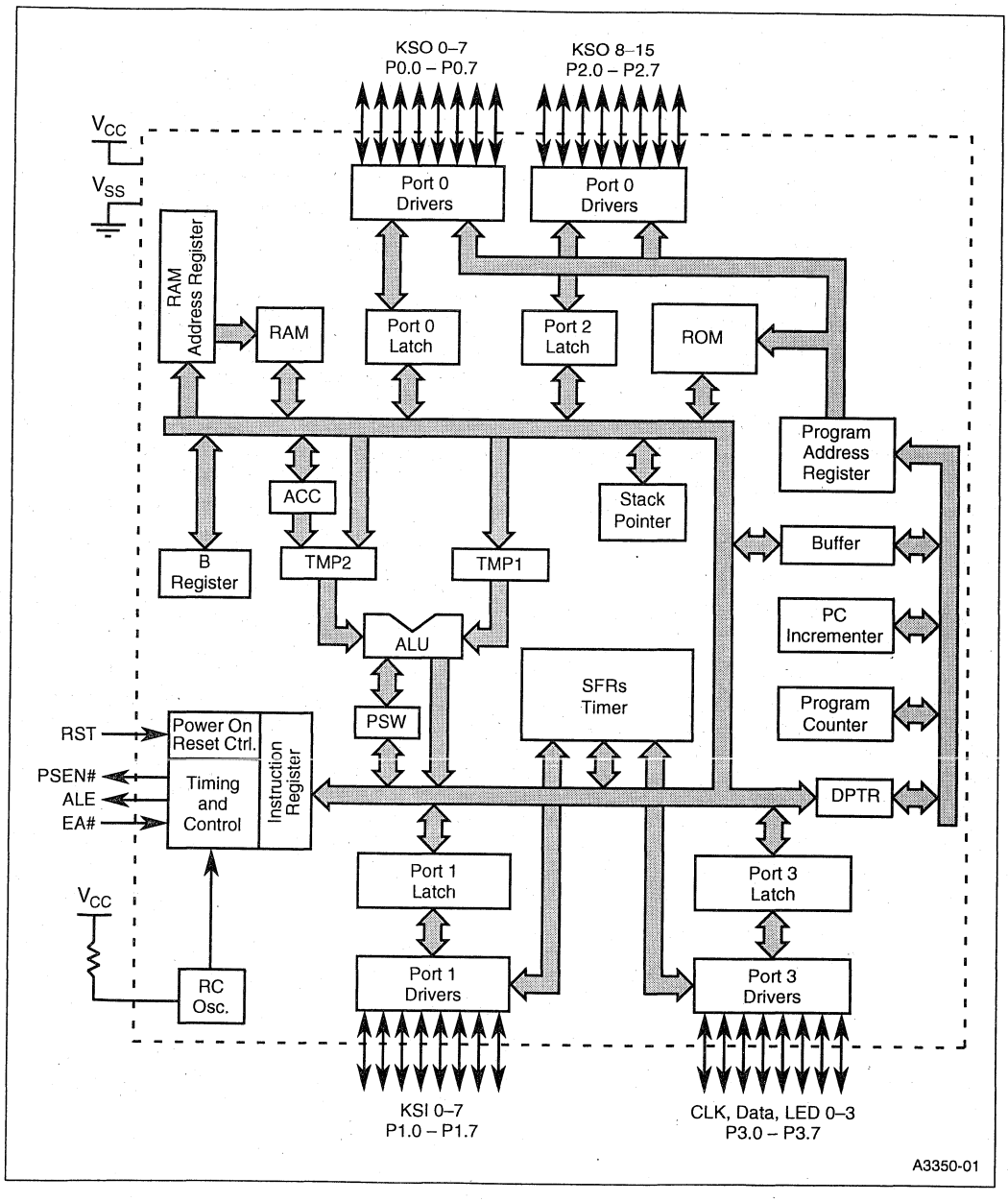


Figure 1. 83C51KB Block Diagram

1.0 TEMPERATURE RANGE

With the commercial (standard) temperature marking, this product line operates over the temperature range 0°C to +70°C.

2.0 PROCESS INFORMATION

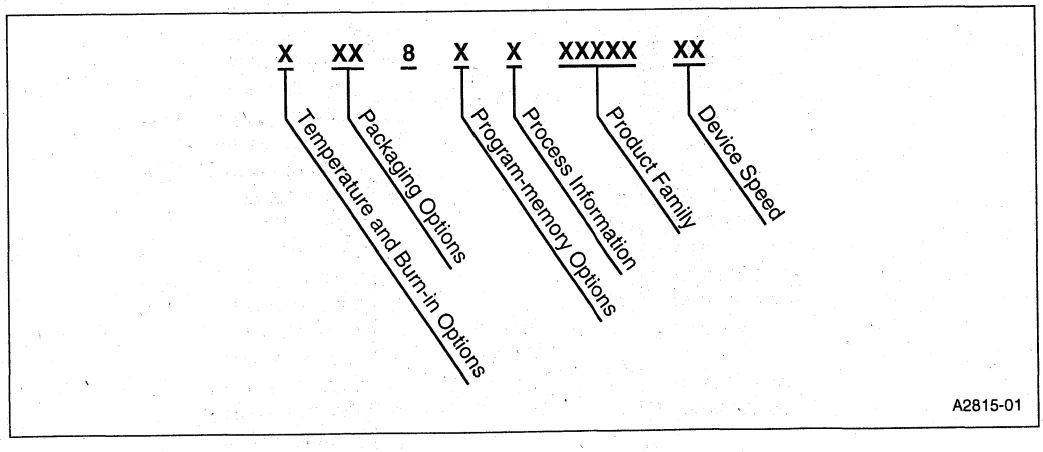
This device is manufactured on a complimentary high-performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
40-lead PDIP	70°C/W	25°C/W

3.0 83C51KB PACKAGE INFORMATION



The 83C51KB Family Nomenclature

Table 2. 83C51KB Nomenclature Definitions

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	P	Plastic Dual-in-line Package (PDIP)
Program Memory Options	3	Factory programmed ROM
Process Information	C	CHMOS
Product Family	51	MCS 51 Compatible Product Family
Device Memory Options	KB	128 bytes RAM
		4 Kbytes ROM
Device Speed	no mark	4-6 MHz

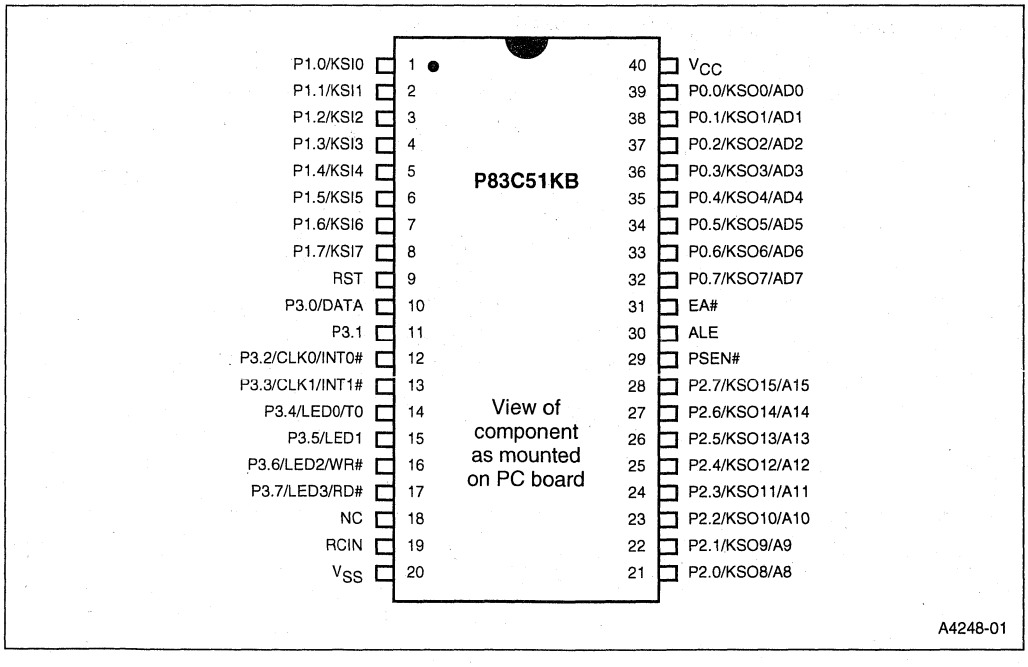


Figure 2. 83C51KB 40-pin DIP Diagram

4.0 83C51KB MEMORY

Table 3. 83C51KB Memory Map

Code Memory	Description	Notes
FFFFH 0000H	External code memory	4
0FFFH 0000H	4-Kbyte on-chip code memory array.	

Data Memory	Description	
FFFFH 0000H	External data memory	2, 3
00FFH 0080H	Special function registers	1
007FH 0020H	On-chip RAM	5
001FH 0000H	4 banks of general purpose registers, R0-R7	

NOTE:
1. The special function registers (SFRs) are accessible by direct addressing only.
2. Data in this area is accessible by indirect addressing only.
3. RD#/WR# active for these external data addresses.
4. PSEN# active for the external code addresses.
5. Addresses 20H through 2FH are bit addressable.

5.0 SIGNAL DESCRIPTION

Table 4. 40-pin DIP Signals Arranged by Name

Keyboard	
Name	**Pin**
P0.7/KSO7/AD7	32
P0.6/KSO6/AD6	33
P0.5/KSO5/AD5	34
P0.4/KSO4/AD4	35
P0.3/KSO3/AD3	36
P0.2/KSO2/AD2	37
P0.1/KSO1/AD1	38
P0.0/KSO0/AD0	39
P2.7/KSO15/A15	28
P2.6/KSO14/A14	27
P2.5/KSO13/A13	26
P2.4/KSO12/A12	25
P2.3/KSO11/A11	24
P2.2KSO10/A10	23
P2.1/KSO9/A9	22
P2.0/KSO8/A8	21

Keyboard	
Name	**Pin**
P 1.0/KSI0	1
P1.1/KSI1	2
P1.2/KSI2	3
P1.3/KSI3	4
P1.4/KSI4	5
P1.5/KSI5	6
P1.6/KSI6	7
P1.7/KSI7	8
P3.0/DATA	10
P3.1	11
P3.2/CLK0/INT0#	12
P3.3/CLK1/INT1#	13
P3.4/LED0/T0	14
P3.5/LED1	15
P3.6/LED2/WR#	16
P3.7/LED3/RD#	17

Chip Control	
Name	**Pin**
RCIN	19
RST	9
ALE	30
PSEN#	29
EA#	31

Power & Ground	
Name	**Pin**
V_{CC}	40
V_{SS}	20

Table 5. 40-pin DIP Signals Arranged by Pin Number

Pin	Name	Pin	Name
1	P 1.0/KSI0	21	P2.0/KSO8/A8
2	P1.1/KSI1	22	P2.1/KSO9/A9
3	P1.2/KSI2	23	P2.2KSO10/A10
4	P1.3/KSI3	24	P2.3/KSO11/A11
5	P1.4/KSI4	25	P2.4/KSO12/A12
6	P1.5/KSI5	26	P2.5/KSO13/A13
7	P1.6/KSI6	27	P2.6/KSO14/A14
8	P1.7/KSI7	28	P2.7/KSO15/A15
9	RST	29	PSEN#
10	P3.0/DATA	30	ALE
11	P3.1	31	EA#
12	P3.2/CLK0/INT0#	32	P0.7/KSO7/AD7
13	P3.3/CLK1/INT1#	33	P0.6/KSO6/AD6
14	P3.4/LED0/T0	34	P0.5/KSO5/AD5
15	P3.5/LED1	35	P0.4/KSO4/AD4
16	P3.6/LED2/WR#	36	P0.3/KSO3/AD3
17	P3.7/LED3/RD#	37	P0.2/KSO2/AD2
18	NC	38	P0.1/KSO1/AD1
19	RCIN	39	P0.0/KSO0/AD0
20	V_{SS}	40	V_{CC}

Table 6. 83C51KB Signal Description

Signal Name	Type	Description	Alternate Function
A15:8†	O	**Address Signals** . Upper address lines for the external bus. These signals are normally used for the KSO15:8 scan function and are not available for external memory access in a keyboard application. (See KSO signals).	KSO.15:8 P2.15:8
AD7:0†	I/O	**Address/Data Signals**. Multiplexed lower address and data signals for external memory. These signals are normally used for the KSO7:0 scan function and are not available for external memory access in a keyboard application. (See KSO)	KSO.7:0 P0.7:0
ALE†	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. Since these external address signals are normally used for the KSO scan function, the ALE should not be used for external memory access in a keyboard application. ALE can be disabled when not used for external memory access by setting bit 0 of SFR AUXR at address 8EH.	
CLK1:0 P3.3:2	I/O	**Clock signal**. Either P3.2 or P3.3 is configurable with a 1.8KΩ pullup and with external interrupt INT0# or INT1# and used as keyboard CLK signal.	INT1:0#
DATA P3.0	I/O	**DATA signal**. P3.0 is configurable with a 1.8KΩ pullup and used as keyboard Data signal..	
EA#	I	**External Access**. Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. EA# should always be strapped to V_{CC} for keyboard applications using the 83C51KB.	
INT1:0#†	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#. For keyboard applicaitons, these signals are normally used for the CLK signals. (See KSIINT and CDPU bits in the PCON register)	CLK1:0 P3.3:2
KSI7:0 P1.7:0	I/O	**Keyboard Scan Inputs**. Application specific keyboard signals.	
KSO15:0 P2.15:8 P0.7:0	I/O	**Keyboard Scan Outputs**. The KSO signals are application specific to keyboard scan functions.	
LED3:0 P3.7:4	I/O	**Light Emitting Diode Drivers**. The LED signals are specifically designed to drive LEDs connected to Vcc directly (see D.C. Characteristics). The alternate functions are not available for keyboard applications.	RD#, WR#, T0
N/C	—	**No Connection Signal**. This signal is to be unconnected.	
P0.7:0†	I/O	**Port 0**. This is an 8-bit quasi-bidirectional I/O port (see KSO signals, see also AD7:0).	AD7:0
P1.7:0	I/O	**Port 1**. This is an 8-bit quasi-bidirectional I/O port (see KSI signals).	
P2.7:0	I/O	**Port 2**. This is an 8-bit quasi-bidirectional I/O port (see also A15:8).	A15:8

† The descriptions of RD#, WR#, ALE, P'SEN#, A15:8/P2.7:0 and AD7:0/P0.7:0 are documented for the standard MCS 51 microcontrollers. They are not used for these functions in keyboard applications.

Table 6. 83C51KB Signal Description

Signal Name	Type	Description	Alternate Function
P3.7:0	I/O	**Port 3.** This is an 8-bit quasi-bidirectional I/O port (see CLK1:0, DATA, LED3:0).	
PSEN#†	O	**Program Store Enable.** This output is asserted for external program memory fetch operations. It is not available for keyboard applications.	—
RCIN	I	**Resonant Clock Input.** RC resonator generated by connecting 1% precision resistor to V_{CC} or provide an external clock input from an external clock device.	
RD#†	O	**Read .** Read signal output for external data memory read operations. It is not available for keyboard applications.	LED3
RST	I	**Reset.** Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation. This signal is input only. When power is applied to the chip, the internal reset signal remains high for approximately 80ms to 260ms (see the datasheet for current specifications). The reset circuit then deactivates and does not reactivate unless V_{CC} drops below the crossover at approximately 3VDC.	—
V_{CC}	PWR	**Supply Voltage.** Connect this pin to the +5V supply voltage.	—
V_{SS}	GND	**Circuit Ground.** Connect this pin to ground.	—
WR#†	O	**Write.** Write signal output for external data memory write operations. It is not available for keyboard applications.	LED2

† The descriptions of RD#, WR#, ALE, P'SEN#, A15:8/P2.7:0 and AD7:0/P0.7:0 are documented for the standard MCS 51 microcontrollers. They are not used for these functions in keyboard applications.

6.0 ELECTRICAL CHARACTERISTICS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature under Bias:
Commercial ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin to V_{SS} ..... -0.5 V to +6.5 V
I_{OL} per I/O Pin ..... 15 mA
Power Dissipation ..... 1.5 W

NOTE: Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias):
Commercial ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
V_{SS} ..... 0 V

†**WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

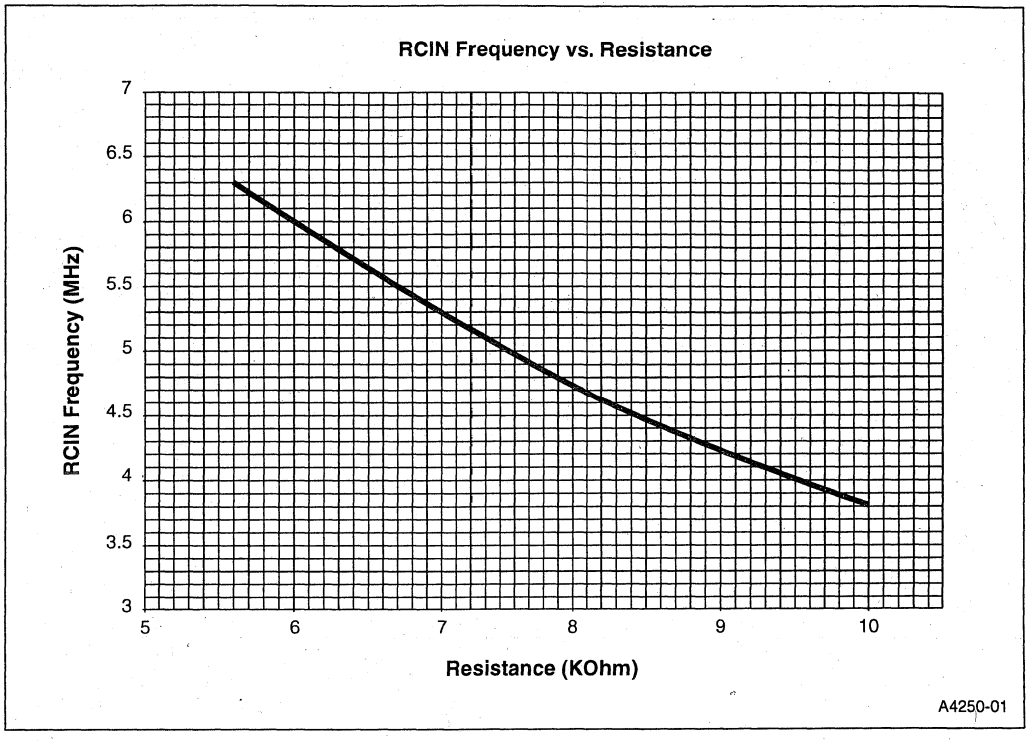


Figure 3. RCIN Frequency

NOTE: RC resonator accuracy is ± 5% at fixed V_{CC} and temperature using a 1% external precision resistor.

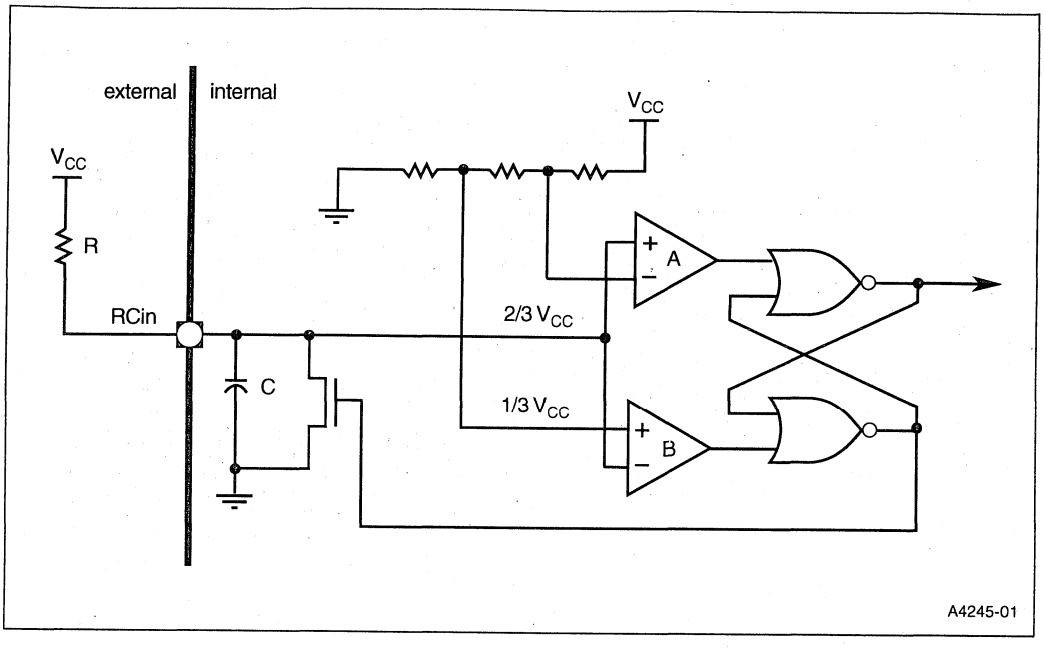


Figure 4. RC Oscillator

6.1 D.C. Characteristics

Table 7. D.C. Characteristics

Symbol	Parameter	Min	Typical (note 1)	Max	Unit	Test Condition
V_{IL}	Input Low Voltage (except EA#, RCIN, RST)	-0.5		0.2 V_{CC} -0.1	V	
V_{IL1}	Input Low Voltage RST	0		0.2 V_{CC} -0.3	V	
V_{IL2}	Input Low Voltage EA#	-0.5		0.5	V	
V_{IL3}	Input Low Voltage RCIN			V_{CC}/3	V	
V_{IH}	Input High Voltage (except EA#, RCIN, RST)	0.2V_{CC}+ 0.9		V_{CC}+0.5	V	
V_{IH1}	Input High Voltage (EA#, RST)	0.7V_{CC}		V_{CC}+0.5	V	
V_{IH2}	Input High Voltage RCIN	2V_{CC}/3				I_{IH} = 8 mA when external clock source is used on RCIN
V_{OL}	Output Low Voltage (Port 0, 1, 2, 3, ALE, PSEN# except P3.4/LED0, P3.5/LED1, P3.6/LED2, P3.7/LED3)			0.3 0.45 1.0	V	I_{OL}=200 µA I_{OL}=3.2 mA I_{OL}=7.0 mA (note 2,3)
I_{OL}	Output Low Current (P3.4/LED0, P3.5/LED1, P3.6/LED2, P3.7/LED3 only)	6	13	22	mA	V_{OL}=3.0 V
V_{OH}	Output High Voltage (Port 0, 1, 2, 3, ALE, PSEN#, except P3.0, P3.2, P3.3)	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5			V	I_{OH}= -25 µA I_{OH}= -65 µA I_{OH}= -100 µA (note 4)

NOTE:

1. Typical values are obtained using V_{CC}=5.0V, TA=25°C and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:
   Maximum I_{OL} per Port Pin—Port 0, 1, 2, P3.1-P3.3: 10mA
   Maximum I_{OL} per Port Pin—P3.4-P3.7: 22mA
   Maximum I_{OL} per 8-bit port—Port 0-2: 15mA
   Ports 3: 95mA
   Maximum Total I_{OL} for AllOutput Pins: 110mA

   If I_{OL} exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V to be superimposed on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify signals with a Schmitt Trigger, or CMOS-level input logic.

4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

Table 7. D.C. Characteristics (Continued)

Symbol	Parameter	Min	Typical (note 1)	Max	Unit	Test Condition
V_{OH1}	Output High Voltage (P3.0, P3.2, P3.3 without 1.8K Ohm pullup)	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5			V	I_{OH}= -8 µA I_{OH}= -25 µA I_{OH}= -50 µA
V_{OH2}	Output High Voltage (P3.0, P3.2, P3.3 with 1.8K Ohm pullup)	V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5			V	I_{OH}= -0.15 mA I_{OH}= -0.50 mA I_{OH}= -1.0 mA
R_{RST}	Reset Pulldown Resistor	40		225	K Ohm	
R_{CD}	Pull Up Resistance (P3.0, P3.2, P3.3 with 1.8K Ohm pullup)	1.2	1.8	2.9	K Ohm	
C_{IO}	Pin Capacitance		10		pF	@1MHz, 25°C
I_{IL}	Logical 0 Input Current (Port 0, 1, 2, 3, except P3.0, P3.2, P3.3)			-50	µA	V_{IN}=0.45V
I_{IL1}	Logical 0 Input Current (P3.0, P3.2, P3.3 without 1.8K Ohm pullup)			-250	µA	V_{IN}=0.45V
I_{IL2}	Logical 0 Input Current (P3.0, P3.2, P3.2 with 1.8K Ohm pullup)	-1.5		-4.5	mA	V_{IN}=0.45V
I_{TL}	Logical 1-to-0 Transiton Current (Port 0, 1, 2, 3)			-650	µA	V_{IN}=2.0V
I_{TL1}	Logical 1-to-0 Transition Current (P3.0, P3.2 or P3.3 with 1.8K Ohm pullups)			-4.5	mA	V_{IN} = 2.0V

NOTE:

1. Typical values are obtained using V_{CC}=5.0V, TA=25°C and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:
   Maximum I_{OL} per Port Pin—Port 0, 1, 2, P3.1-P3.3: 10mA
   Maximum I_{OL} per Port Pin—P3.4-P3.7: 22mA
   Maximum I_{OL} per 8-bit port—Port 0-2: 15mA
   Ports 3: 95mA
   Maximum Total I_{OL} for AllOutput Pins: 110mA

   If I_{OL} exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V to be superimposed on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify signals with a Schmitt Trigger, or CMOS-level input logic.

4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

Table 7. D.C. Characteristics (Continued)

Symbol	Parameter	Min	Typical (note 1)	Max	Unit	Test Condition
I_{CC}	Power Supply Current: Active Mode at 6MHz Idle Mode at 6MHz Power Down Mode		7 2 10	12 5 50	mA mA µA	RST, EA# to V_{CC} RST, EA# to V_{SS} RST, EA# to V_{SS} (RCIN pin to external resistor, all other pins are no connect)
V_{POR}	Power on reset crossover	2.4	3	3.6	V	

NOTE:

1. Typical values are obtained using V_{CC}=5.0V, TA=25°C and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:
   Maximum I_{OL} per Port Pin—Port 0, 1, 2, P3.1-P3.3: 10mA
   Maximum I_{OL} per Port Pin—P3.4-P3.7: 22mA
   Maximum I_{OL} per 8-bit port—Port 0-2: 15mA
   Ports 3: 95mA
   Maximum Total I_{OL} for AllOutput Pins: 110mA

   If I_{OL} exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V to be superimposed on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify signals with a Schmitt Trigger, or CMOS-level input logic.

4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

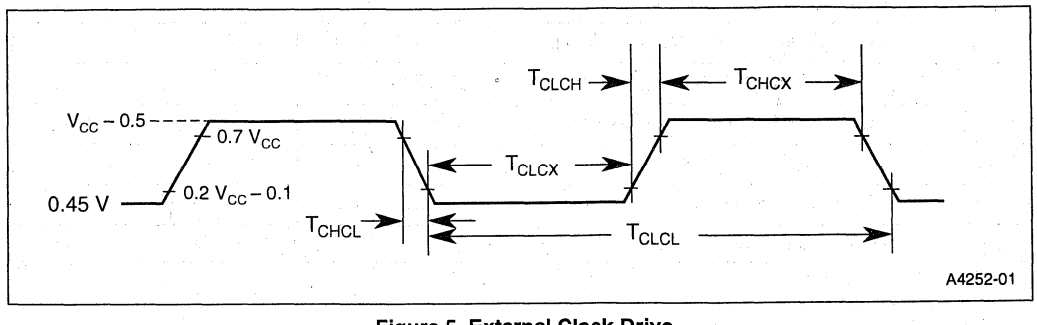


Figure 5. External Clock Drive

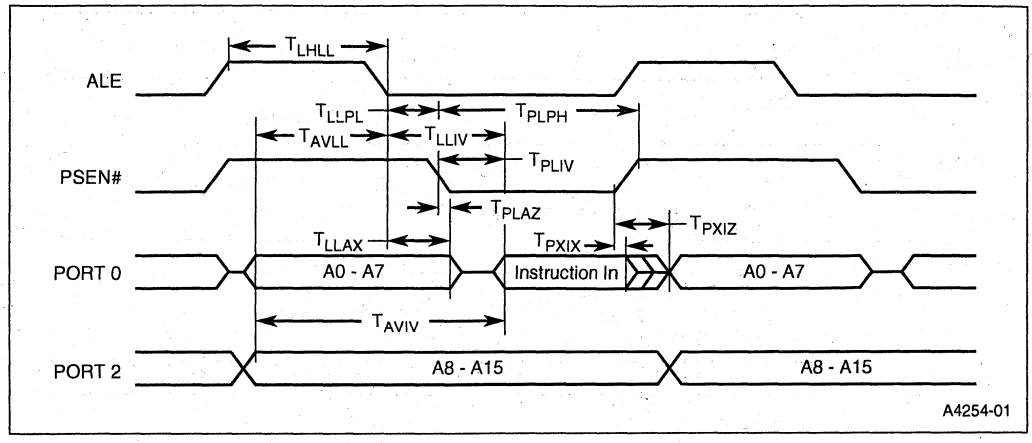
6.2 A.C. Characteristics

Table 8. A.C. Characteristics (Note 1, 2)

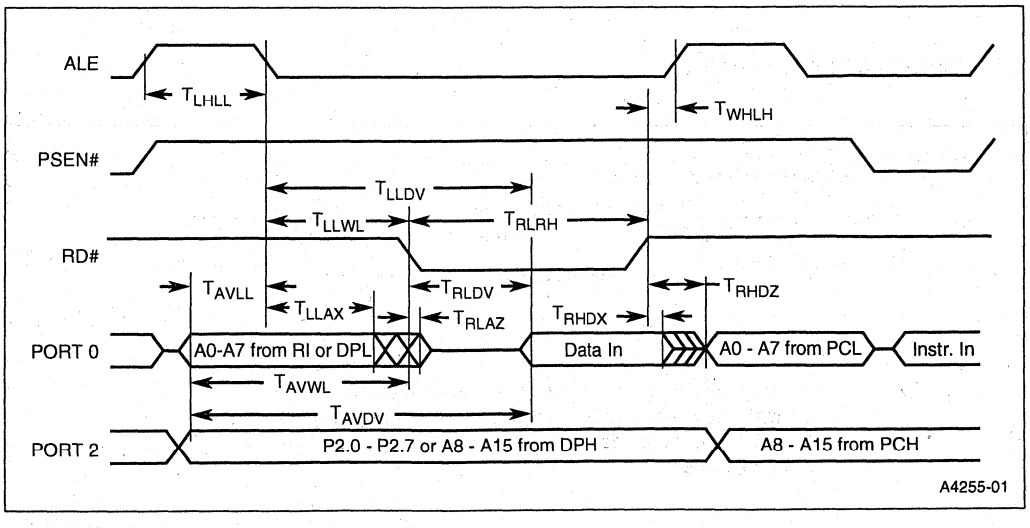
Symbol	Parameter	Min	Max	Unit
F_{OSC}	RCIN Frequency	4	6	MHz
T_{OSC}	1/Fosc	166.7	250	ns
T_{LHLL}	ALE Pulse Width	2Tosc - 50		ns
T_{AVLL}	Address Valid to ALE Low	Tosc - 50		ns
T_{LLAX}	Address Hold after ALE Low	Tosc - 40		ns
T_{LLIV}	ALE Low to Valid Instruction In		4Tosc - 80	ns
T_{LLPL}	ALE Low to PSEN# Low	Tosc - 40		ns
T_{PLPH}	Psen# Pulse Width	3Tosc - 60		ns
T_{PLIV}	Psen# Low to Valid Instruction In		3Tosc - 90	ns
T_{PXIX}	Input Instruction Hold after PSEN#	0		ns
T_{PXIZ}	Input Instruction Float after PSEN#		Tosc - 20	ns
T_{AVIV}	Address Valid to Valid Instruction In		5Tosc - 90	ns
T_{PLAZ}	Psen# Low to Address Float		20	ns
T_{RLRH}	RD# Pulse Width	6Tosc - 120		ns
T_{WLWH}	Write# Pulse Width	6Tosc - 120		ns
T_{RLDV}	RD# Low to Valid Data In		5Tosc - 150	ns
T_{RHDX}	Input Data Hold after RD# High	0		ns
T_{RHDZ}	Input Data Float after RD# High		2Tosc - 45	ns
T_{LLDV}	ALE Low to Valid Data In		8Tosc - 130	ns
T_{AVDV}	Address Valid to Valid Data In		9Tosc - 145	ns
T_{LLWL}	ALE Low to RD# or WR# Low	3Tosc - 70	3Tosc + 70	ns
T_{AVWL}	Address Valid to WR# Low	4Tosc - 150		ns
T_{QVWX}	Output Data Valid before WR#	Tosc - 70		ns
T_{QVWH}	Output Data Valid to WR# High	7Tosc - 170		ns
T_{WHQX}	Output Data Hold after WR# High	Tosc - 60		ns
T_{RLAZ}	RD# Low to Address Float		0	ns
T_{WHLH}	RD# or WR# High to ALE High	Tosc - 55	Tosc + 40	ns
T_{POR}	Power on reset internal high time (note 3)	80	260	ms

NOTE:
1. Capacitive loading=100pF
2. Rise time and fall time = 20ns for external clock drive
3. T_{POR} timing begins when the voltage exceeds the V_{POR} crossover voltage.

6.3 External Program Memory Read Cycle Waveform



6.4 External Program Memory Read Cycle External Data Memory Read Cycle Waveform



6.5 External Data Memory Read Cycle External Data Memory Write Cycle Waveform

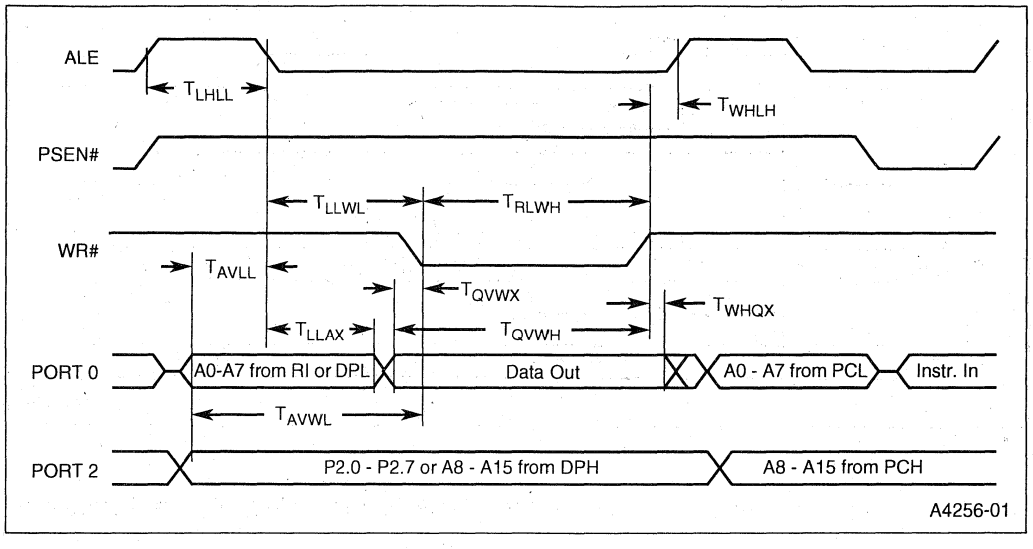


Figure 6. External Data Memory Write Cycle

6.6 Testing Characteristics

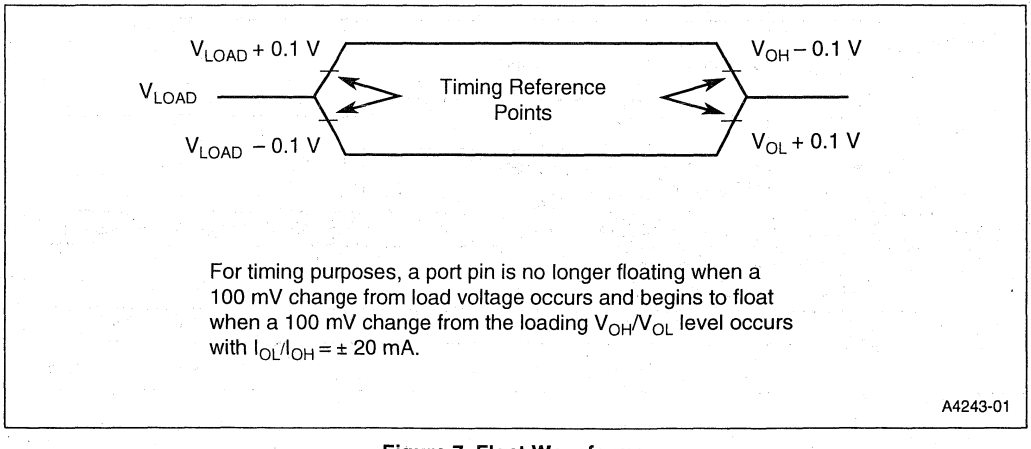
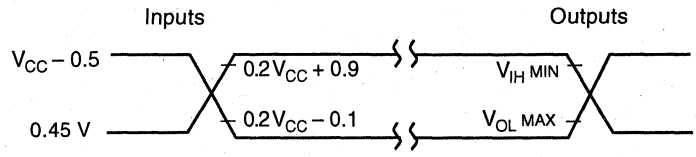


Figure 7. Float Waveforms



AC inputs during testing are driven at V_{CC} – 0.5V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at a min of V_{IH} for a logic 1 and V_{OL} for a logic 0.

A4244-01

6.7 A.C. Testing Input, Output Waveforms Signature Byte Information

Valid signature bytes for the 83C51KB are detailed in the following table:

Table 9. 83C51KB Signature Byte Values

TROM Address	Contents	Device Type
30H	89H	Intel Corp.
31H	58H	FX-core
60H	20H	83C51KB

8XC152JA/JB/JC/JD
UNIVERSAL COMMUNICATION CONTROLLER
8-BIT MICROCONTROLLER

- **8K Factory Mask Programmable ROM Available**

- **Superset of 80C51 Architecture**
- **Multi-Protocol Serial Communication I/O Port (2.048 Mbps/2.4 Mbps Max)**
  - **— SDLC/HDLC Only**
  - **— CSMA/CD and SDLC/HDLC**
  - **— User Definable Protocols**
- **Full Duplex/Half Duplex**
- **MCS®-51 Compatible UART**
- **16.5 MHz Maximum Clock Frequency**
- **Multiple Power Conservation Modes**
- **64KB Program Memory Addressing**
- **64KB Data Memory Addressing**
- **256 Bytes On-Chip RAM**
- **Dual On-Chip DMA Channels**
- **Hold/Hold Acknowledge**
- **Two General Purpose Timer/Counters**
- **5 or 7 I/O Ports**
- **56 Special Function Registers**
- **11 Interrupt Sources**
- **Available in 48 Pin Dual-in-Line Package and 68 Pin Surface Mount PLCC Package**
  (See Packaging Spec. Order #231369)

The 80C152, which is based on the MCS®-51 CPU, is a highly integrated single-chip 8-bit microcontroller designed for cost-sensitive, high-speed, serial communications. It is well suited for implementing Integrated Services Digital Networks (ISDN), emerging Local Area Networks, and user defined serial backplane applications. In addition to the multi-protocol communication capability, the 80C152 offers traditional microcontroller features for peripheral I/O interface and control.

Silicon implementations are much more cost effective than multi-wire cables found in board level parallel-to-serial and serial-to-parallel converters. The 83C152 contains, in silicon, all the features needed for the serial-to-parallel conversion. Other 83C152 benefits include: 1) better noise immunity through differential signaling or fiber optic connections, 2) data integrity utilizing the standard, designed in CRC checks, and 3) better modularity of hardware and software designs. All of these—cost, network parameter and real estate improvements—apply to 83C152 serial links between boards or systems and 83C152 serial links on a single board.

October 1989

Order Number: 270431-003

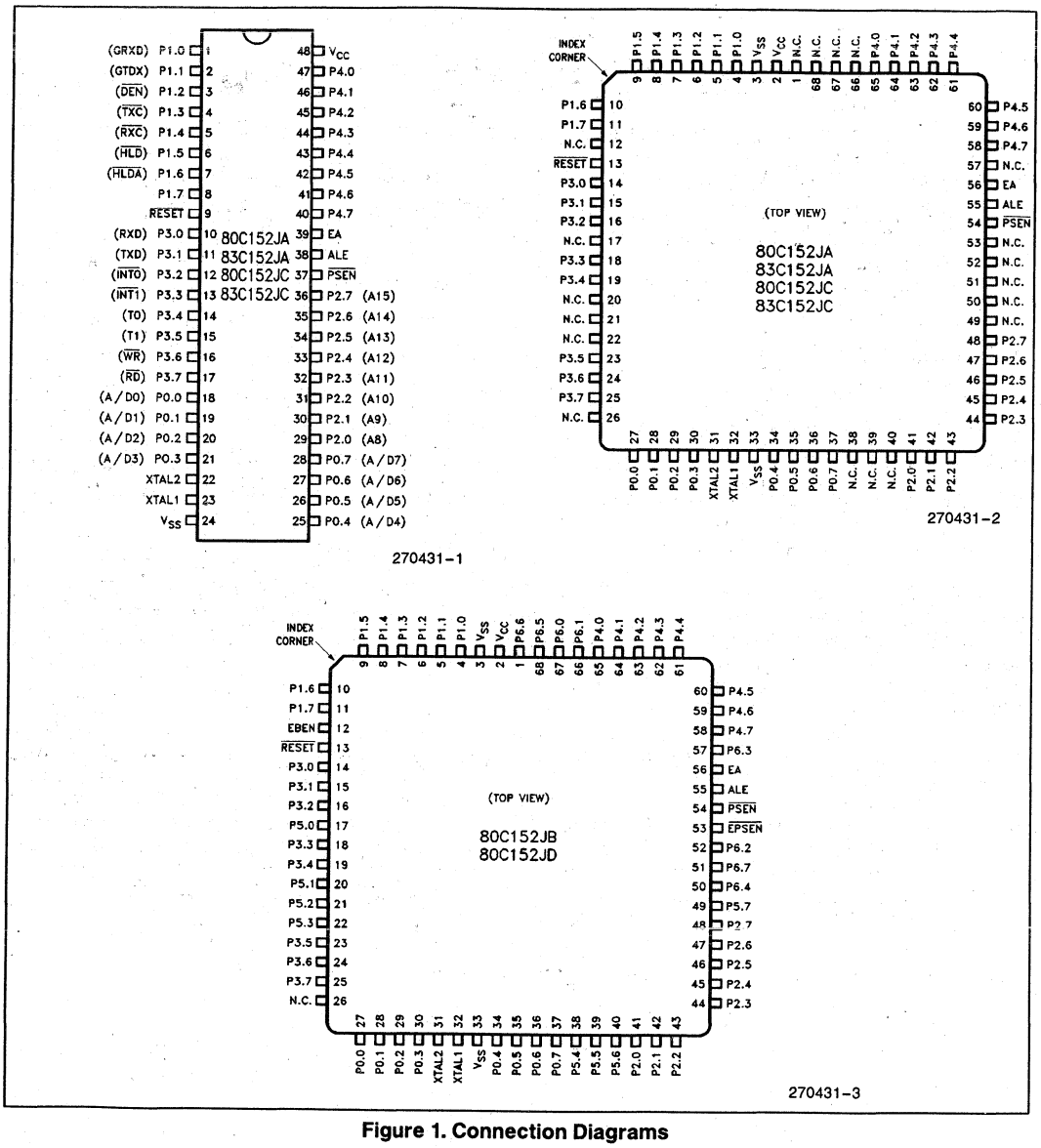


Figure 1. Connection Diagrams

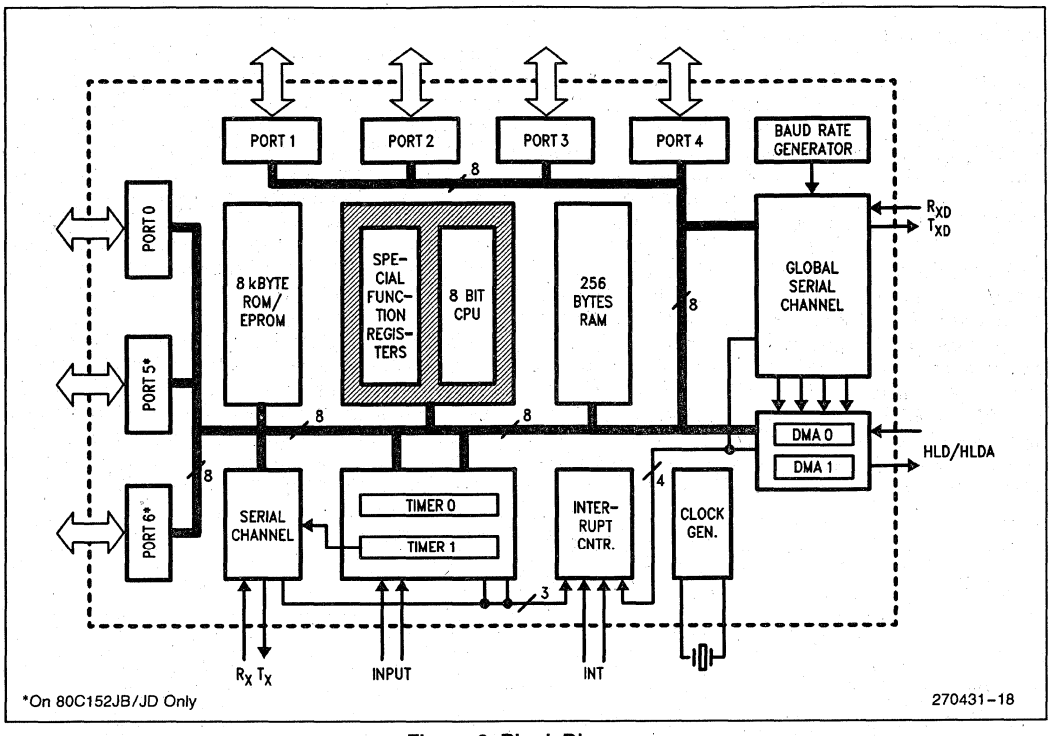


Figure 2. Block Diagram

80C152JB/JD General Description

The 80C152JB/JD is a ROMless extension of the 80C152 Universal Communication controller. The 80C152JB has the same five 8-bit I/O ports of the 80C152, plus an additional two 8-bit I/O ports, Port 5 and Port 6. The 80C152JB/JD also has two additional control pins, EBEN (**E**PROM **B**us **EN**able), and $\overline{\text{EPSEN}}$ (**E**PROM bus **P**rogram **S**tore **EN**able).

EBEN selects the functionality of Port 5 and Port 6. When EBEN is low, these ports are strictly I/O, similar to Port 4. The SFR location for Port 5 is 91H and Port 6 is 0A1H. This means Port 5 and Port 6 are not bit addressable. With EBEN low, all program memory fetches take place via Port 0 and Port 2. (The 80C152 is a ROMless only product). When EBEN is high, Port 5 and Port 6 form an address/data bus called the E-Bus (EPROM-Bus) for program memory operations.

$\overline{\text{EPSEN}}$ is used in conjunction with Port 5 and Port 6 program memory operations. $\overline{\text{EPSEN}}$ functions like $\overline{\text{PSEN}}$ during program memory operation, but supports Port 5 and Port 6. $\overline{\text{EPSEN}}$ is the read strobe to external program memory for Port 5 and Port 6. $\overline{\text{EPSEN}}$ is activated twice during each machine cycle unless an external data memory operation occurs on Port(s) 0 and Port 2. When external data memory is accessed the second activation of $\overline{\text{EPSEN}}$ is skipped, which is the same as when using $\overline{\text{PSEN}}$. Note that data memory fetches cannot be made through Ports 5 and 6.

When EBEN is high and EA is low, all program memory operations take place via Ports 5 and 6. The high byte of the address goes out on Port 6, and the low byte is output on Port 5. ALE is still used to latch the address on Port 5. Next, the op code is read on Port 5. The timing is the same as when using Ports 0 and 2 for external program memory operations.

Table 1. Program Memory Fetches

EBEN	$\overline{\text{EA}}$	Program Fetch via	$\overline{\text{PSEN}}$	$\overline{\text{EPSEN}}$	Comments
0	0	P0, P2	Active	Inactive	Addresses 0–0FFFFH
0	1	N/A	N/A	N/A	Invalid Combination
1	0	P5, P6	Inactive	Active	Addresses 0–0FFFFH
1	1	P5, P6 P0, P2	Inactive Active	Active Inactive	Addresses 0–1FFFH Addresses ≥ 2000H

Table 2. 8XC152 Product Differences

ROMless Version	CSMA/CD and HDLC/SDLC	HDLC/SDLC Only	ROM Version Available	PLCC and DIP	PLCC Only	5 I/O Ports	7 I/0 Ports
80C152JA	*		*(83C152JA)	*		*	
80C152JB	*				*		*
80C152JC		*	*(83C152JC)	*		*	
80C152JD		*			*		*

NOTES:
* = options available
0 standard frequency range 3.5 MHz to 12 MHz
0 "–1" frequency range 3.5 MHz to 16.5 MHz

<table>
<tr><th colspan="2">Pin #</th><th colspan="3">Pin Description</th></tr>
<tr><td>DIP</td><td>PLCC(1)</td><td colspan="3"></td></tr>
<tr><td>48</td><td>2</td><td colspan="3">V_{CC}—Supply voltage.</td></tr>
<tr><td>24</td><td>3,33(2)</td><td colspan="3">V_{SS}—Circuit ground.</td></tr>
<tr><td>18-21,
25-28</td><td>27-30,
34-37</td><td colspan="3">Port 0—Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.
Port 0 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled low. During accesses to external Data Memory, Port 0 always emits the low-order address byte and serves as the multiplexed data bus. In these applications it uses strong internal pullups when emitting 1s.
Port 0 also outputs the code bytes during program verification. External pullups are required during program verification.</td></tr>
<tr><td>1-8</td><td>4-11</td><td colspan="3">Port 1—Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.
Port 1 also serves the functions of various special features of the 8XC152, as listed below:
<table>
<tr><th>Pin</th><th>Name</th><th>Alternate Function</th></tr>
<tr><td>P1.0</td><td>GRXD</td><td>GSC data input pin</td></tr>
<tr><td>P1.1</td><td>GTXD</td><td>GSC data output pin</td></tr>
<tr><td>P1.2</td><td>$\overline{DEN}$</td><td>GSC enable signal for an external driver</td></tr>
<tr><td>P1.3</td><td>$\overline{TXC}$</td><td>GSC input pin for external transmit clock</td></tr>
<tr><td>P1.4</td><td>$\overline{RXC}$</td><td>GSC input pin for external receive clock</td></tr>
<tr><td>P1.5</td><td>$\overline{HLD}$</td><td>DMA hold input/output</td></tr>
<tr><td>P1.6</td><td>$\overline{HLDA}$</td><td>DMA hold acknowledge input/output</td></tr>
</table></td></tr>
<tr><td>29-36</td><td>41-48</td><td colspan="3">Port 2—Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.
Port 2 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled low. During accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR and DMA operations), Port 2 emits the high-order address byte. In these applications it uses strong internal pullups when emitting 1s.
During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.
Port 2 also receives the high-order address bits during program verification.</td></tr>
<tr><td>10- 17</td><td>14-16,
18, 19,
23-25</td><td colspan="3">Port 3—Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.
Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:
<table>
<tr><th>Pin</th><th>Name</th><th>Alternate Function</th></tr>
<tr><td>P3.0</td><td>RXD</td><td>Serial input line</td></tr>
<tr><td>P3.1</td><td>TXD</td><td>Serial output line</td></tr>
<tr><td>P3.2</td><td>$\overline{INT0}$</td><td>External Interrupt 0</td></tr>
<tr><td>P3.3</td><td>$\overline{INT1}$</td><td>External Interrupt 1</td></tr>
<tr><td>P3.4</td><td>T0</td><td>Timer 0 external input</td></tr>
<tr><td>P3.5</td><td>T1</td><td>Timer 1 external input</td></tr>
<tr><td>P3.6</td><td>$\overline{WR}$</td><td>External Data Memory Write strobe</td></tr>
<tr><td>P3.7</td><td>$\overline{RD}$</td><td>External Data Memory Read strobe</td></tr>
</table></td></tr>
</table>

Pin Description (Continued)

Pin #		Pin Description
47-40	65-58	**Port 4**—Port 4 is an 8-bit bidirectional I/O port with internal pullups. Port 4 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. In addition, Port 4 also receives the low-order address bytes during program verification.
9	13	**$\overline{RST}$**—Reset input. A logic low on this pin for three machine cycles while the oscillator is running resets the device. An internal pullup resistor permits a power-on reset to be generated using only an external capacitor to V_{SS}. Although the GSC recognizes the reset after three machine cycles, data may continue to be transmitted for up to 4 machine cycles after Reset is first applied.
38	55	**ALE**—Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. While in Reset, ALE remains at a constant high level.
37	54	**$\overline{PSEN}$**—Program Store Enable is the Read strobe to External Program Memory. When the 8XC152 is executing from external program memory, $\overline{PSEN}$ is active (low). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory. While in Reset, $\overline{PSEN}$ remains at a constant high level.
39	56	**$\overline{EA}$**—External Access enable. $\overline{EA}$ must be externally pulled low in order to enable the 8XC152 to fetch code from External Program Memory locations 0000H to 0FFFH. $\overline{EA}$ must be connected to V_{CC} for internal program execution.
23	32	**XTAL1**—Input to the inverting oscillator amplifier and input to the internal clock generating circuits.
22	31	**XTAL2**—Output from the inverting oscillator amplifier.
N/A	17, 20 21, 22 38, 39 40, 49	**Port 5**—Port 5 is an 8-bit bidirectional I/O port with internal pullups. Port 5 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 5 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 5 is also the multiplexed low-order address and data bus during accesses to external program memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	67, 66 52, 57 50, 68 1, 51	**Port 6**—Port 6 is an 8-bit bidirectional I/O port with internal pullups. Port 6 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 6 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups. Port 6 emits the high-order address byte during fetches from external Program Memory if EBEN is pulled high. In this application it uses strong pullups when emitting 1s.
N/A	12	**EBEN**—E-Bus Enable input that designates whether program memory fetches take place via Ports 0 and 2 or Ports 5 and 6. Table 1 shows how the ports are used in conjunction with EBEN.
N/A	53	**$\overline{EPSEN}$**—E-bus Program Store Enable is the Read strobe to external program memory when EBEN is high. Table 2 shows when $\overline{EPSEN}$ is used relative to $\overline{PSEN}$ depending on the status of EBEN and $\overline{EA}$.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

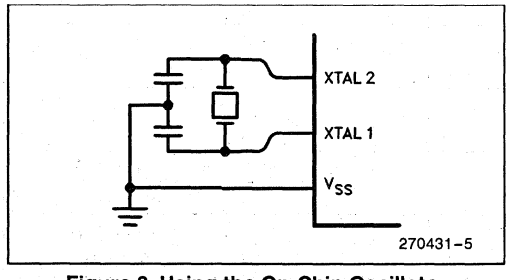


Figure 3. Using the On-Chip Oscillator

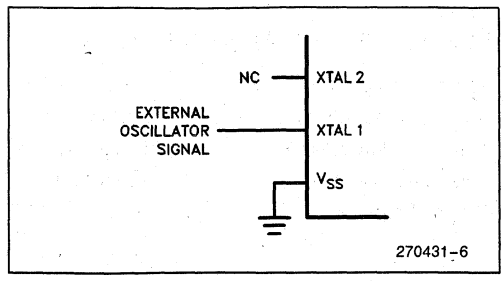


Figure 4. External Clock Drive

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while most of the on-chip peripherals remain active. The major peripherals that do not remain active during Idle, are the DMA channels. The Idle Mode is invoked by software. The content of the on-chip RAM and all the Special Function Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

POWER DOWN MODE

In Power Down Mode, the oscillator is stopped and all on-chip functions cease except that the on-chip RAM contents are maintained. The mode Power Down is invoked by software. The Power Down Mode can be terminated only by a hardware reset.

Table 3. Status of the External Pins During Idle and Power Down Modes

80C152JA/83C152JA/80C152JC/83C152JC

Mode	Program Memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4
Idle	Internal	1	1	Data	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data	Data
Power Down	Internal	0	0	Data	Data	Data	Data	Data
Power Down	External	0	0†	Float	Data	Data	Data	Data

80C152JB/80C152JD

Mode	Instruction Bus	ALE	$\overline{PSEN}$	$\overline{EPSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6
Idle	P0, P2	1	1	1	Float	Data	Address	Data	Data	0FFH	0FFH
Idle	P5, P6	1	1	1	Data	Data	Data	Data	Data	0FFH	Address
Power Down	P0, P2	0	0	1	Float	Data	Data	Data	Data	0FFH	0FFH
Power Down	P5, P6	0	1†	0	Data	Data	Data	Data	Data	0FFH	0FFH

NOTE:
For more detailed information on the reduced power modes refer to the Embedded Controller Handbook, and Application Note AP-252, "Designing with the 80C51BH."
†Note difference of logic level of $\overline{PSEN}$ during Power Down for ROM JA/JC and ROM emulation mode for JC/JD.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any pin to V_{SS} . . −0.5V to (V_{CC} + 0.5V)
Voltage on V_{CC} to VSS . . . . . −0.5V to +6.5V
Power Dissipation . . . . . 1.0W(9)

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V)

Symbol	Parameter	Min	Typ (Note 3)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (All Except $\overline{EA}$, EBEN)	−0.5		$0.2V_{CC}-0.1$	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$, EBEN)	−0.5		$0.2V_{CC}-0.3$	V	
V_{IH}	Input High Voltage (Except XTAL1, $\overline{RST}$)	$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, $\overline{RST}$)	$0.7V_{CC}$		$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3, 4, 5, 6)			0.45	V	I_{OL} = 1.6 mA (Note 4)
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$, $\overline{EPSEN}$)			0.45	V	I_{OL} = 3.2 mA (Note 4)
V_{OH}	Output High Voltage (Ports 1, 2, 3, 4, 5, 6 COMM9 ALE, $\overline{PSEN}$, $\overline{EPSEN}$)	2.4			V	I_{OH} = −60 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −10 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −400 μA V_{CC} = 5V ±10%
		$0.9V_{CC}$			V	I_{OH} = −40 μA (Note 5)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, 4, 5, 6)			−50	μA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3, 4, 5, 6)			−650	μA	V_{IN} = 2V
I_{LI}	Input Leakage (Port 0, $\overline{EA}$)			±10	μA	$0.45 < V_{IN} < V_{CC}$
RRST	Reset Pullup Resistor	40			kΩ	
I_{IH}	Logical 1 Input Current (EBEN)			+60	μA	
I_{CC}	Power Supply Current : Active (16.5 MHz) Idle (16.5 MHz) Power Down Mode		31 8 10	41.1 15.4	mA mA μA	(Note 6) (Note 6) V_{CC} = 2.0V to 5.5V

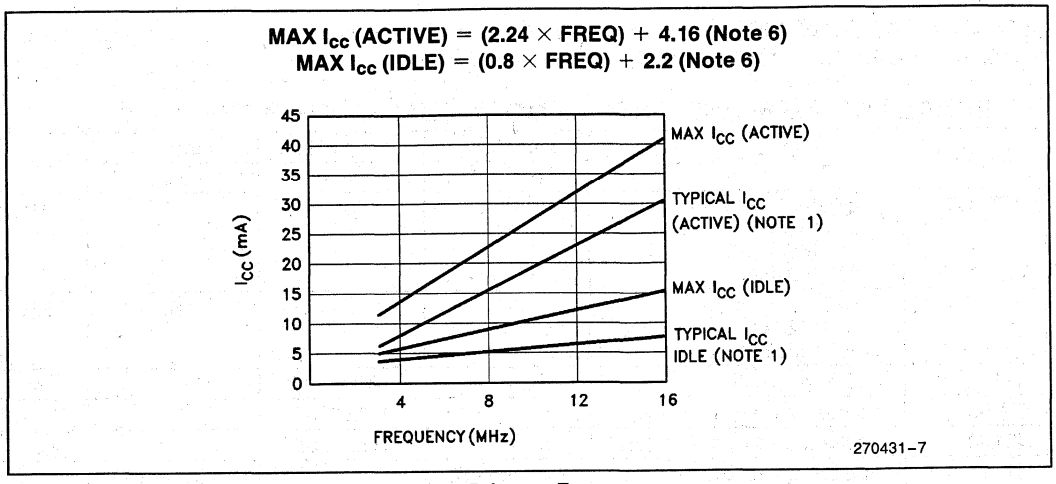


Figure 5. I_{CC} vs Frequency

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address.
C: Clock
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: $\overline{\text{PSEN}}$.
Q: Output data.
R: $\overline{\text{READ}}$ signal.
T: Time.
V: Valid.
W: $\overline{\text{WRITE}}$ signal.
X: No longer a valid logic level.
Z: Float.

For example,

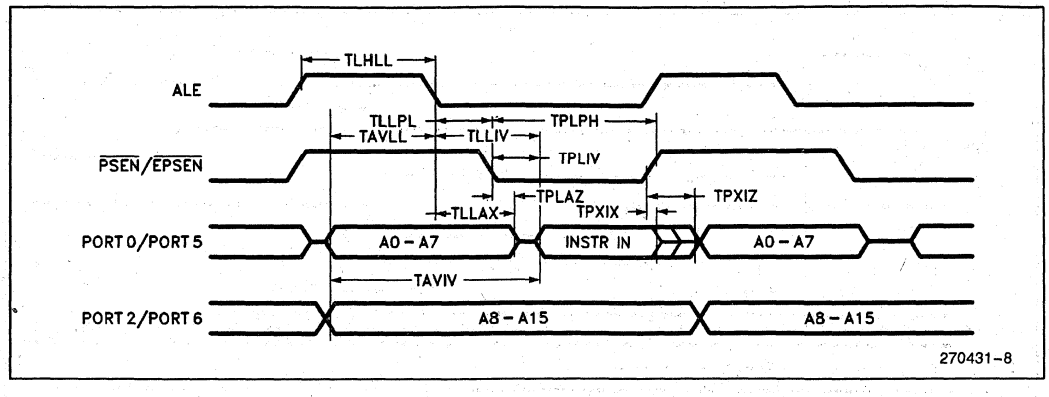
TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{\text{PSEN}}$ Low.

A.C. CHARACTERISTICS (T_A = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

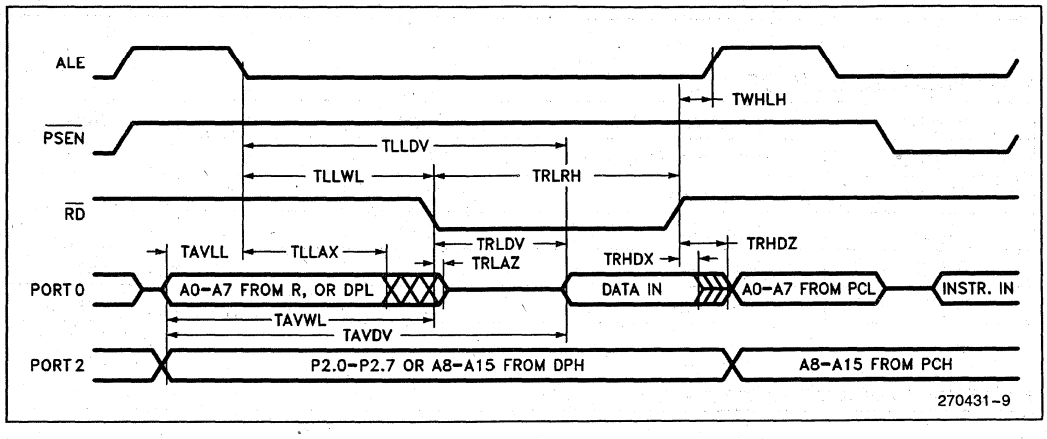
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS (Note 7, 10)

Symbol	Parameter	16.5 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 80C152JA/JC 83C152JA/JC 80C152JB/JD			3.5	12	MHz
	80C152JA/JC-1 83C152JA/JC-1 80C152JB/JD-1			3.5	16.5	MHz
TLHLL	ALE Pulse Width	81		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	5		TCLCL-55		ns
TLLAX	Address Hold After ALE Low	25		TCLCL-35		ns
TLLIV	ALE Low to Valid Instruction In		142		4TCLCL-100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	20		TCLCL-40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	137		3TCLCL-45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		77		3TCLCL-105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		35		TCLCL-25	ns
TAVIV	Address to Valid Instruction In		198		5TCLCL-105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	263		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	263		6TCLCL-100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		138		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		51		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		335		8TCLCL-150	ns
TAVDV	Address to Valid Data In		380		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	132	232	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	112		4TCLCL-130		ns
TQVWX(8)	Data Valid to $\overline{WR}$ Transition	196		6TCLCL-167		ns
TWHQX	Data Hold After $\overline{WR}$	10		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	20	100	TCLCL-40	TCLCL+40	ns

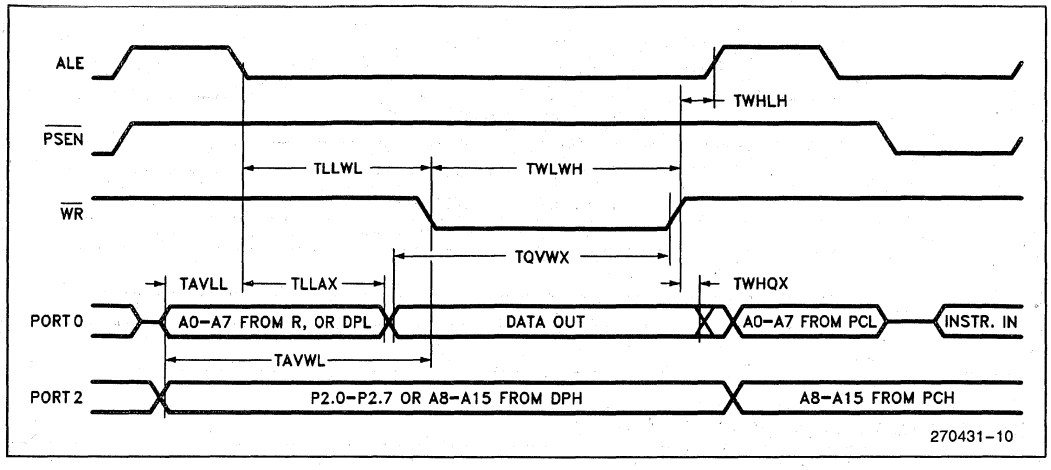
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



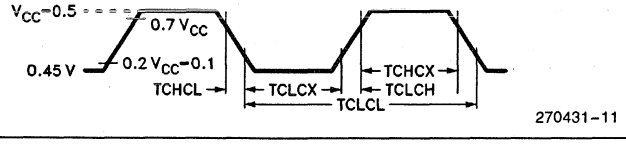
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	16.5	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

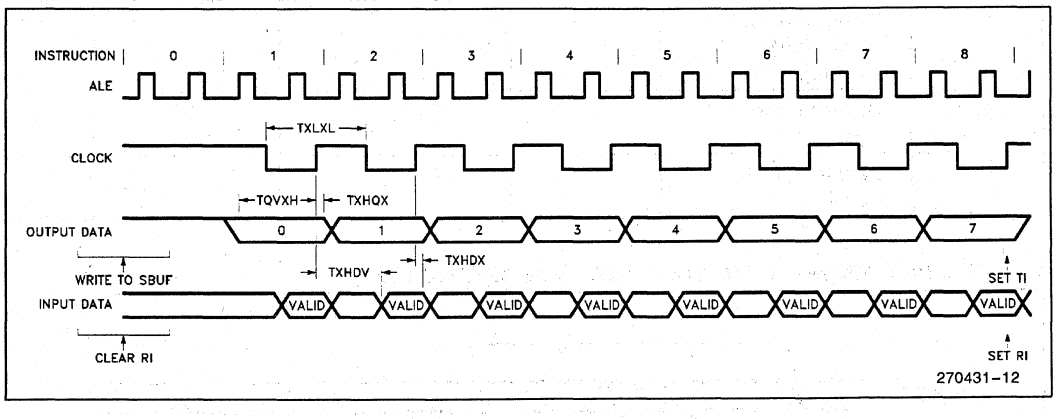
EXTERNAL CLOCK DRIVE WAVEFORM



LOCAL SERIAL CHANNEL TIMING—SHIFT REGISTER MODE

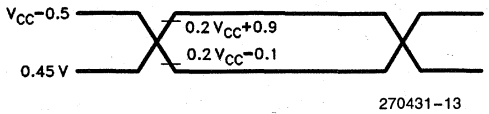
Symbol	Parameter	16.5 MHz		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	727		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	473		10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	4		2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		473		10TCLCL-133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS



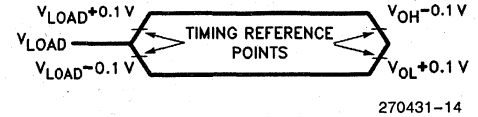
A.C. TESTING:

INPUT, OUTPUT WAVEFORMS



AC Inputs During Testing are Driven at $V_{CC}-0.5$ for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at V_{IH} Min for a Logic "1" and V_{IL} Max for a Logic "0".

FLOAT WAVEFORM

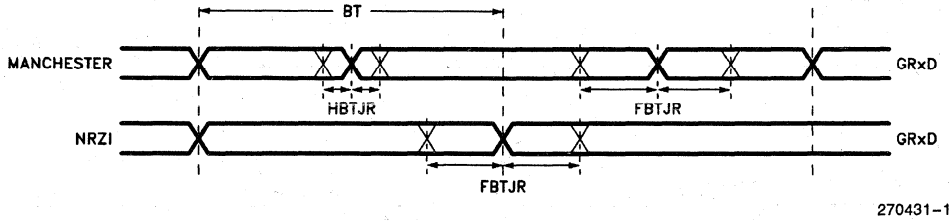


For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs, and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \geq \pm 20$ mA.

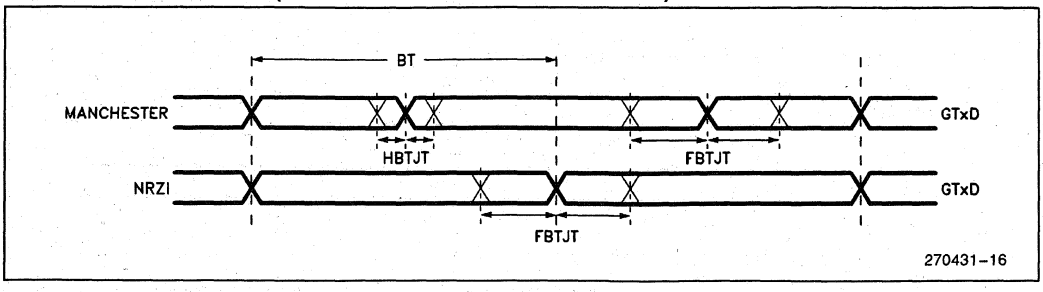
GLOBAL SERIAL PORT TIMINGS—Internal Baud Rate Generator

Symbol	Parameter	16.5 MHz (BAUD = 0)		Variable Oscillator		Unit
		Min	Max	Min	Max	
HBTJR	Allowable jitter on the Receiver for ½ bit time (Manchester encoding only)		0.0375		(0.125 × (BAUD+1)× 8TCLCL) −25 ns	μs
FBTJR	Allowable jitter on the Receiver for one full bit time (NRZI and Manchester)		0.10		(0.25 × (BAUD+1)× 8TCLCL) −25 ns	μs
HBTJT	Jitter of data from Transmitter for ½ bit time (Manchester encoding only)		±10		±10	ns
FBTJT	Jitter of data from Transmitter for one full bit time (NRZI and Manchester)		±10		±10	ns
DRTR	Data rise time for Receiver(11)		20		20	ns
DFTR	Data fall time for Receiver(12)		20		20	ns

GSC RECEIVER TIMINGS (INTERNAL BAUD RATE GENERATOR)



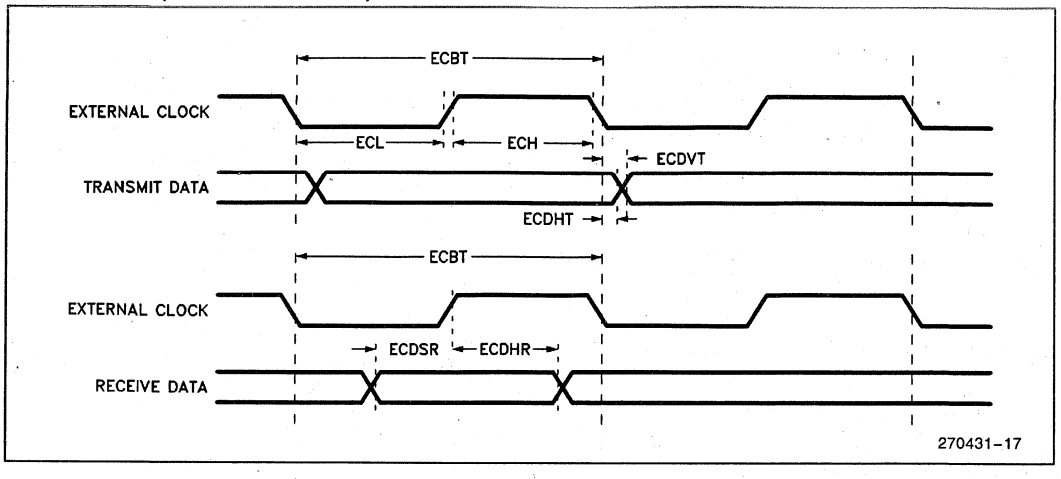
GSC TRANSMIT TIMINGS (INTERNAL BAUD RATE GENERATOR)



GLOBAL SERIAL PORT TIMINGS—External Clock

Symbol	Parameter	16.5 MHz		Variable Oscillator		Unit
		Min	Max	Min	Max	
1/ECBT	GSC Frequency with an External Clock		2.4	0.009	$F_{OSC} \times 0.145$	MHz
ECH	External Clock High	170		2TCLCL + 45 ns		ns
ECL(13)	External Clock Low	170		2TCLCL + 45 ns		ns
ECRT	External Clock Rise Time(11)		20		20	ns
ECFT	External Clock Fall Time(12)		20		20	ns
ECDVT	External Clock to Data Valid Out - Transmit (to External Clock Negative Edge)		150		150	ns
ECDHT	External Clock Data Hold - Transmit (to External Clock Negative Edge)	0		0		ns
ECDSR	External Clock Data Set-up - Receiver (to External Clock Positive Edge)	45		45		ns
ECDHR	External Clock to Data Hold - Receiver (to External Clock Positive Edge)	50		50		ns

GSC TIMINGS (EXTERNAL CLOCK)



NOTES:

1. N.C. pins on PLCC package may be connected to internal die and should not be used in customer applications.
2. It is recommended that both Pin 3 and Pin 33 be grounded for PLCC devices.
3. "Typicals" are based on samples taken from early manufacturing lots and are not guaranteed. The measurements were made with V_{CC} = 5V at room temperature.
4. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
5. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
6. I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; Port 0 pins connected to V_{CC}. "Operating" current is measured with $\overline{EA}$ connected to V_{CC} and $\overline{RST}$ connected to V_{SS}. "Idle" current is measured with $\overline{EA}$ connected to V_{SS}, $\overline{RST}$ connected to V_{CC} and GSC inactive.
7. The specifications relating to external data memory characteristics are also applicable to DMA operations.
8. TQVWX should not be confused with TQVWX as specified for 80C51BH. On 80C152, TQVWX is measured from data valid to rising edge of $\overline{WR}$. On 80C51BH, TQVWX is measured from data valid to falling edge of $\overline{WR}$. See timing diagrams.
9. This value is based on the maximum allowable die temperature and the thermal resistance of the package.
10. All specifications relating to external program memory characteristics are applicable to:
    $\overline{EPSEN}$ for $\overline{PSEN}$
    Port 5 for Port 0
    Port 6 for Port 2
    when EBEN is at a Logical 1 on the 80C152JB/JD.
11. Same as TCLCH, use External Clock Drive Waveform.
12. Same as TCHCL, use External Clock Drive Waveform.
13. When using the same external clock to drive both the receiver and transmitter, the minimum ECL spec effectively becomes 195 ns at all frequencies (assuming 0 ns propagation delay) because ECDVT (150 ns) plus ECDSR (45 ns) requirements must also be met (150 + 45 = 195 ns). The 195 ns requirement would also increase to include the maximum propagation delay between receivers and transmitters.

DESIGN NOTES

Within the 8XC152 there exists a race condition that may set both the RDN and AE bits at the end of a valid reception. This will not cause a problem in the application as long as the following steps are followed:

—Never give the receive error interrupt a higher priority than the valid reception interrupt

—Do not leave the valid reception interrupt service routine when AE is set by using a RETI instruction until AE is cleared. To clear AE set the GREN bit, this enables the receiver. If the user desires that the receiver remain disabled, clear GREN after setting it before leaving the interrupt service routine.

—If the AE bit is checked by user software in response to a valid reception interrupt, the status of AE should be considered invalid.

The race condition is dependent upon both the temperature that the device is currently operating at and the processing the device received during the wafer fabrication.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

DATA SHEET REVISION SUMMARY

The following represent the key differences between the "-003" and the "-002" version of the 80C152/83C152 data sheet. Please review this summary carefully.

1. Removed minimum GSC frequency spec when used with an external clock.
2. Change figure "External Program Memory Read Cycle" to show Port 0/Port 5 address floating after PSEN goes low.
3. Added design note on terminating idle with reset.
4. Added status of PSEN during Power Down mode to Table 3.
5. Moved all notes to back of data sheet.
6. Changed microcomputer to microcontroller.
7. Added External Oscillator start-up capacitance note.

The following represent the key differences between the "-002" and the "-001" version of the 80C152/83C152 data sheet. Please review this summary carefully.

1. Status of data sheet changed from "ADVANCED" to "PRELIMINARY".
2. 80C152JC, 83C152JC, and 80C152JD were added.
3. Added AE/RDN design note.
4. This revision summary was added.
5. Note #13 was added (Effective ECL spec at higher clock rates).
6. Table #2 changed to Table #3 (Status of pins during Idle/Power Down).
7. Current Table #2 was added (JA vs. JB vs. JC vs. JD matrix).
8. Transmit jitter spec changed from ±35 ns and ±70 ns to ±10 ns.

intel®

2

MCS®251 Microcontroller Family

8XC151SA/SB HIGH-PERFORMANCE CHMOS MICROCONTROLLER

Commercial/Express

- MCS® 51 Microcontroller Compatible Instruction Set
- Pin Compatible with 44-lead PLCC and 40-lead PDIP MCS 51 Sockets
- Fast Instruction Pipeline
- 16-bit Internal Code Fetch
- 8-bit, Min 2-clock External Code Fetch in Page Mode
- User-selectable Configurations:
  - External Wait States (0-3 wait states)
  - Page Mode
- 64K External Code Memory Space
- 64K External Data Memory Space
- ROM/OTPROM Options: 8 Kbytes (SA), 16 Kbytes (SB) or without ROM/OTPROM
- 256 Bytes On-Chip RAM
- Power Management
  - Idle Mode
  - Powerdown Mode
- 32 Programmable I/O Lines
- Seven Maskable Interrupt Sources with Four Programmable Priority Levels
- Three Flexible 16-bit Timer/counters
- Hardware Watchdog Timer
- Programmable Counter Array
  - High-speed Output
  - Compare/Capture Operation
  - Pulse Width Modulator
  - Watchdog Timer
- Programmable Serial I/O Port
  - Framing Error Detection
  - Automatic Address Recognition
- High-performance CHMOS Technology
- Static Standby to 16-MHz Operation
- Package Options (PDIP, PLCC)

The 8XC151SA/SB has an MCS 51 microcontroller compatible instructon set. It is available in 40-pin PDIP and 44-lead PLCC compatible with the MCS 51 microcontroller. The 8XC151SA/SB has 256 bytes of on-chip RAM and is available in 8/16 Kbytes of on-chip ROM/OTPROM or without ROM/OTPROM. A variety of new features such as programmable wait states, page mode and extended ALE can be selected using the new user-programmable configuration.

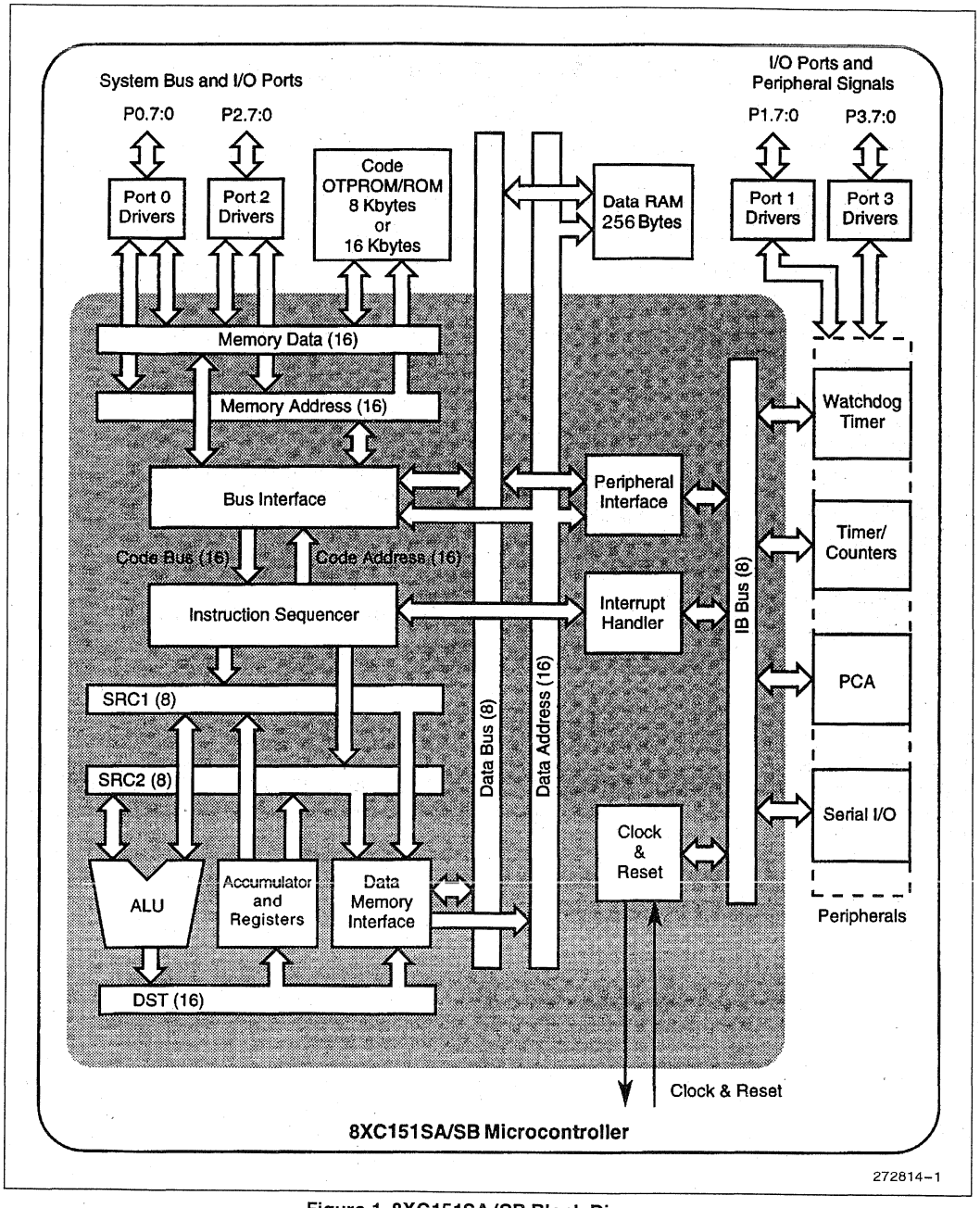


Figure 1. 8XC151SA/SB Block Diagram

TEMPERATURE RANGE

With the commercial (standard) temperature option, the device operates over the temperature range 0°C to +70°C. The express temperature option provides −40°C to +85°C device operation.

PROLIFERATION OPTIONS

Table 1 lists the proliferation options. See Figure 2 for the 8XC151SA/SB family nomenclature.

Table 1. Proliferation Options

8XC151SA/SB (0 MHz–16 MHz; 5V ± 10%)	
80C151SB	CPU-only
83C151SA	8K ROM
83C151SB	16K ROM
87C151SA	8K OTPROM
87C151SB	16K OTPROM

PROCESS INFORMATION

This device is manufactured on a complimentary high-performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 2. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
44-Lead PLCC	46°C/W	16°C/W
40-Pin PDIP	45°C/W	16°C/W

PACKAGE OPTIONS

Table 3 lists the 8XC151SA/SB packages.

Table 3. Package Information

Pkg.	Definition	Temperature
N	44-Lead PLCC	0°C to +70°C
P	40-Pin Plastic DIP	0°C to +70°C
TN	44-Lead PLCC	−40°C to +85°C
TP	40-Pin Plastic DIP	−40°C to +85°C

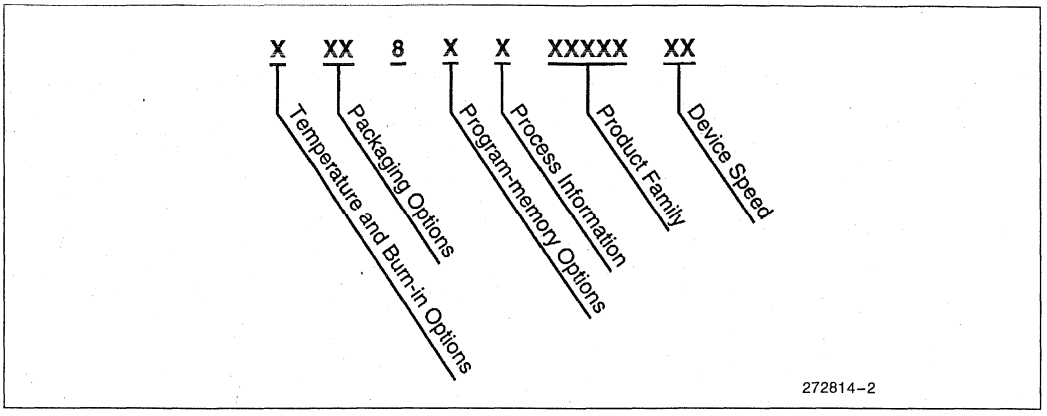


Figure 2. The 8XC151SA/SB Family Nomenclature

Table 4. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
	T	Express operating temperature range (−40°C to 85°C) with Intel standard burn-in.
Packaging Options	N	44-lead Plastic Leaded Chip Carrier (PLCC)
	P	40-pin Plastic Dual In-line Package (PDIP)
Program Memory Options	0	Without ROM/OTPROM
	3	ROM
	7	User programmable OTPROM
Process Information	C	CHMOS
Product Family	151	8-bit controller architecture
Device Memory Options	SA/SB	256 bytes RAM/8/16 Kbyte ROM/OTPROM or without ROM/OTPROM
Device Speed	16	External clock frequency

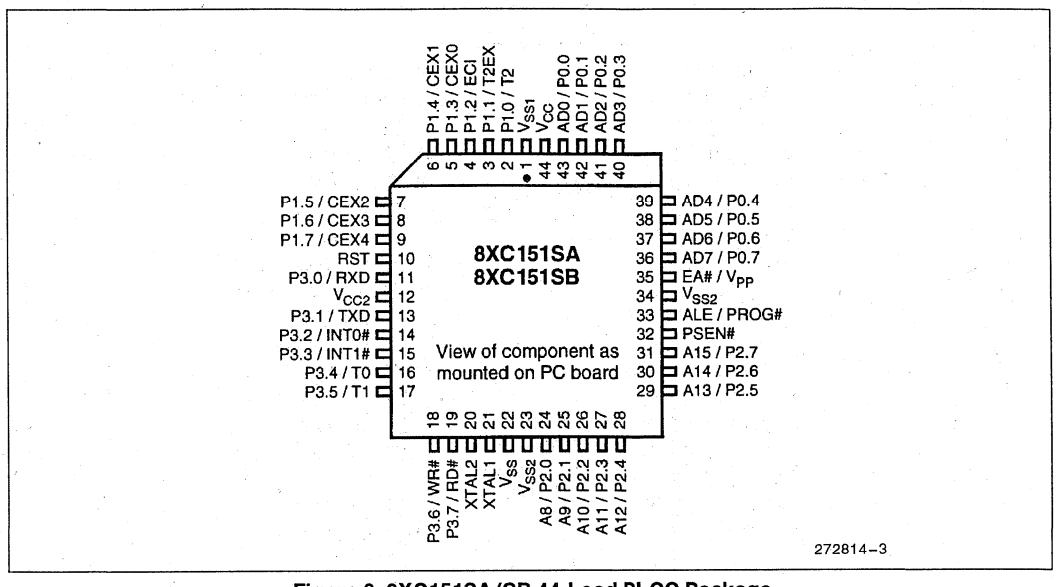


Figure 3. 8XC151SA/SB 44-Lead PLCC Package

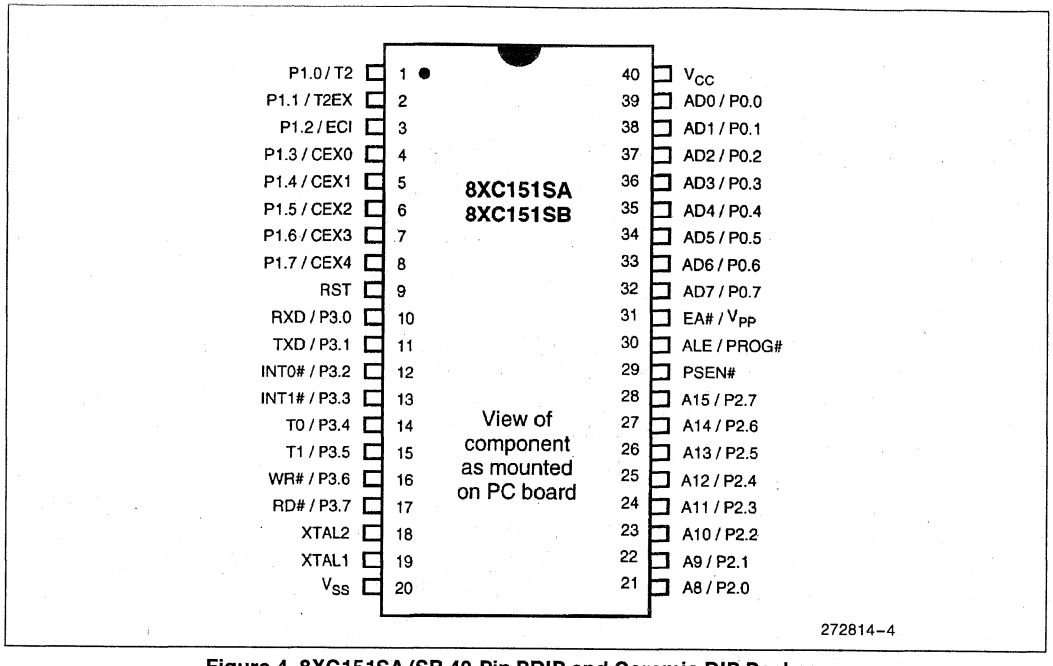


Figure 4. 8XC151SA/SB 40-Pin PDIP and Ceramic DIP Packages

Table 5. PLCC/DIP Signal Assignment Arranged by Functional Categories

Address & Data		
Name	**PLCC**	**DIP**
AD0/P0.0	43	39
AD1/P0.1	42	38
AD2/P0.2	41	37
AD3/P0.3	40	36
AD4/P0.4	39	35
AD5/P0.5	38	34
AD6/P0.6	37	33
AD7/P0.7	36	32
A8/P2.0	24	21
A9/P2.1	25	22
A10/P2.2	26	23
A11/P2.3	27	24
A12/P2.4	28	25
A13/P2.5	29	26
A14/P2.6	30	27
A15/P2.7	31	28

Processsor Control		
Name	**PLCC**	**DIP**
P3.2/INT0#	14	12
P3.3/INT1#	15	13
EA#/V_{PP}	35	31
RST	10	9
XTAL1	21	18
XTAL2	20	19

Input/Output		
Name	**PLCC**	**DIP**
P1.0/T2	2	1
P1.1/T2EX	3	2
P1.2/ECI	4	3
P1.3/CEX0	5	4
P1.4/CEX1	6	5
P1.5/CEX2	7	6
P1.6/CEX3	8	7
P1.7/CEX4	9	8
P3.0/RXD	11	10
P3.1/TXD	13	11
P3.4/T0	16	14
P3.5/T1	17	15

Power & Ground		
Name	**PLCC**	**DIP**
V_{CC}	44	40
V_{CC2}	12	—
V_{SS}	22	20
V_{SS1}	1	—
V_{SS2}	23, 34	—
EA#/V_{PP}	35	31

Bus Control & Status		
Name	**PLCC**	**DIP**
P3.6/WR#	18	16
P3.7/RD#	19	17
ALE/PROG#	33	30
PSEN#	32	29

Table 6. Signal Assignments Arranged by Package Number

PLCC	DIP	Name
1	—	V_{SS1}
2	1	P1.0/T2
3	2	P1.1/T2EX
4	3	P1.2/ECI
5	4	P1.3/CEX0
6	5	P1.4/CEX1
7	6	P1.5/CEX2
8	7	P1.6/CEX3
9	8	P1.7/CEX4
10	9	RST
11	10	P3.0/RXD
12	—	V_{CC2}
13	11	P3.1/TXD
14	12	P3.2/INT0#
15	13	P3.3/INT1#
16	14	P3.4/T0
17	15	P3.5/T1
18	16	P3.6/WR#
19	17	P3.7/RD#
20	18	XTAL2
21	19	XTAL1
22	20	V_{SS}

PLCC	DIP	Name
23	—	V_{SS2}
24	21	A8/P2.0
25	22	A9/P2.1
26	23	A10/P2.2
27	24	A11/P2.3
28	25	A12/P2.4
29	26	A13/P2.5
30	27	A14/P2.6
31	28	A15/P2.7
32	29	PSEN#
33	30	ALE/PROG#
34	—	V_{SS2}
35	31	EA#/V_{pp}
36	32	AD7/P0.7
37	33	AD6/P0.6
38	34	AD5/P0.5
39	35	AD4/P0.4
40	36	AD3/P0.3
41	37	AD2/P0.2
42	38	AD1/P0.1
43	39	AD0/P0.0
44	40	V_{CC}

SIGNAL DESCRIPTIONS

Table 7. Signal Descriptions

Signal Name	Type	Description	Multiplexed With
A15:8†	O	**Address Lines.** Upper address lines for the external bus.	P2.7:0
AD7:0†	I/O	**Address/Data Lines.** Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable.** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	PROG#
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Pins.** These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.6:3 P1.7
EA#	I	**External Access.** Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is to on-chip ROM/OTPROM if the address is within the range of the on-chip ROM/OTPROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM/OTPROM, EA# must be strapped to ground.	V_{PP}
ECI	I	**PCA External Clock Input.** External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1.** These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
PROG#	I	**Programming Pulse.** The programming pulse is applied to this pin for programming the on-chip OTPROM.	ALE
P0.7:0	I/O	**Port 0.** This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1.** This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI CEX3:0 CEX4
P2.7:0	I/O	**Port 2.** This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3.** This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#
PSEN#	O	**Program Store Enable.** Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte UCONFIG0.	—
RD#	O	**Read.** Read signal output to external data memory.	P3.7
RST	I	**Reset.** Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this pin and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data.** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
T1:0	I	**Timer 1:0 External Clock Inputs.** When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output.** For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input.** In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data.** TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
V_{CC}	PWR	**Supply Voltage.** Connect this pin to the +5V supply voltage.	—
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this pin to the +5V supply voltage is recommended. However, when using the 8XC151SA/SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—
V_{PP}	I	**Programming Supply Voltage.** The programming supply voltage is applied to this pin for programming the on-chip OTPROM.	EA#

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
V_{SS}	GND	**Circuit Ground.** Connect this pin to ground.	—
V_{SS1}	GND	**Secondary Ground.** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC151SA/SB as a pin-for-pin replacement for the 8XC51BH, V_{SS1} can be unconnected without loss of compatibility. (Not available on DIP)	
V_{SS2}	GND	**Secondary Ground 2.** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC151SA/SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	
WR#	O	**Write.** Write signal output to external memory.	P3.6
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier.** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier.** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	—

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias:
- Commercial ..... 0°C to +70°C
- Express ..... −40°C to +85°C

Storage Temperature ..... −65°C to +150°C

Voltage on EA#/V_{PP} Pin to V_{SS} ..... 0V to +13.0V

Voltage on Any other Pin to V_{SS} ... −0.5V to +6.5V

I_{OL} per I/O Pin ..... 15 mA

Power Dissipation 1.5W

NOTE:

Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias):
- Commercial ..... 0°C to +70°C
- Express ..... −40°C to +85°C

V_{CC} (Digital Supply Voltage) ..... 4.5V to 5.5V

V_{SS} 0V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC CHARACTERISTICS

Parameter values apply to all devices unless otherwise indicated.

Table 8. DC Characteristics at V_{CC} = 4.5V – 5.5V

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	−0.5		$0.2V_{CC} - 0.1$	V	
V_{IL1}	Input Low Voltage (EA#)	0		$0.2V_{CC} - 0.3$	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 μA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (Note 1, Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (Note 1, Note 2)
V_{OH}	Output High Voltage (Port 1, 2, 3, ALE, PSEN#)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	I_{OH} = −10 μA I_{OH} = −30 μA I_{OH} = −60 μA (Note 3)

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   port 0 26 mA
   ports 1–3 15 mA
   Maximum Total I_{OL} for
   all output pins 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.

Table 8. DC Characteristics at V_{CC} = 4.5V – 5.5V (Continued)

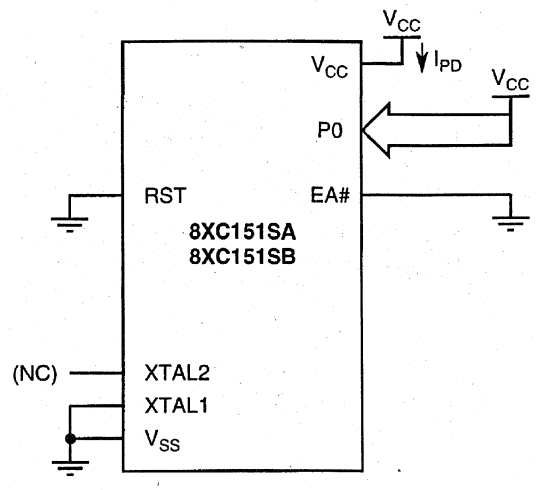
Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = –200 μA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
V_{OH2}	Output High Voltage (Port 2 in External Address during Page Mode)	V_{CC} –0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = –200 μA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)			–50	μA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45< V_{IN} < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Port 1, 2, 3)			–650	μA	V_{IN} = 2.0V
R_{RST}	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10 (Note 4)		pF	F_{OSC} = 16 MHz T_A = 25°C
I_{PD}	Powerdown Current		10 (Note 4)	< 20	μA	
I_{DL}	Idle Mode Current 83C151SA/SB, 87C151SA/SB 80C151SB		 12 (Note 4) 12 (Note 4)	 20 20	mA	F_{OSC} = 16 MHz
I_{CC}	Operating Current 83C151SA/SB, 87C151SA/SB 80C151SB		 73 (Note 4) 65 (Note 4)	 85 75	mA	F_{OSC} = 16 MHz

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

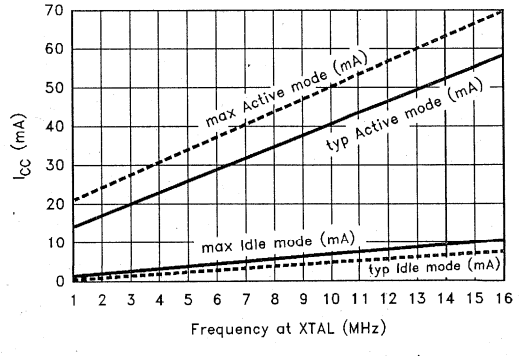
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   port 0 26 mA
   ports 1–3 15 mA
   Maximum Total I_{OL} for
   all output pins 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.



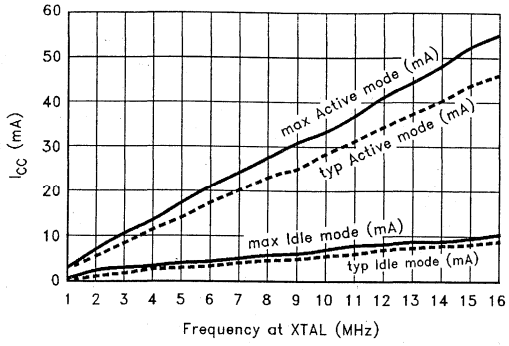
All other 8XC151SA/SB pins are unconnected.

Figure 5. I_{PD} Test Condition, Powerdown Mode, V_{CC} = 2.0V – 5.5V



These graphs are plotted for reference only and the values are not guaranteed.

Figure 6. I_{CC} vs Frequency (MHz) for 83C151SA/SB and 87C151SA/SB



272814-19

These graphs are plotted for reference only and the values are not guaranteed.

Figure 7. I_{CC} vs Frequency (MHz) for 80C151SB

AC Characteristics

Table 8 lists AC timing parameters for the 8XC151SA/SB with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and/or by extending ALE. In the table, Notes 3 and 5 mark parameters affected by an ALE wait state, and Notes 4 and 5 mark parameters affected by a PSEN#/RD#/WR# wait state.

Figures 5–13 show the bus cycles with the timing parameters.

Table 9. AC Characteristics (Capacitive Loading = 50 pF)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
F_{OSC}	XTAL1 Frequency	N/A	N/A	0	16	MHz
T_{OSC}	$1/F_{OSC}$ @ 12 MHz @ 16 MHz	N/A	N/A	 83.3 62.5		ns
T_{LHLL}	ALE Pulse Width @ 12 MHz @ 16 MHz	 70.3 49.5		 (1+2M) T_{OSC} − 13		ns (3)
T_{AVLL}	Address Valid to ALE Low @ 12 MHz @ 16 MHz	 58.3 37.5		 (1+2M) T_{OSC} − 25		ns (3)
T_{LLAX}	Address Hold after ALE Low @ 12 MHz @ 16 MHz	 15 15		 15		ns
T_{RLRH} (2)	RD# or PSEN# Pulse Width @ 12 MHz @ 16 MHz	 146.6 105		 2(1+N) T_{OSC} − 20		ns (4)
T_{WLWH}	WR# Pulse Width @ 12 MHz @ 16 MHz	 146.6 105		 2(1+N) T_{OSC} − 20		ns (4)
T_{LLRL} (2)	ALE Low to RD# or PSEN# Low @ 12 MHz @ 16 MHz	 58.3 37.5		 Tosc − 25		ns
T_{LHAX}	ALE High to Address Hold @ 12 MHz @ 16 MHz	 83.3 62.5		 (1+2M) T_{OSC}		ns (3)

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M = Number of wait states (0 or 1) for ALE.
4. In the formula, N = Number of wait states (0, 1, 2, or 3) for RD#/PSEN#/WR#.
5. "Typical" specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max Fosc (1)		Fosc Variable		Units
		Min	Max	Min	Max	
T_{RLDV} (2)	RD#/PSEN# Low to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 111.6 70		 2(1+N) T_{OSC} − 55	ns (4)
T_{RHDX} (2)	RD#/PSEN# Data/Instruction Hold after RD# and PSEN# High	0		0		ns
T_{RLAZ} (2)	RD#/PSEN# Low to Address Float	Typ. = 0 (5)	2	Typ. = 0 (5)	2	ns
T_{RHDZ1}	Instruction Float after RD#/PSEN# High Commercial @ 12 MHz and 16 MHz Express @ 12 MHz and 16 MHz	 Typ. = 20 Typ. = 18	 18 10	 Typ. = 20 Typ. = 18	 18 10	ns
T_{RHDZ2}	Data Float after RD#/PSEN# High @ 12 MHz @ 16 MHz		 151.6 110		 $2T_{OSC}$ −15	ns
T_{RHLH1}	RD#/PSEN# High to ALE High (Instruction) @ 12 MHz @ 16 MHz	 7 7	 Typ. = 17	 0	 Typ. = 17	ns
T_{RHLH2}	RD#/PSEN# High to ALE High (Data) @ 12 MHz @ 16 MHz	 156.6 115		 $2T_{OSC}$ − 10		ns
T_{WHLH}	WR# High to ALE High @ 12 MHz @ 16 MHz	 166.6 125		 $2T_{OSC}$		ns
T_{AVDV1}	Address (P0) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 248.2 165		 4(1+M/2) T_{OSC} − 85	ns (3)
T_{AVDV2}	Address (P2) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 268.2 185		 4(1+M/2) T_{OSC} − 65	ns (3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In @ 12 MHz @ 16 MHz		 116.6 75		 $2T_{OSC}$ −50	ns

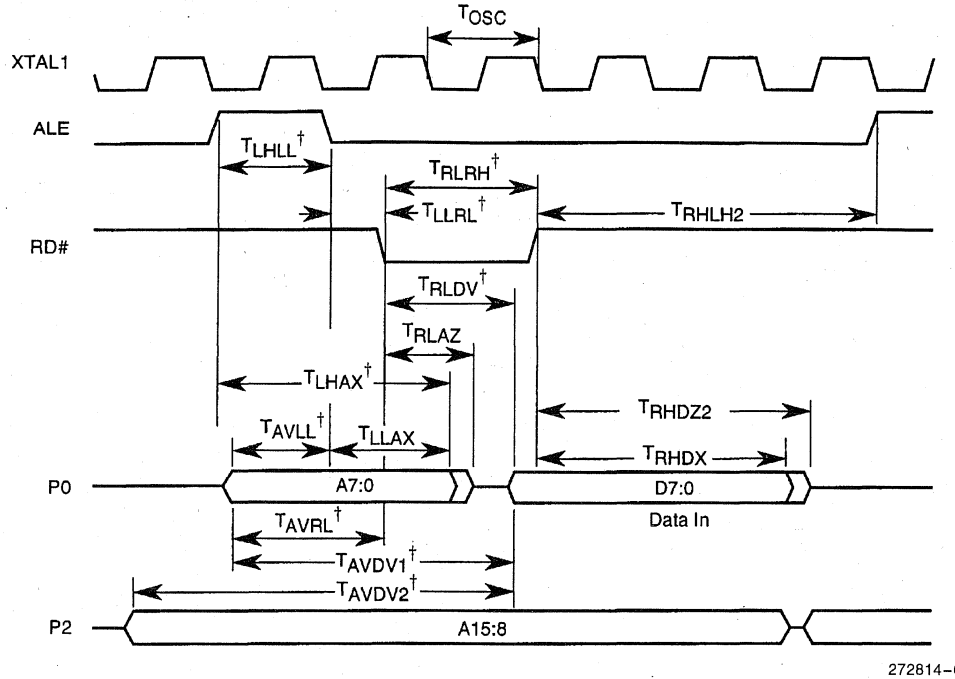
NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M = Number of wait states (0 or 1) for ALE.
4. In the formula, N = Number of wait states (0, 1, 2, or 3) for RD#/PSEN#/WR#.
5. "Typical" specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{OSC} (1)		F_{OSC} Variable		Units
		Min	Max	Min	Max	
T_{AVRL} (2)	Address Valid to RD#/PSEN# Low @ 12 MHz @ 16 MHz	 126.6 85		 2(1+M) T_{OSC} − 40		ns (3)
T_{AVWL1}	Address (P0) Valid to WR# Low @ 12 MHz @ 16 MHz	 126.6 85		 2(1+M) T_{OSC} − 40		ns (3)
T_{AVWL2}	Address (P2) Valid to WR# Low @ 12 MHz @ 16 MHz	 146.6 105		 2(1+M) T_{OSC} − 20		ns (3)
T_{WHQX}	Data Hold after WR# High @ 12 MHz @ 16 MHz	 63.3 42.5		 T_{OSC} − 20		ns
T_{QVWH}	Data Valid to WR# High @ 12 MHz @ 16 MHz	 138.6 97		 2(1+N) T_{OSC} − 28		ns (4)
T_{WHAX}	WR# High to Address Hold @ 12 MHz @ 16 MHz	 156.6 115		 $2T_{OSC}$ − 10		ns

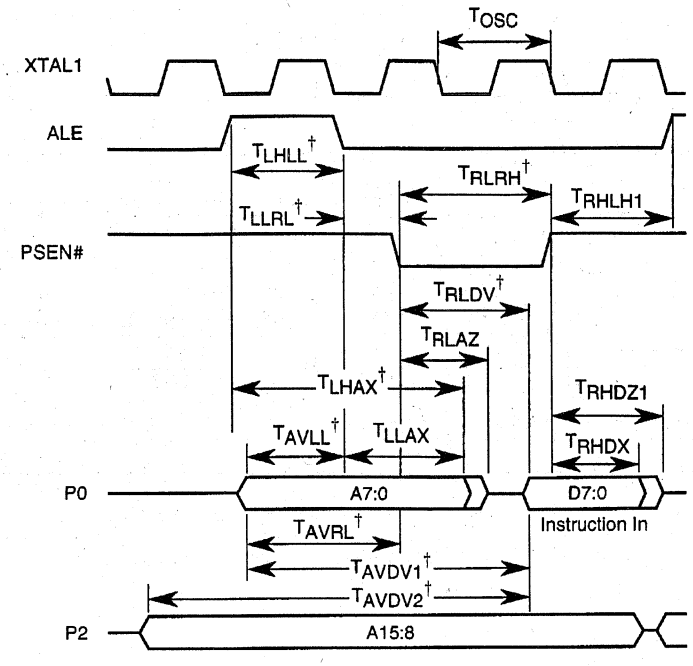
NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M = Number of wait states (0 or 1) for ALE.
4. In the formula, N = Number of wait states (0, 1, 2, or 3) for RD#/PSEN#/WR#.
5. "Typical" specifications are untested and not guaranteed.

SYSTEM BUS TIMINGS



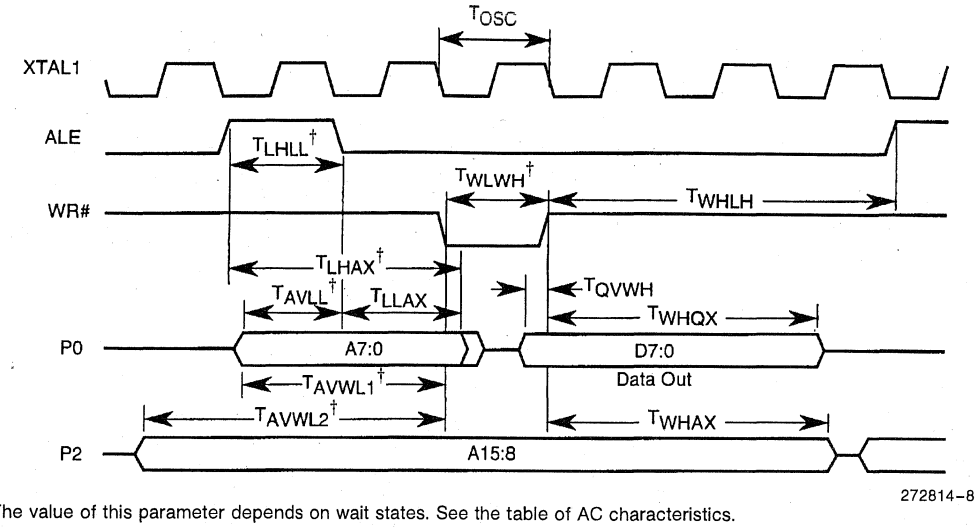
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 8. External Read Data Bus Cycle in Nonpage Mode



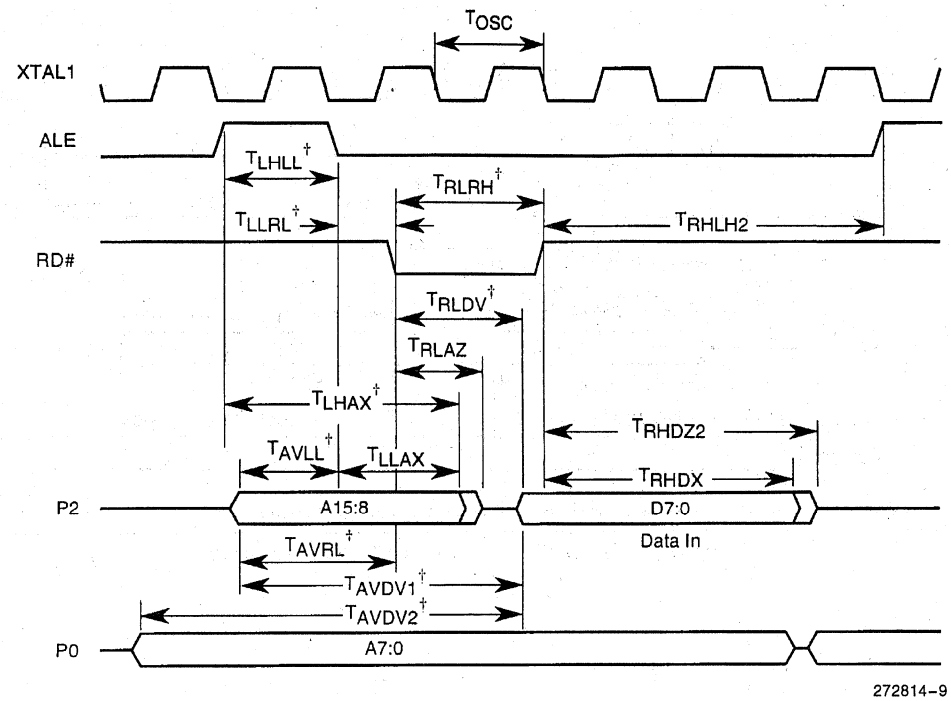
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 9. External Instruction Bus Cycle in Nonpage Mode



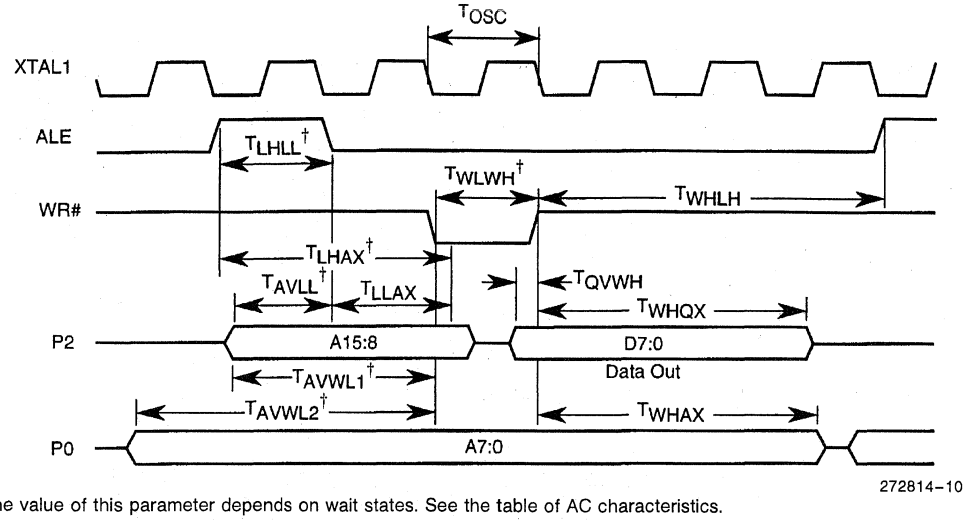
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 10. External Write Data Bus Cycle in Nonpage Mode



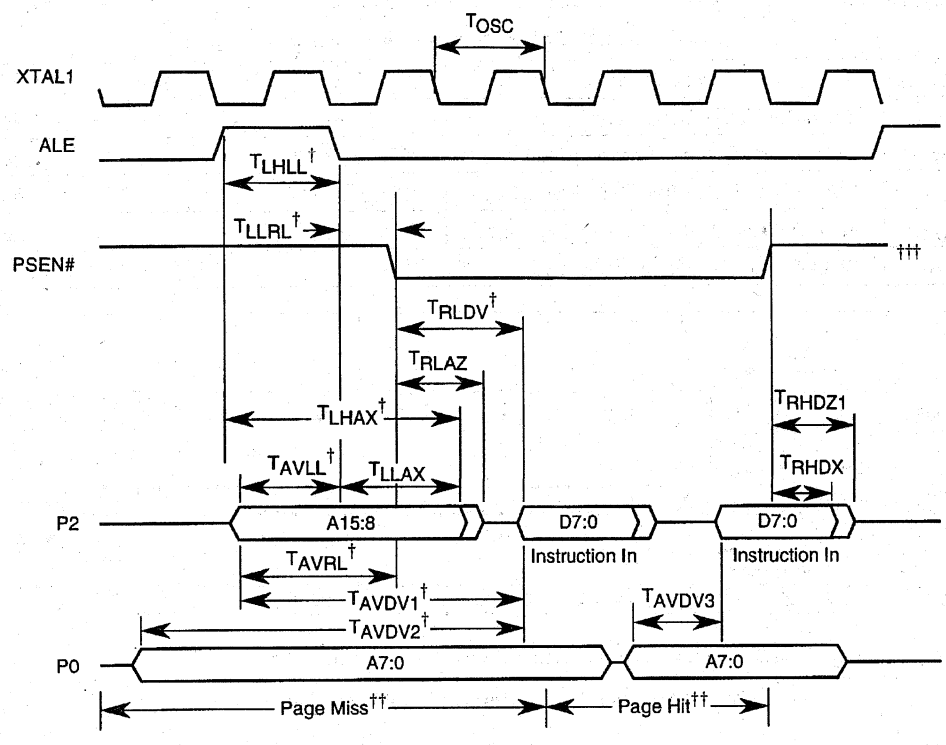
†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 11. External Read Data Bus Cycle in Page Mode



†The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 12. External Write Data Bus Cycle in Page Mode



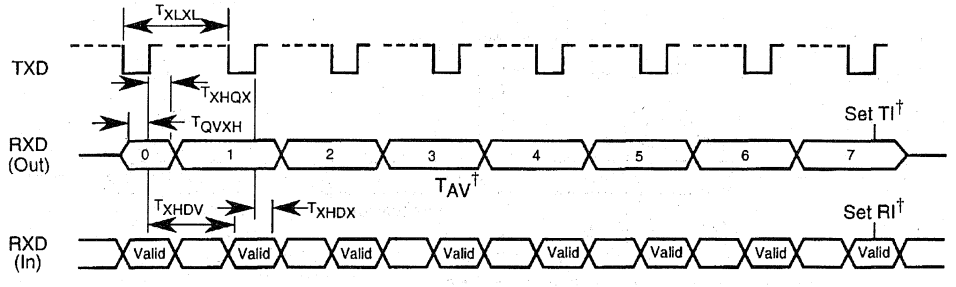
† The value of this parameter depends on wait states. See the table of AC characteristics.
†† A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).
††† During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

Figure 13. External Instruction Bus Cycle in Page Mode

AC Characteristics—Serial Port, Shift Register Mode

Table 10. Serial Port Timing Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns



† TI and RI are set during S1P1 of the peripheral cycle following the shift of the eighth bit.

Figure 14. Serial Port Waveform —Shift Register Mode

External Clock Drive

Table 11. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency (F_{OSC})		16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

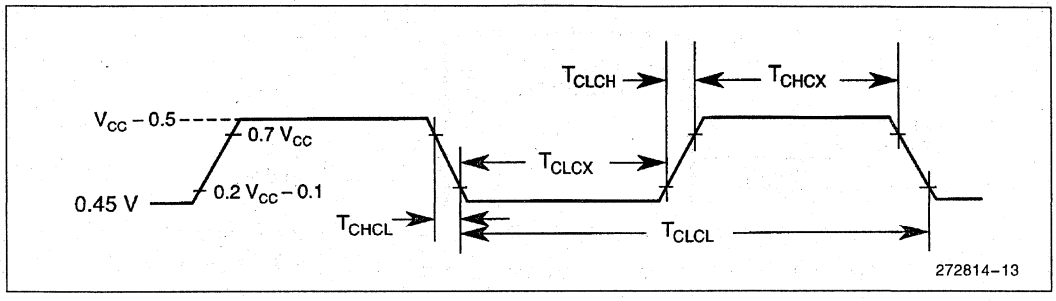
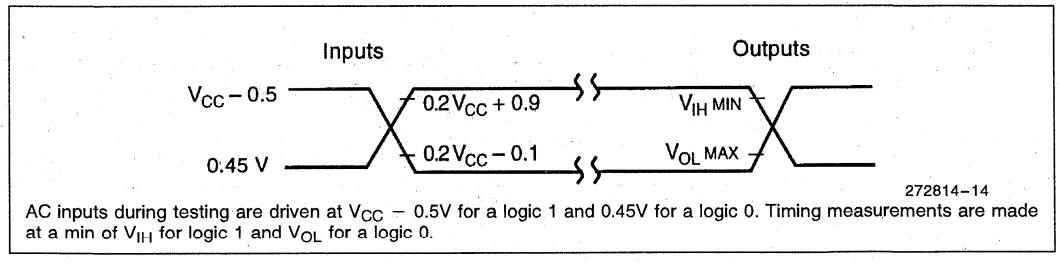
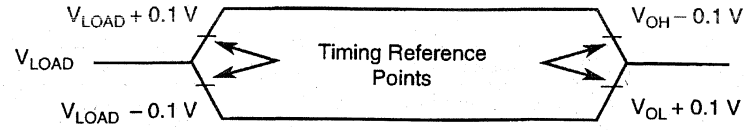


Figure 15. External Clock Drive Waveforms



AC inputs during testing are driven at V_{CC} – 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at a min of V_{IH} for logic 1 and V_{OL} for a logic 0.

Figure 16. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

Figure 17. Float Waveforms

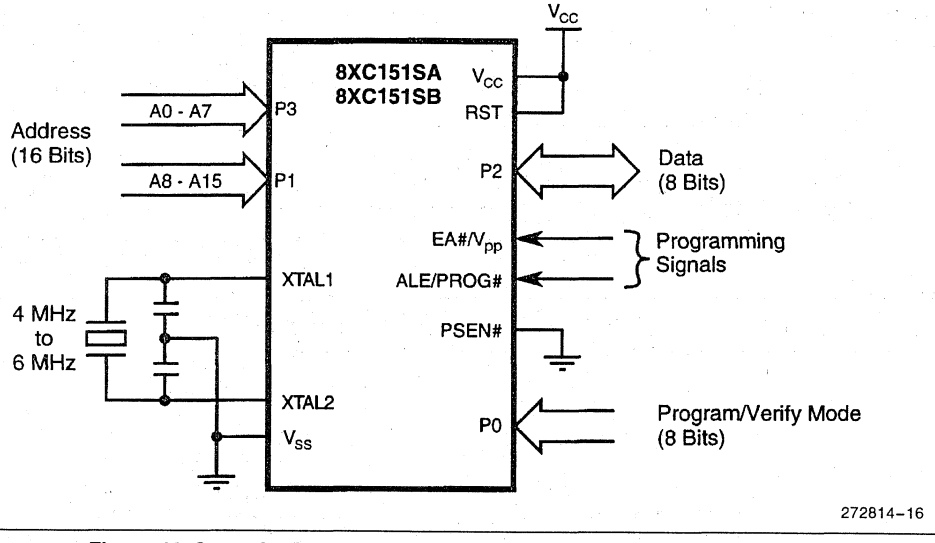


Figure 18. Setup for Programming and Verifying Nonvolatile Memory

PROGRAMMING AND VERIFYING NONVOLATILE MEMORY

The 87C151SA/SB has several areas of nonvolatile memory that can be programmed and/or verified: on-chip code memory (8/16 Kbytes), lock bits (3 bits), encryption array (128 bytes), and signature bytes (3 bytes).

Figure 18 shows the setup for programming and/or verifying the nonvolatile memory. Table 11 lists the programming and verification operations and indicates which operations apply to the different versions of the 87C151SA/SB. It also specifies the signals on the programming input (PROG#) and the ports. The ROM/OTPROM mode (port 0) specifies the operation (program or verify) and the base address of the memory area. The addresses (ports 1 and 3) are relative to the base address. (On-chip memory for a 16-Kbyte ROM/OTPROM device is located at address range 0000H–3FFFH. The other areas of the ROM/OTPROM are outside the memory address space and are accessible only during programming and verification.)

Information in Figures 19 and 20 define the configuration bits. Figure 21 shows the waveforms for the programming and verification cycles, and Table 12 lists the timing specifications. The signature bytes of the 83C151SA/SB ROM versions and the 87C151SA/SB OTPROM versions are factory programmed. Table 13 lists the addresses and the contents of the signature bytes.

Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.

NOTE:

The V_{PP} source in Figure 18 must be well regulated and free of glitches. The voltage on the V_{PP} pin must not exceed the specified maximum, even under transient conditions.

Table 12. Programming and Verification Modes Mode

Mode	8XC151SA/SB		PROG#	P0	P2	Addresses P1 (high), P3 (low)	Notes
	X = 7	X = 3					
Program On-Chip Code Memory	Y		5 Pulses	68H	Data	0000H–3FFFH (16K) 0000H–1FFFH (8K)	1
Verify On-Chip Code Memory	Y	Y	High	28H	Data	0000H–3FFFH (16K) 0000H–1FFFH (8K)	
Program Configuration Bytes							2
Verify Configuration Bytes							2
Program Lock Bits	Y		25 Pulses	6BH	XX	0001H–0003H	1, 3
Verify Lock Bits	Y	Y	High	2BH	Data	0000H	4
Program Encryption Array	Y		25 Pulses	6CH	Data	0000H–007FH	1
Verify Signature Bytes	Y	Y	High	29H	Data	0030H, 0031H, 0060H	

NOTES:
1. The PROG# pulse waveform is shown in Figure 20.
2. Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.
3. When programming the lock bits, the data bits on port 2 are don't care. Identify the lock bits with the address as follows: LB3 - 0003H, LB2 - 0002H, LB1 - 0001H.
4. The three lock bits are verified in a single operation. The states of the lock bits appear simultaneously at port 2 as follows: LB3 - P2.3, LB2 - P2.2. LB1 - P2.1. High = programmed.

UCONFIG0 Address FFF8H

7							0
—	WSA1#	WSA0#	XALE#	—	—	PAGE#	—

Bit Number	Bit Mnemonic	Function
7	—	Reserved
6:5	WSA1# WSA0# (see Note)	Wait State Select for external code WSA1# WSA0# Description 1 1 No wait states 1 0 Insert 1 wait state 0 1 Insert 2 wait states 0 0 Insert 3 wait states
4	XALE#	Extend Ale: If this bit is set, the time of the ALE pulse is T_{OSC}. Clearing this bit extends the time of the ALE pulse from T_{OSC} to $3T_{OSC}$, which adds one external wait state.
1	PAGE#	Page Mode Select: Clear this bit for page-mode (A15:8/D7:0 on P2, and A7:0 on P0). Set this bit for nonpage-mode (A15:8 on P2, and A7:0/D7:0 on P0 (compatible with MCS 51 microcontrollers)).

NOTE:
Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.

Figure 19. Configuration Byte 0

UCONFIG1 Address FFF9H

7							0
—	—	—	—	—	WSB1#	WSB0#	—

Bit Number	Bit Mnemonic	Function		
7:5	—	Reserved; set these bits when writing to UCONFIG1.		
2:1	WSB1#, WSB0#	Wait States for external data		
		WSB1#	WSB0#	Description
		1	1	No wait states
		1	0	Insert 1 wait state
		0	1	Insert 2 wait states
		0	0	Insert 3 wait states

NOTE:
Factory-programmed ROM and OTPROM versions of 8XC151SA/SB use configuration byte information supplied in a separate hexadecimal disk file. 8XC151SA/SB devices without internal ROM/OTPROM arrays fetch configuration byte information from external application memory based on an internal address range of FFF9:8H.

Figure 20. Configuration Byte 1

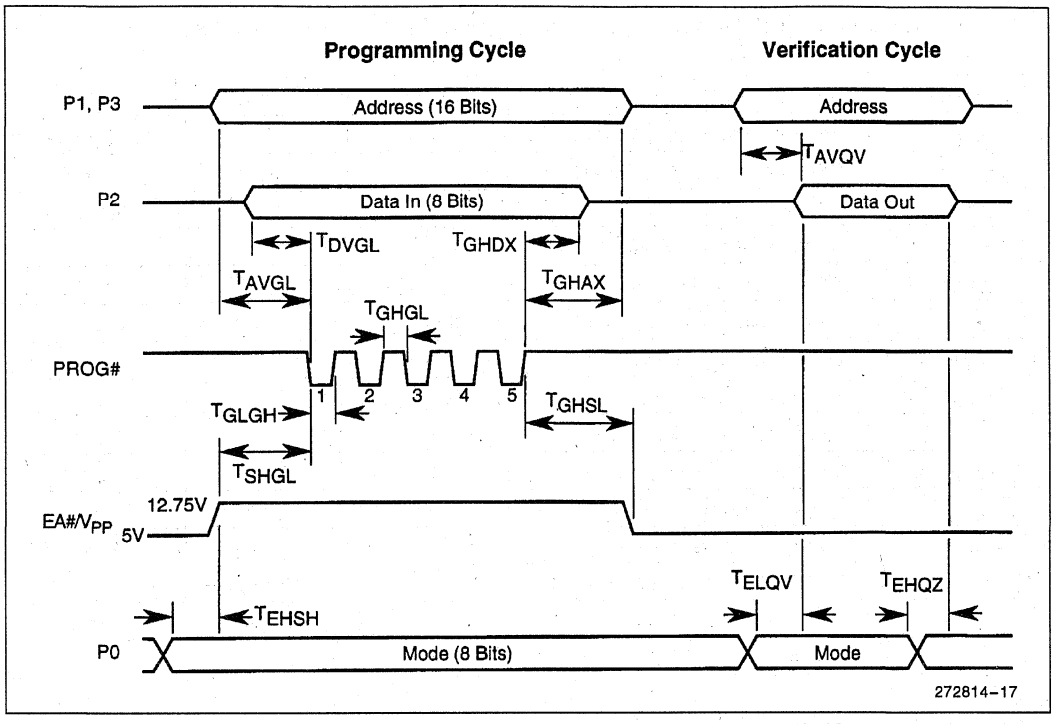


Figure 21. Timing for Programming and Verification of Nonvolatile Memory

Table 13. Nonvolatile Memory Programming and Verification Characteristics at T_A = 21 – 27°C, V_{CC} = 5V, and V_{SS} = 0V

Symbol	Definition	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.5	D.C. Volts
I_{PP}	Programming Supply Current		75	mA
F_{OSC}	Oscillator Frequency	4.0	6.0	MHz
T_{AVGL}	Address Setup to PROG# Low	$48T_{OSC}$		
T_{GHAX}	Address Hold after PROG#	$48T_{OSC}$		
T_{DVGL}	Data Setup to PROG# Low	$48T_{OSC}$		
T_{GHDX}	Data Hold after PROG#	$48T_{OSC}$		
T_{EHSH}	ENABLE High to V_{PP}	$48T_{OSC}$		
T_{SHGL}	V_{PP} Setup to PROG# Low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{GLGH}	PROG# Width	90	110	µs
T_{AVQV}	Address to Data Valid		$48T_{OSC}$	
T_{ELQV}	ENABLE Low to Data Valid		$48T_{OSC}$	
T_{EHQZ}	Data Float after ENABLE	0	$48T_{OSC}$	
T_{GHGL}	PROG# High to PROG# Low	10		µs

NOTE:
Notation for timing parameters:

A = Address D = Data E = Enable G = PROG# H = High L = Low
Q = Data out S = Supply (V_{PP}) V = Valid X = No Longer Valid Z = Floating

Table 14. Contents of the Signature Bytes

ADDRESS	CONTENTS	DEVICE TYPE
30H	89H	Indicates Intel Devices
31H	48H	Indicates MCS 151 core product
60H	7BH	Indicates 83C151SB device
60H	FBH	Indicates 87C151SB device
60H	7AH	Indicates 83C151SA device
60H	FAH	Indicates 87C151SA device

intel®

3

MCS®96 Microcontroller Family

MCS® 251 Architecture Overview

- **Binary Code Compatible with MCS 51® Architecture**
- **5 to 15 Times Increase in Performance Compared to MCS 251 Microcontroller at the Same Clock Speed**
- **3-Stage Pipeline CPU Architecture**
- **2 Clocks (1 State) per Instruction**
- **16-Bit Internal Code Bus**
  - **— 2 Bytes/State Code Fetch**
- **8-Bit ALU**
  - **— High Speed 8-Bit Source and 16-Bit Destination Bus**
- **40 Bytes General Purpose Register File**
  - **— Accessible as 16 8-Bit, 16 16-Bit or 10 32-Bit Registers**
  - **— With Accumulator Functionality and Data Indexing Capability**
- **24-Bit Linear Code and Data Addressing**
- **64KB Stack Space**
- **New Instructions and Addressing Modes**
  - **— 8, 16 and Limited 32-Bit Data Transfer, Arithmetic and Logical Instructions**
  - **— Supports Register, Immediate, Direct, Indirect, Displacement, Relative and Bit Addressing**
- **Support 64 Interrupt Sources**
  - **— 1 TRAP Instruction Interrupt (Highest Priority)**
  - **— 1 Non-Maskable Interrupt (2nd Highest Priority)**
  - **— 62 Maskable Interrupt Sources**
  - **— 4 Interrupt Priority Levels**
- **Complete Tools Support**
  - **— Assemblers and C Compilers**
  - **— In-Circuit Emulator**
  - **— OTP/EPROM Programmer**
  - **— Debuggers**

MCS 251 architecture is the next generation of Intel MCS 51 architecture that increases system performance by a factor of five using existing MCS 51 microcontroller code. By rewriting code using the MCS 251 architecture instructions, designers can increase performance up to 15 times.

The new MCS 251 architecture brings high performance, an increased memory mix and addressing, low power, low noise, efficient high level language support, enhanced instruction set, integrated features and functionality to the 8-bit embedded control market segment. All products in the family will be built around the new MCS 251 architecture core. They will have various peripherals, memories, input/ouput (I/O) ports, and a BIU (Bus Interface Unit). Most importantly, new proliferations will be binary code-compatible with existing 8051 components. Software investment is protected while providing an easy performance upgrade path. (See table 1 for features and benefits listing.)

The first product based on the new architecture will be 80C51 pin-compatible and a direct "plug-in" replacement. Anticipated availability of general samples is Q1 of 1995 with additional proliferations to follow later in the year.

Development tools for the new architecture will be available from some of the leading tools vendors. The vendors, including BSO Tasking; Data I/O Corporation; Keil Elektronik GmbH/Franklin Software Inc.; Metalink Corporation; Needham; Nohau Corporation; Production Languages Corporation (PLC); SMS Mikrocomputer-Systeme GmbH; and System General Corporation are planning to supply a full range of hardware and software development tools such as emulators, compilers, programmers and debuggers.

December 1995 Order Number: 272620-001

Table 1. Features and Benefits

Features	Benefits
• 3-stage pipeline CPU architecture • 1 state (2 clocks) per machine cycle (vs 6 states (12 clocks) per machine cycle for MCS® 51 microcontroller) • 16-bit internal code bus	• High performance. 5 to 15 times increase in performance compared to MCS 51 microcontroller at the same clock speed • High instruction throughput at low clock speed reduces power consumption and RFI

• Enhanced MCS 51 instruction set with:
  • 16-bit and limited 32-bit data transfer, arithmetic and logic instructions
  • Register-to-register operations
  • Extended addressing modes
  • Improved control instructions
  • Bigger bit addressable space
	• Increased performance and programming flexibility.
	• Reduced code size.

• Binary code-compatible with MCS 51 microcontroller	• Protects software investment • Easy performance upgrade from MCS 51 microcontroller applications
• Register-based machine with 40 register bytes accessible as 16 8-bit registers, 16 16-bit registers, 10 32-bit registers or a combination of all. All registers are general-purpose with accumulator functionality and data indexing capability.	• Increased performance and programming flexibility • Increased efficiency for C code
• 24-bit linear addressing for up to 16 MB memory space	• Support bigger code and data memory requirement.
• 64 KB extended stack space and additional stack instructions	• Increased efficiency for C code

CPU Overview

The central processing unit (CPU) represents the heart of the MCS 251 architecture and consists of the ALU, instruction sequencer, program counter and the register file, connected by high-speed source and destination buses. The CPU performs all instructions as a series of 8-bit microcontroller operations. The CPU is implemented using typical pipelining techniques, and is built around a three-stage pipeline. The pipe stages are instruction fetch or decode, address generation or data fetch, and execution or write back. The three-stage pipeline implementation offers the best trade-off between performance and design complexity.

Memory Interface

The CPU interfaces with the peripherals, memories and other chip units via internal instruction and data buses. The MCS 251 architecture has an internal 16-bit wide instruction bus capable of sustained 2 bytes/state code fetches. It also has an 8-bit data bus capable of one byte/state data transfer rate.

The MCS 251 architecture has one contiguous 16MB address space that is used for both code and data. The 16MB address space will be partitioned for internal and external access, depending on the amount of on-chip memory.

Code memory can reside anywhere in the address space except for reserved areas. Further restrictions may prevent code execution from certain locations that may vary from product to product. The code memory resides outside the CPU and will be partitioned as internal and external memory, depending on the amount of on-chip code memory.

Data memory can reside anywhere in the address space except for reserved areas. The lower 32 bytes of the data memory space can be accessed as both data memory and as four banks of general-purpose registers. All MCS 251 controllers will have this memory as part of the CPU; the amount of additional on-chip data memory may vary from product to product.

To provide flexibility to designers during development and production, the MCS 251 microcontroller will have one-time programmable (OTP), ROM and CPU-only versions available. Flash memory versions will be available in the future.

The MCS 251 architecture also supports an extra 32 bytes of general-purpose registers which reside in the CPU as register file. This is in addition to the 4 banks of 8 registers found on the MCS 51 microcontroller architecture. The register file can be addressed in the following ways, depending upon the registers to be accessed: registers 0–15 can be addressed as either byte, word or double word (Dword) registers; registers 16–31 can be addressed as either word or Dword registers; and registers 56–63 can be addressed only as Dword registers. There are 16 possible byte registers, 16 possible word registers and 10 possible Dword registers depending on the combinations. (See Figure 1 for register file diagram.)

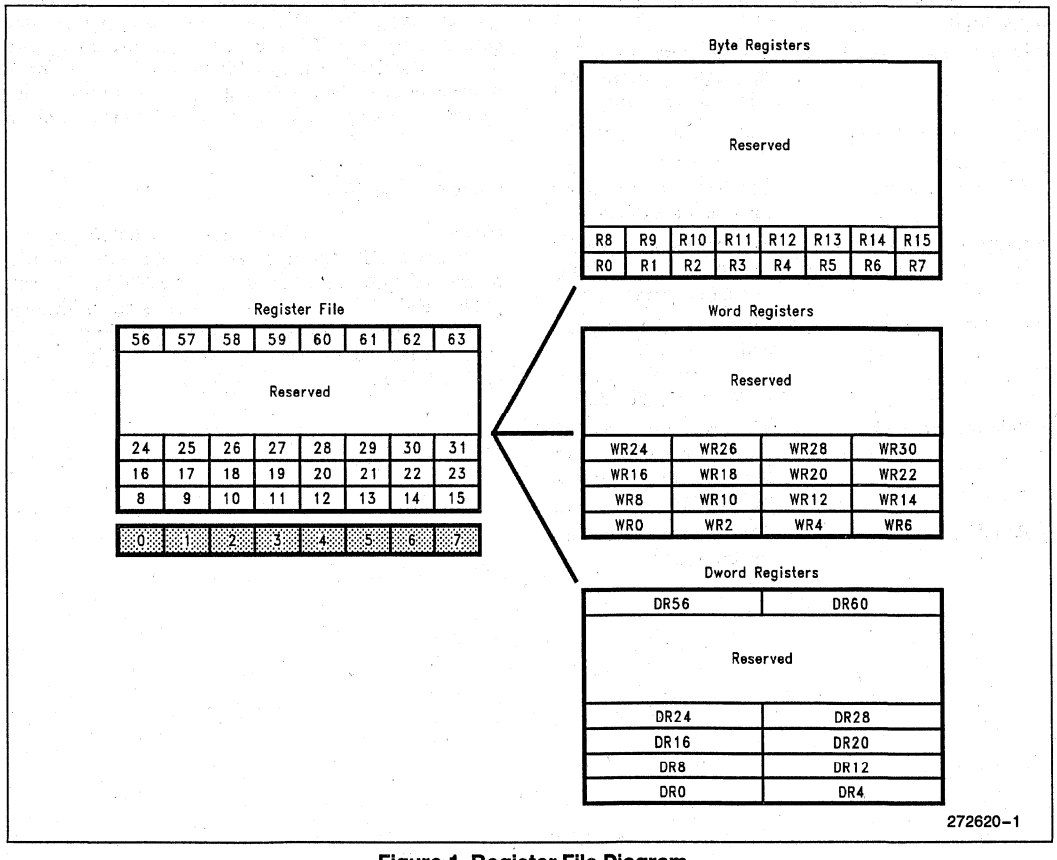


Figure 1. Register File Diagram

New Instruction Set

The MCS 251 architecture instruction set provides the user with newly-defined instructions that take advantage of the new architecture while maintaining all existing MCS 51 microcontroller instructions. Many of the MCS 251 microcontroller instructions can operate on either 8-, 16-, or limited 32-bit operands. This capability allows the MCS 251 architecture proliferations to be used more easily and efficiently with high-level programming languages such as "C."

The instruction set consists of data instructions, bit instructions and control instructions. Data instructions process 8-, 16-, and limited 32-bit data; bit instructions manipulate bits; and control instructions manage program flow. Each instruction type has a unique set of addressing modes; for example, not all data addressing modes apply to control instructions and vice-versa. The MCS 251 architecture supports the following addressing modes:

- Register addressing: The instruction specifies the register which contains the operand.
- Immediate addressing: The instruction contains the operand.
- Direct addressing: The instruction contains the operand address.
- Indirect addressing: The instruction specifies the register containing operand address.
- Displacement addressing: The sum of the register and a signed offset specified by the instruction is the operand address.
- Relative addressing: The instruction contains the relative offset from the next instruction to target address.
- Bit addressing: The instruction contains the bit address.

Interrupt Overview

The MCS 251 architecture supports one non-maskable interrupt, one TRAP (technical return analysis program) instruction interrupt and up to 62 maskable interrupt sources. The user can select each interrupt individually as well as control its priority level. The non-maskable interrupt is fixed in hardware to always have the second highest priority (after TRAP) and is always enabled. The exact number of interrupt sources, both internal and external, depends on the specific MCS 251 architecture proliferations.

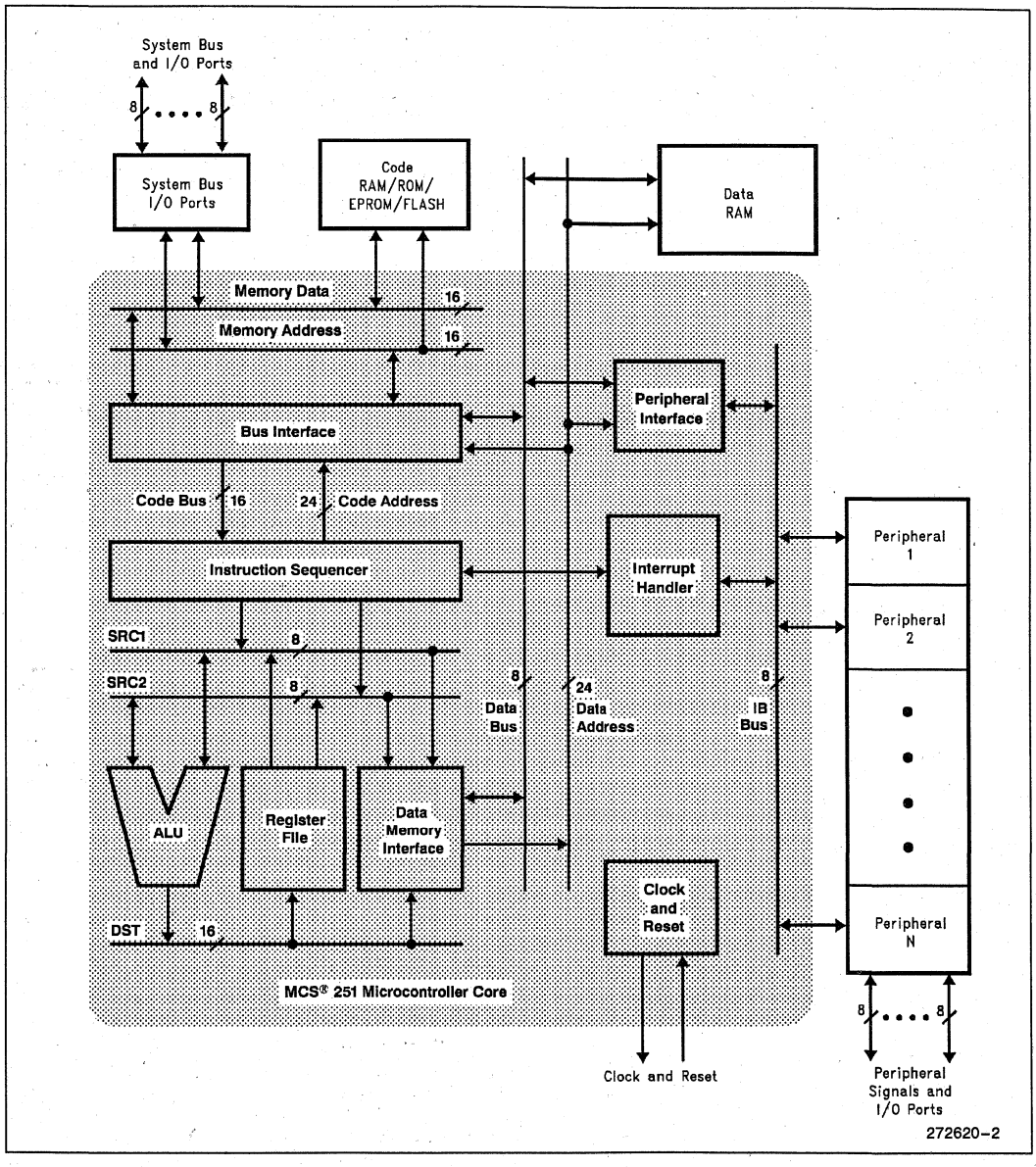
Compatibility

The MCS 251 architecture is code-compatible with the MCS 51 architecture. And, all 51 microcontroller instructions are available on the 251. The 51 controllers have four separate address spaces: program memory, special function registers, and internal and external data memory. The 251 incorporates the program memory and the data memory address spaces into a 16MB unified address space. The mapping is completely transparent to the user and is taken care of by the assembler.

Future Outlook

General samples for first product based on the MCS 251 architecture core are anticipated in the first quarter of 1995. This product will be 80C51 pin-compatible and a direct plug-in replacement. Additional products based on the core will include additional peripherals targeted to specific market segments to meet customer needs.

MCS® 251 Architecture Block Diagram



8XC251SB
HIGH-PERFORMANCE
CHMOS SINGLE-CHIP MICROCONTROLLER

Commercial

- Binary-code Compatible with MCS® 51 Microcontrollers
- Pin Compatible with 44-lead PLCC MCS 51 Microcontrollers
- Register-based MCS 251 Architecture
  - 40-byte Register File
  - Registers Accessible as Bytes, Words, and Double Words
- Enriched Instruction Set
  - 16-bit and 32-bit Arithmetic and Logic Instructions
  - Compare and Conditional Jump Instructions
  - Expanded Set of Move Instructions
- Linear Addressing
- 128-Kbyte External Code/Data Memory Space
- 16-Kbyte On-chip OTPROM/ROM (Optional device without ROM available)
- 16-bit Internal Code Fetch
- 64-Kbyte Extended Stack Space
- 1-Kbyte On-chip Data RAM
- 8-bit, 2-clock External Code Fetch in Page Mode
- Instruction Pipeline
- User-selectable Configurations:
  - External Wait State
  - Address Range
  - Page Mode
- 32 Programmable I/O Lines
- Seven Maskable Interrupt Sources with Four Programmable Priority Levels
- Three Flexible 16-bit Timer/counters
- Hardware Watchdog Timer
- Programmable Counter Array
  - High-speed Output
  - Compare/Capture Operation
  - Pulse Width Modulator
  - Watchdog Timer
- Programmable Serial I/O Port
  - Framing Error Detection
  - Automatic Address Recognition
- Power-saving Idle and Powerdown Modes
- High-performance CHMOS Technology
- 0–16 MHz Operation
- Complete System Development Support
  - Compatible with Existing Tools
  - New Tools Available: Compiler, Assembler, Debugger, ICE

A member of the Intel family of 8-bit MCS 251 microcontrollers, the 8XC251SB is binary-code compatible with MCS 51 microcontrollers and pin compatible with 44-lead PLCC MCS 51 microcontrollers. MCS 251 microcontrollers feature an enriched instruction set, linear addressing, and efficient C-language support. The 8XC251SB has 1 Kbyte of on-chip RAM and is available with 16 Kbytes of on-chip OTPROM (87C251SB), with 16 Kbytes of ROM (83C251SB), or without ROM (80C251SB). A variety of features can be selected by user-programmed OTPROM configuration (87C251SB) or factory-programmed ROM configuration (83C251SB).

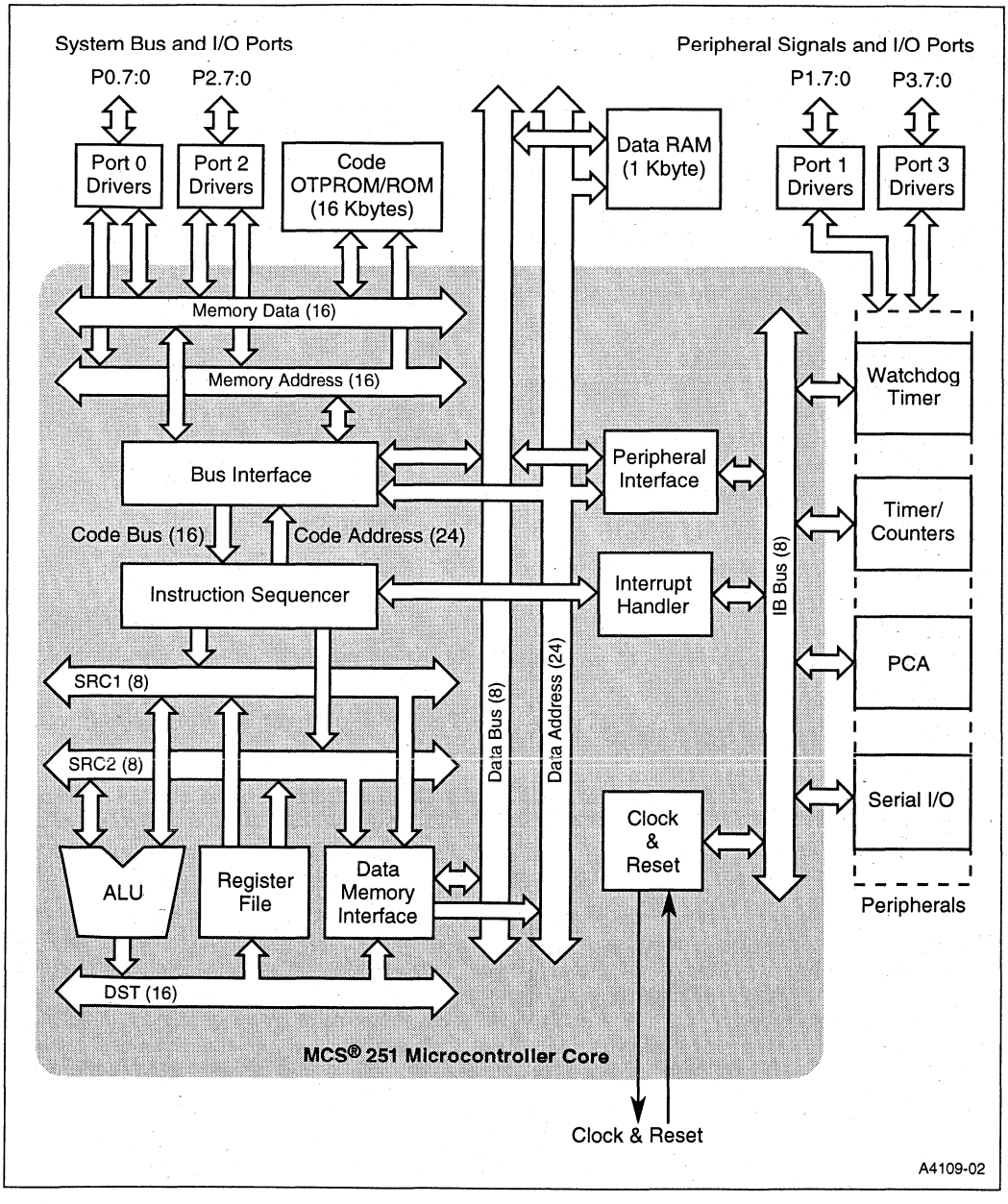


Figure 1. 8XC251SB Block Diagram

COMMERCIAL TEMPERATURE RANGE

With the commercial (standard) temperature option, the device operates over the temperature range 0°C to +70°C.

PROLIFERATION OPTIONS

Table 1. Proliferation Options

8XC251SB (1) (0 – 12 MHz; 5 V ±10%)	8XC251SB-16 (1) (0 – 16 MHz; 5 V ±10%)
80C251SB (2)	80C251SB-16 (3)
83C251SB	83C251SB-16
87C251SB	87C251SB-16

NOTES:
1. The 8XC251SB and 8XC251SB-16 are binary-code compatible with MCS 51 microcontrollers.
2. Configurations available for 80C251SB:
   a. Nonpage mode and no wait states (Table 13)
   b. User-defined configurations
3. Configurations available for 80C251SB-16:
   a. Nonpage mode and one wait state (Table 13)
   b. User-defined configurations

NOTE:

Data for the 8XC251SB also applies to the 8XC251SB-16 unless otherwise noted.

PROCESS INFORMATION

This device is manufactured on a complimentary high performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change dependent upon operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 2. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
44-pin PLCC	46°C/W	16°C/W

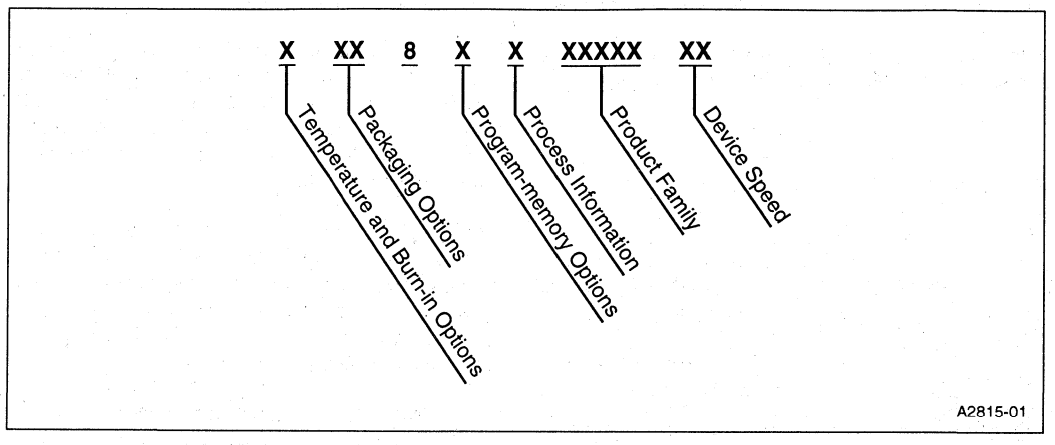


Figure 2. The 8XC251SB Family Nomenclature

Table 3. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	N	Plastic Leaded Chip Carrier (PLCC)
Program Memory Options	0	Without ROM
	3	With ROM
	7	With OTPROM
Process Information	C	CHMOS
Product Family	251SB	Advanced 8-bit control architecture
Device Speed	no mark	12 MHz
	-16	16 MHz

Table 4. 8XC251SB Memory Map

Address (Note 1, 2)	Description	Notes
FF:FFFFH FF:4000H	External Memory	3
FF:3FFFH FF:0000H	87C251SB/83C251SB: 16-Kbyte Internal OTPROM/ROM or External Memory, as determined by EA# pin (Table 7) 80C251SB: External Memory	3, 4, 5
FE:FFFFH FE:0000H	External Memory	3
FD FFFFH 02:0000H	Reserved	6
01:FFFFH 01:0000H	External Memory	3
00:FFFFH 00:E000H	87C251SB/83C251SB: External Memory or redirected to OTPROM/ROM 80C251SB: External Memory	5, 7
00:DFFFH 00:0420H	External Memory	7
00:041FH 00:0080H	On-chip RAM	7
00:007FH 00:0020H	On-chip RAM	8
00:001FH 00:0000H	Storage for R0–R7 of Register File	9

NOTES:
1. Only 16/17 address lines are bonded out (A15:0 or A16:0 as selected during chip configuration).
2. The special function registers (SFRs) and the register file have separate address spaces.
3. Data is accessible by indirect addressing only.
4. The 8XC251SB resets to location FF:0000H.
5. The 87C251SB/83C251SB can be configured so that locations FF:2000H–FF:3FFFH in internal OTPROM/ROM are also mapped to locations 00:E000H–00:FFFFH. In this case, if EA# = 1, a data read to 00:E000H–00:FFFFH is redirected to internal OTPROM/ROM (see bit 1 in CONFIG0).
6. This reserved area of memory is unavailable for use. Reading a location in this area returns an unspecified value. A write to this area does execute, but nothing is actually written.
7. Data is accessible by direct and indirect addressing.
8. Data is accessible by direct, indirect, and bit addressing.
9. Data is accessible by direct, indirect, and register addressing.

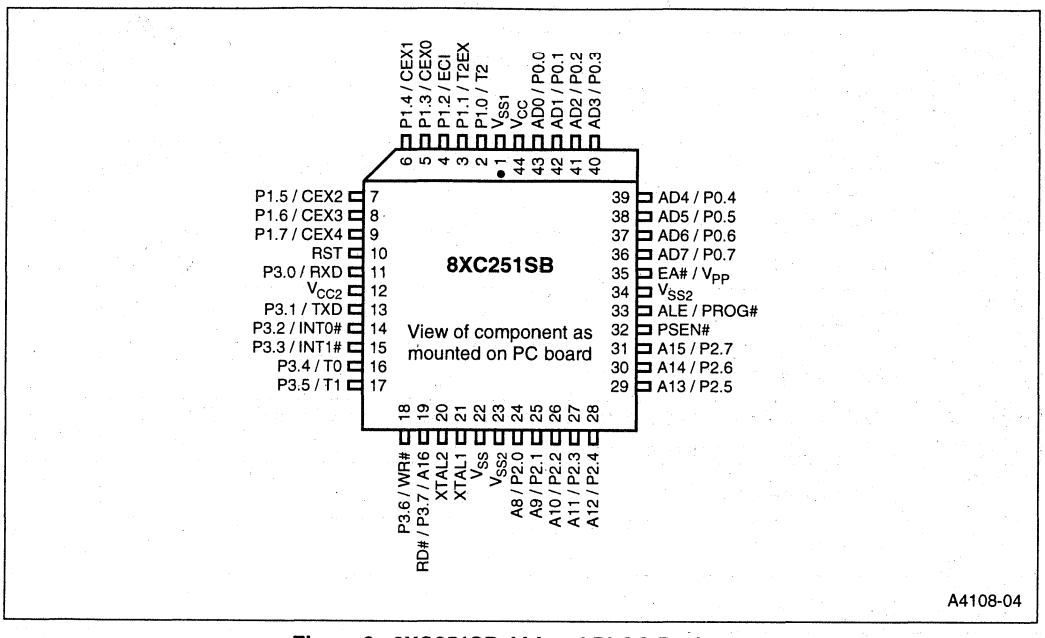


Figure 3. 8XC251SB 44 Lead PLCC Package

Table 5. 44-pin PLCC Pin Assignment

Pin	Name
1	V_{SS1}
2	T2/P1.0
3	T2EX/P1.1
4	ECI/P1.2
5	CEX0/P1.3
6	CEX1/P1.4
7	CEX2/P1.5
8	CEX3/P1.6
9	CEX4/P1.7
10	RST
11	RXD/P3.0
12	V_{CC2}
13	TXD/P3.1
14	INT0#/P3.2
15	INT1#/P3.3
16	T0/P3.4
17	T1/P3.5
18	WR#/P3.6
19	RD#/P3.7
20	XTAL2
21	XTAL1
22	V_{SS}

Pin	Name
23	V_{SS2}
24	A8/P2.0
25	A9/P2.1
26	A10/P2.2
27	A11/P2.3
28	A12/P2.4
29	A13/P2.5
30	A14/P2.6
31	A15/P2.7
32	PSEN#
33	ALE/PROG#
34	V_{SS2}
35	EA#/V_{PP}
36	AD7/P0.7
37	AD6/P0.6
38	AD5/P0.5
39	AD4/P0.4
40	AD3/P0.3
41	AD2/P0.2
42	AD1/P0.1
43	AD0/P0.0
44	V_{CC}

Table 6. 44-pin PLCC Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
AD0/P0.0	43
AD1/P0.1	42
AD2/P0.2	41
AD3/P0.3	40
AD4/P0.4	39
AD5/P0.5	38
AD6/P0.6	37
AD7/P0.7	36
A8/P2.0	24
A9/P2.1	25
A10/P2.2	26
A11/P2.3	27
A12/P2.4	28
A13/P2.5	29
A14/P2.6	30
A15/P2.7	31

Processor Control	
Name	**Pin**
INT0#/P3.2	14
INT1#/P3.3	15
EA#/V_{PP}	35
RST	10
XTAL1	21
XTAL2	20

Input/Output	
Name	**Pin**
T2/P1.0	2
T2EX/P1.1	3
ECI/P1.2	4
CEX0/P1.3	5
CEX1/P1.4	6
CEX2/P1.5	7
CEX3/P1.6	8
CEX4/P1.7	9
RXD/P3.0	11
TXD/P3.1	13
T0/P3.4	16
T1/P3.5	17

Power & Ground	
Name	**Pin**
V_{CC}	44
V_{CC2}	12
V_{SS}	22
V_{SS1}	1
V_{SS2}	23, 34

Bus Control & Status	
Name	**Pin**
WR#/P3.6	18
RD#/P3.7	19
ALE/PROG#	33
PSEN#	32

PIN DESCRIPTIONS

Table 7. Pin Descriptions

Signal Name	Type	Description	Multiplexed With
A16	O	**Address Line 16**. See RD#.	N.A.
A15:8†	O	**Address Lines**. Upper address lines for the external bus.	P2.7:0
AD7:0†	I/O	**Address/Data Lines**. Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	PROG#
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Pins**. These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.7:3
EA#	I	**External Access**. Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is to on-chip OTPROM/ROM if the address is within the range of the on-chip OTPROM/ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground.	V_{PP}
ECI	I	**PCA External Clock Input**. External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
P0.7:0	I/O	**Port 0**. This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1**. This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI CEX4:0
P2.7:0	I/O	**Port 2**. This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3**. This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#
PROG#	I	**Programming Pulse**. The programming pulse is applied to this pin for programming the on-chip OTPROM.	ALE

NOTE: †The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Pin Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
PSEN#	O	**Program Store Enable.** Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte CONFIG1 (see also RD#): **RD1 RD0 Address Range for Assertion** 0 0 Reserved 0 1 All addresses 1 0 All addresses 1 1 All addresses ≥ 80:0000H	—
RD#	O	**Read or 17th Address Bit (A16).** Read signal output to external data memory or 17th external address bit (A16), depending on the values of bits RD0 and RD1 in configuration byte CONFIG1. (See also PSEN#): **RD1 RD0 Function** 0 0 Reserved 0 1 The pin functions as A16 only. 1 0 The pin functions as P3.7 only. 1 1 RD#: asserted for reads at all addresses ≤ 7F:FFFFH	P3.7
RST	I	**Reset.** Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this pin and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data.** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
T1:0	I	**Timer 1:0 External Clock Inputs.** When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output.** For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input.** In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data.** TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
V_{CC}	PWR	**Supply Voltage.** Connect this pin to the +5V supply voltage.	—

NOTE: †The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Pin Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this pin to the +5V supply voltage is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility.	—
V_{PP}	I	**Programming Supply Voltage**. The programming supply voltage is applied to this pin for programming the on-chip OTPROM.	EA#
V_{SS}	GND	**Circuit Ground**. Connect this pin to ground.	—
V_{SS1}	GND	**Secondary Ground**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51BH, V_{SS1} can be unconnected without loss of compatibility.	—
V_{SS2}	GND	**Secondary Ground 2**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility.	—
WR#	O	**Write**. Write signal output to external memory. For configuration bits RD1 = RD0 = 1, WR# is strobed only for writes to locations 00:0000H–01:FFFFH. For other values of RD1:0, WR# is strobed for writes to all memory locations.	P3.6
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	—
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	—

NOTE: †The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on EA#/V_{PP} Pin to V_{SS} ..... 0 V to +13.0 V
Voltage on any other Pin to V_{SS} ..... -0.5 V to +6.5 V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation ..... 1.5 W

NOTE:

Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias):
Commercial ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
V_{SS} ..... 0 V

NOTICE: This datasheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC Characteristics

Parameter values apply to all devices unless otherwise indicated.

Table 8. DC Characteristics at V_{CC} = 4.5 – 5.5 V

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	-0.5		$0.2V_{CC} - 0.1$	V	
V_{IL1}	Input Low Voltage (EA#)	0		$0.2V_{CC} - 0.3$	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (Note 1, Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (Note 1, Note 2)
V_{OH}	Output High Voltage (Port 1, 2, 3, ALE, PSEN#)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA (Note 3)

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   - port 0: 26 mA
   - ports 1–3: 15 mA

   Maximum Total I_{OL} for All Output Pins: 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25° C and are not guaranteed.

Table 8. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Continued)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{OH2}	Output High Voltage (Port 2 in External Address during Page Mode)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)			-50	µA	VIN = 0.45 V
I_{LI}	Input Leakage Current (Port 0)			+/-10	µA	0.45 < VIN < V_{CC}
I_{TL}	Logical 1–to–0 Transition Current (Port 1, 2, 3)			-650	µA	VIN = 2.0 V
R_{RST}	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10 (Note 4)		pF	F_{OSC} = 16 MHz T_A = 25 °C
I_{PD}	Powerdown Current		10 (Note 4)	75	µA	
I_{DL}	Idle Mode Current		10 (Note 4)	20	mA	F_{OSC} = 16 MHz
I_{CC}	Operating Current		45 (Note 4)	80	mA	F_{OSC} = 16 MHz

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   - port 0: 26 mA
   - ports 1–3: 15 mA

   Maximum Total I_{OL} for All Output Pins: 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25° C and are not guaranteed.

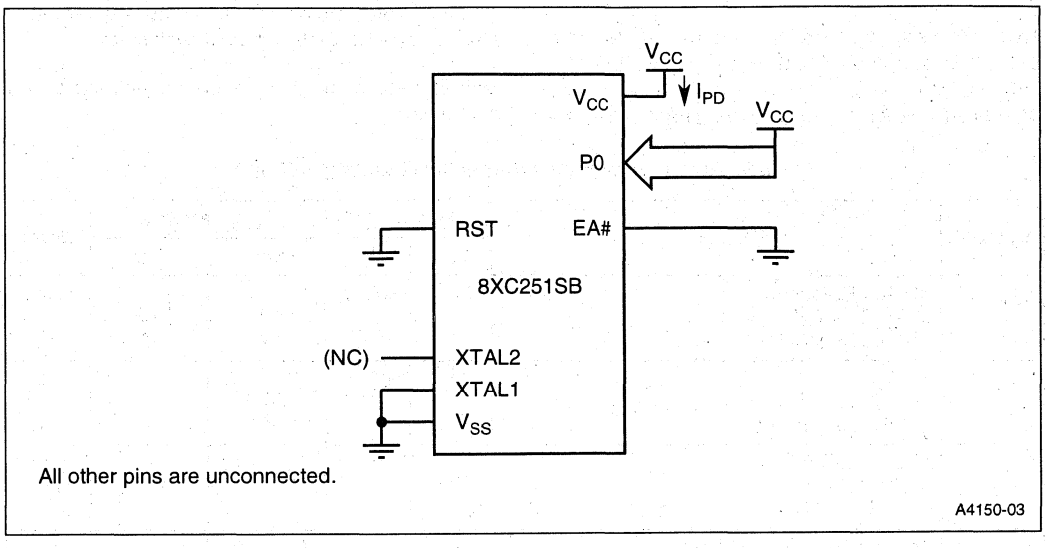


Figure 4. I_{PD} Test Condition, Powerdown Mode, V_{CC} = 2.0 – 5.5V.

AC Characteristics

Table 9 lists AC timing parameters for the 8XC251SB and 8XC251SB-16 with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and/or by extending ALE. In the table, Notes 3 and 5 mark parameters affected by an ALE wait state, and Notes 4 and 5 mark parameters affected by a PSEN#/RD#/WR# wait state.

Figures 5–10 show the bus cycles with the timing parameters.

Table 9. AC Characteristics (Capacitive Loading = 50 pF)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
F_{OSC}	XTAL1 Frequency 8XC251SB 8XC251SB-16	N/A	N/A	 0 0	 12 16	MHz
T_{OSC}	$1/F_{OSC}$ 8XC251SB 8XC251SB-16	N/A	N/A	 83.3 62.5		ns
T_{LHLL}	ALE Pulse Width 8XC251SB 8XC251SB-16	 73.3 52.5		$T_{OSC} - 10$		ns (3)
T_{AVLL}	Address Valid to ALE Low 8XC251SB 8XC251SB-16	 63.3 42.5		$T_{OSC} - 20$		ns (3)
T_{LLAX}	Address Hold after ALE Low 8XC251SB 8XC251SB-16	 63.3 42.5		$T_{OSC} - 20$		ns
T_{RLRH} (2)	RD# or PSEN# Pulse Width 8XC251SB 8XC251SB-16	 65.3 44.5		$T_{OSC} - 18$		ns (4)
T_{WLWH}	WR# Pulse Width 8XC251SB 8XC251SB-16	 65.3 44.5		$T_{OSC} - 18$		ns (4)
T_{LLRL} (2)	ALE Low to RD# or PSEN# Low 8XC251SB 8XC251SB-16	 73.3 52.5		$T_{OSC} - 10$		ns
T_{LHAX}	ALE High to Address Hold 8XC251SB 8XC251SB-16	 146.6 105		$2T_{OSC} - 20$		ns (3)
T_{RLDV} (2)	RD# or PSEN# Low to Valid Data/Instruct. In 8XC251SB 8XC251SB-16		 33.3 12.5		$T_{OSC} - 50$	ns (4)

NOTES:
1. 12 MHz for 8XC251SB and 16 MHz for 8XC251SB-16.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$.
5. If wait states are added as described in both Note 4 and Note 3, add a total of $4T_{OSC}$.
6. "Typical" specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{RHDX} (2)	Data/Instruct. Hold After RD# or PSEN# High	0		0		ns
T_{RLAZ} (2)	RD#/PSEN# Low to Address Float	Typ.=0 (6)	2	Typ. = 0 (6)	2	ns
T_{RHDZ} (2)	Data/Instruct. Float After RD# or PSEN# High 8XC251SB 8XC251SB-16		 63.3 42.5		T_{OSC} – 20	ns
T_{RHLH1}	RD#/PSEN# High to ALE High (Instruction) 8XC251SB 8XC251SB-16	 68.3 47.5		T_{OSC} – 15		ns
T_{RHLH2}	RD#/PSEN# High to ALE High (Data) 8XC251SB 8XC251SB-16	 234.9 172.5		$3T_{OSC}$ – 15		ns
T_{WHLH}	WR# High to ALE High 8XC251SB 8XC251SB-16	 234.9 172.5		$3T_{OSC}$ – 15		ns
T_{AVDV1}	Address (P0) Valid to Valid Data/Instruction In 8XC251SB (3) 8XC251SB-16 (3)		 189.9 127.5		$3T_{OSC}$ – 60	ns (3,4,5)
T_{AVDV2}	Address (P2) Valid to Valid Data/Instruction In 8XC251SB (3) 8XC251SB-16 (3)		 273.2 190		$4T_{OSC}$ – 60	ns (3,4,5)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In 8XC251SB 8XC251SB-16		 106.6 65		$2T_{OSC}$ – 60	ns
T_{AVRL} (2)	Address Valid to RD#/PSEN# Low 8XC251SB 8XC251SB-16	 142.6 101		$2T_{OSC}$ – 24		ns (3)
T_{AVWL1}	Address (P0) Valid to WR# Low 8XC251SB 8XC251SB-16	 142.6 101		$2T_{OSC}$ – 24		ns (3)
T_{AVWL2}	Address (P2) Valid to WR# Low 8XC251SB 8XC251SB-16	 219.9 157.5		$3T_{OSC}$ – 30		ns (3)

NOTES:
1. 12 MHz for 8XC251SB and 16 MHz for 8XC251SB-16.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$.
5. If wait states are added as described in both Note 4 and Note 3, add a total of $4T_{OSC}$.
6. "Typical" specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{WHQX}	Data Hold after WR# High 8XC251SB 8XC251SB-16	 63.3 42.5		$T_{OSC} - 20$		ns
T_{QVWH}	Data Valid to WR# High 8XC251SB 8XC251SB-16	 58.3 37.5		$T_{OSC} - 25$		ns (4)
T_{WHAX}	WR# High to Address Hold 8XC251SB 8XC251SB-16	 146.6 105		$2T_{OSC} - 20$		ns

NOTES:
1. 12 MHz for 8XC251SB and 16 MHz for 8XC251SB-16.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$.
5. If wait states are added as described in both Note 4 and Note 3, add a total of $4T_{OSC}$.
6. "Typical" specifications are untested and not guaranteed.

SYSTEM BUS TIMINGS

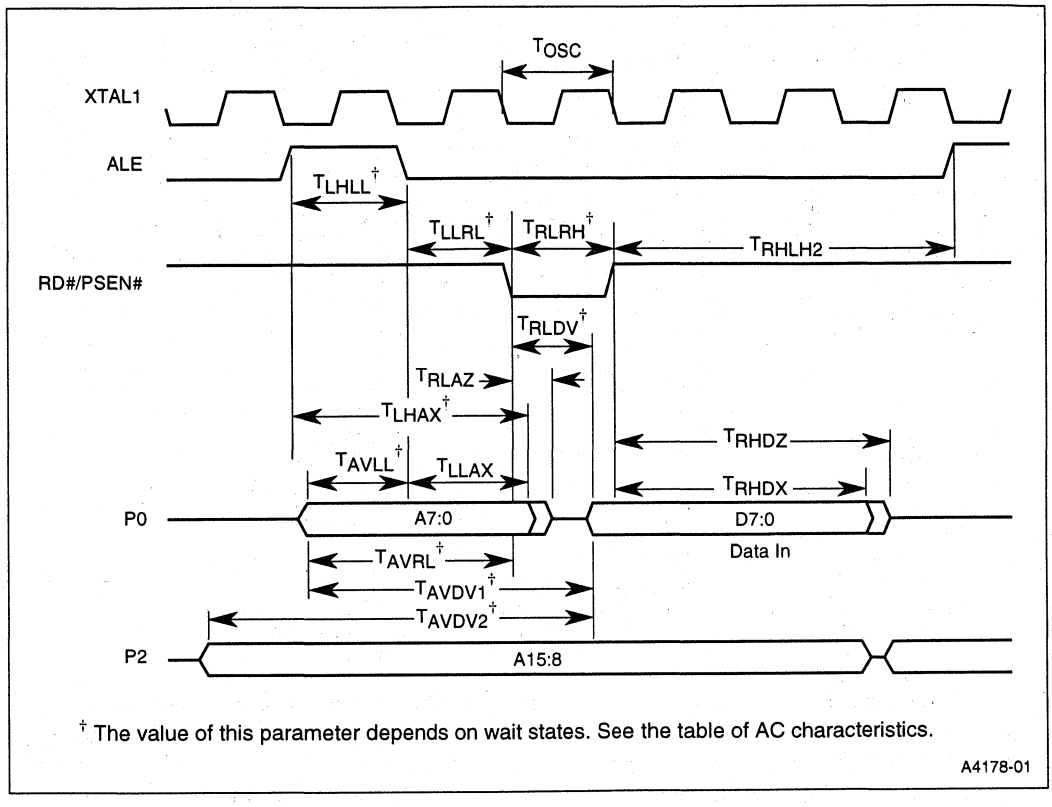
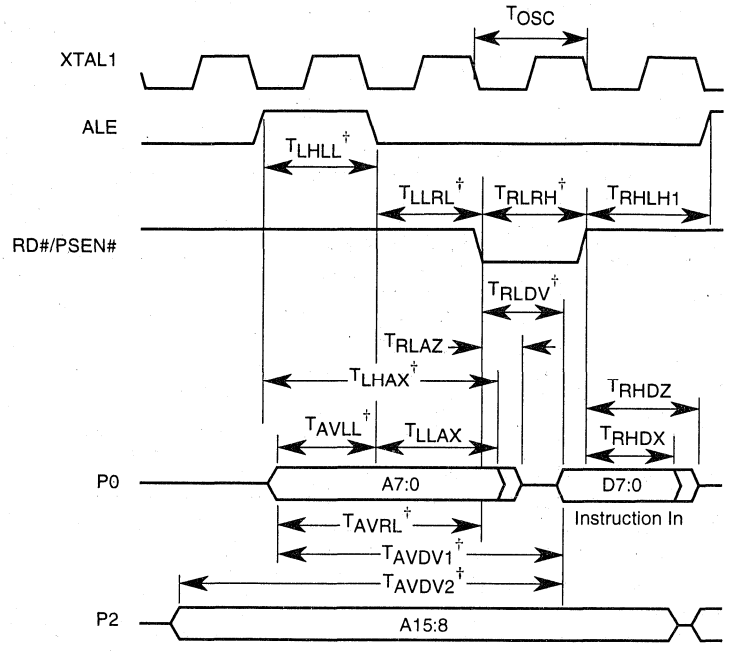


Figure 5. External Read Data Bus Cycle in Nonpage Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

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Figure 6. External Instruction Bus Cycle in Nonpage Mode

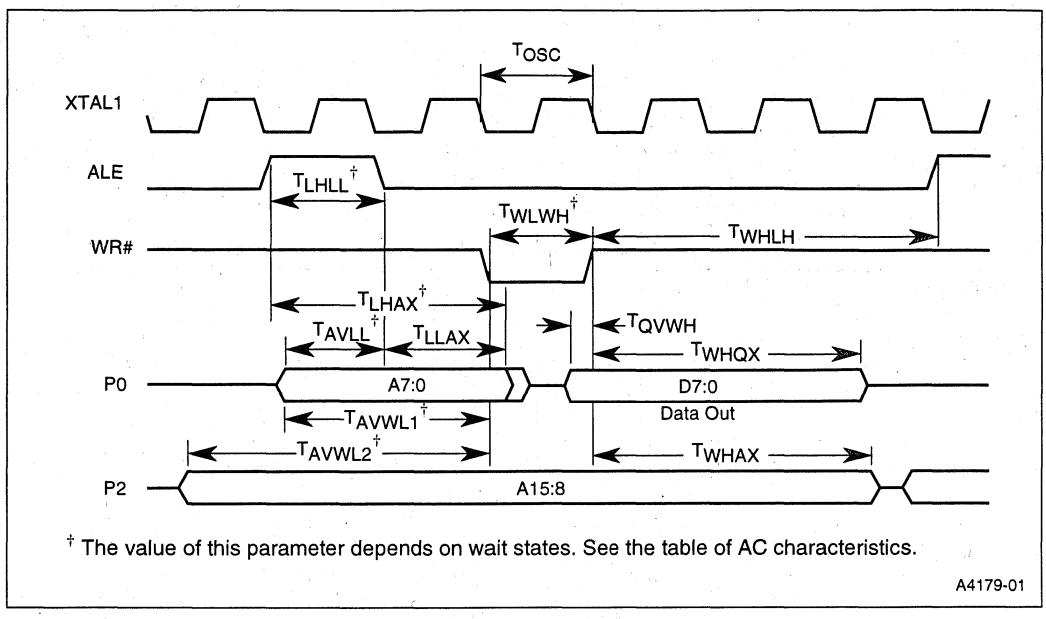


Figure 7. External Write Data Bus Cycle in Nonpage Mode

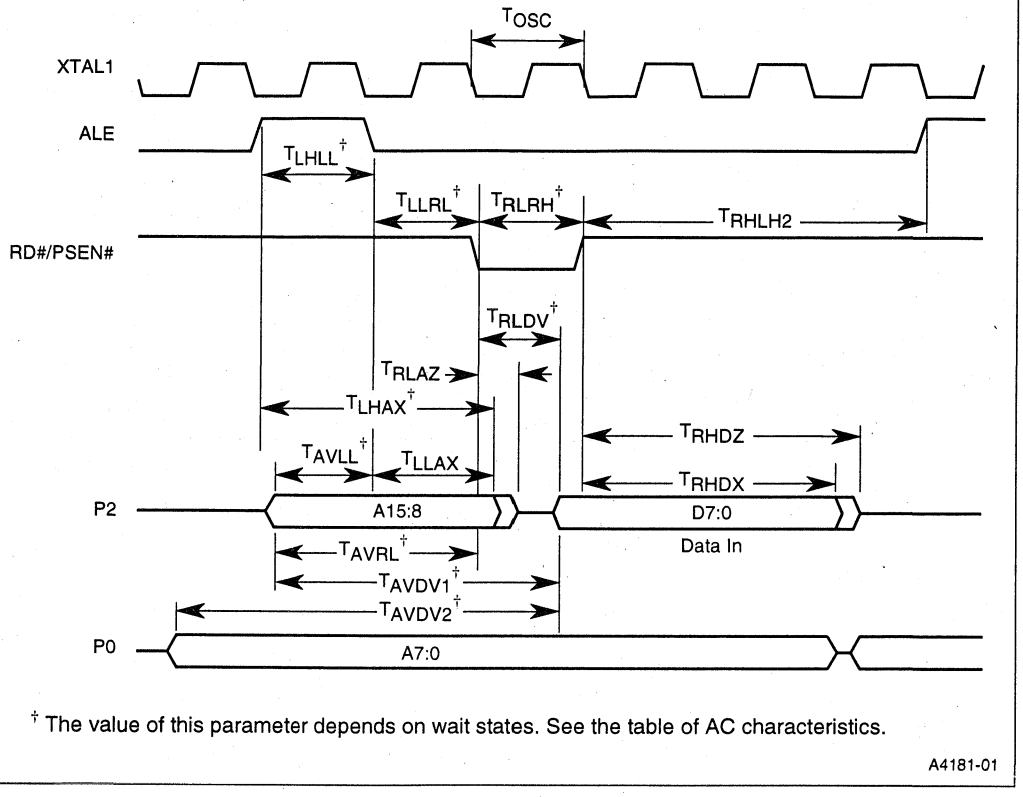


Figure 8. External Read Data Bus Cycle in Page Mode

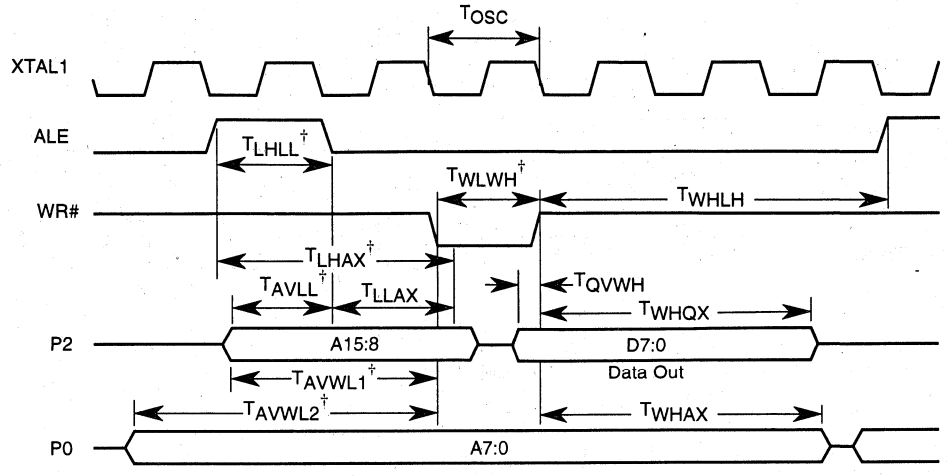
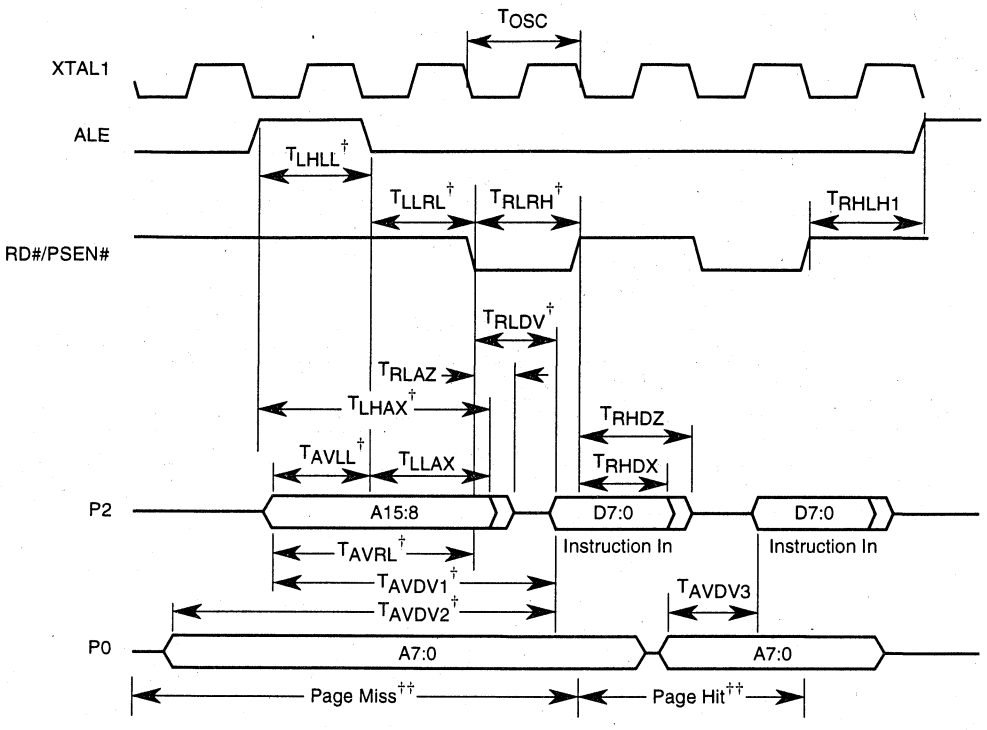


Figure 9. External Write Data Bus Cycle in Page Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

†† A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).

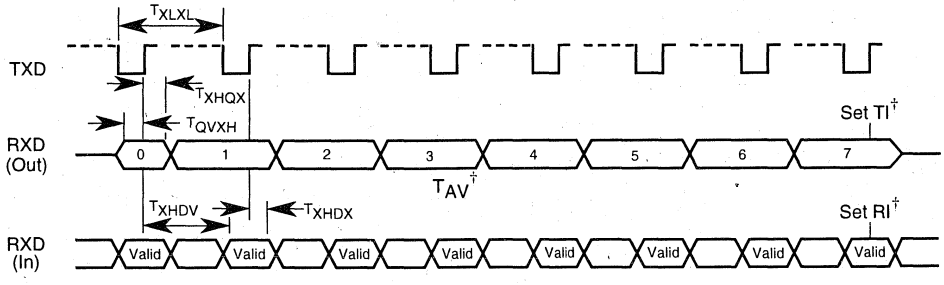
A4183-01

Figure 10. External Instruction Bus Cycle in Page Mode

AC Characteristics — Serial Port, Shift Register Mode

Table 10. Serial Port Timing — Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns



†TI and RI are set during S1P1 of the peripheral cycle following the shift of the eighth bit.

A2592-02

Figure 11. Serial Port Waveform — Shift Register Mode

External Clock Drive

Table 11. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency (F_{OSC})		16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

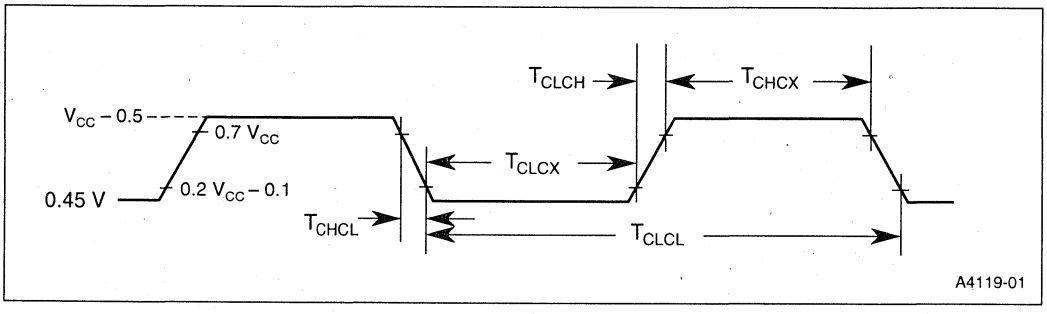


Figure 12. External Clock Drive Waveforms

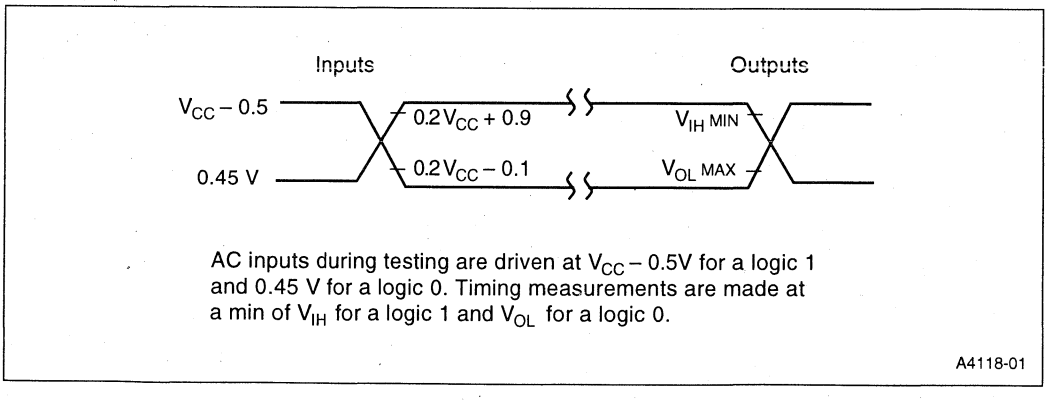
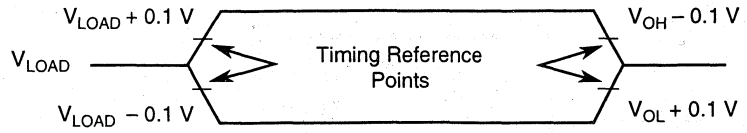


Figure 13. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm$ 20 mA.

A4117-01

Figure 14. Float Waveforms

PROGRAMMING AND VERIFYING NONVOLATILE MEMORY

The 8XC251SB has several areas of nonvolatile memory that can be programmed and/or verified: on-chip code memory (16 Kbytes), configuration bytes (2 bytes), lock bits (3 bits), encryption array (128 bytes), and signature bytes (3 bytes). The *8XC251SB User's Manual* (Order Number: 272617) provides procedures for programming and verifying the nonvolatile memory.

Figure 15 shows the setup for programming and/or verifying the nonvolatile memory. Table 12 lists the programming and verification operations and indicates which operations apply to the three versions of the 8XC251SB. It also specifies the signals on the programming input (PROG#) and the ports. The OTPROM/ROM mode (port 0) specifies the operation (program or verify) and the base address of the memory area. The addresses (ports 1 and 3) are relative to the base address. (The on-chip memory is at locations FF:0000H–FF:3FFFH of the memory address space. The other areas of the OTPROM/ROM are outside the memory address space and are accessible only during programming and verification.)

Configuration bytes CONFIG0 and CONFIG1 (Figures 16 and 17) define the configuration bits. Table 13 lists values of configuration bits for the 80C251SB.

Figure shows the waveforms for the programming and verification cycles, and Table 13 lists the timing specifications. The signature bytes of the 83C251SB and 87C251SB are factory programmed. Table 14 lists the addresses and the contents of the signature bytes.

NOTE

The V_{PP} source in Figure 15 must be well regulated and free of glitches. The voltage on the V_{PP} pin must not exceed the specified maximum, even under transient conditions.

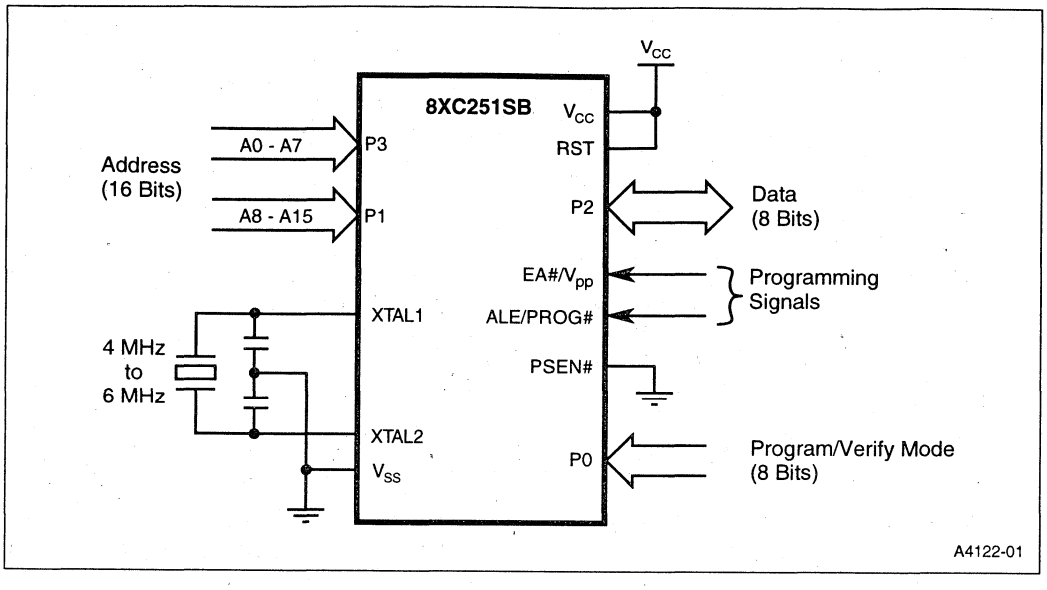


Figure 15. Setup for Programming and Verifying Nonvolatile Memory

Table 12. Programming and Verification Modes

Mode	8XC251SB			PROG#	P0	P2	Addresses P1 (high), P3 (low)	Notes
	X = 7	X = 3	X = 0					
Program on-chip code memory	Y			5 Pulses	68H	Data	0000H–3FFFH	1
Verify on-chip code memory	Y	Y		High	28H	Data	0000H–3FFFH	
Program configuration bytes	Y			5 Pulses	69H	Data	0080H–0083H	1, 2
Verify configuration bytes	Y	Y	Y	High	29H	Data	0080H–0083H	
Program lock bits	Y			25 Pulses	6BH	XX	0001H–0003H	1, 3
Verify lock bits	Y	Y		High	2BH	Data	0000H	4
Program encryption array	Y			25 Pulses	6CH	Data	0000H–007FH	1
Verify signature bytes	Y	Y		High	29H	Data	0030H, 0031H, 0060H	

NOTES:
1. The PROG# pulse waveform is shown in Figure .
2. The 8XC251SB uses only 2 bytes: 0080H and 0081H.
3. When programming the lock bits, the data bits on port 2 are don't care. Identify the lock bits with the address as follows: LB3 - 0003H, LB2 - 0002H, LB1 - 0001H
4. The three lock bits are verified in a single operation. The states of the lock bits appear simultaneously at port 2 as follows: LB3 - P2.3, LB2 - P2.2. LB1 - P2.1. High = programmed.

CONFIG0

7							0
—	—	WSA	XALE	RD1	RD0	PAGE	SRC

Bit Number	Bit Mnemonic	Function
7:6	—	Reserved; set these bits when writing to CONFIG0.
5	WSA	Wait State A: Clear this bit to generate one external wait state for memory regions 00:, FE:, and FF:. Set this bit for no wait states for these regions.
4	XALE	Extend Ale: If this bit is set, the time of the ALE pulse is T_{osc}. Clearing this bit extends the time of the ALE pulse from T_{osc} to $3T_{osc}$, which adds one external wait state.
3:2	RD1, RD0	RD# and PSEN# Function Select: RD1 RD0 RD# Range PSEN# Range Features 0 0 Reserved Reserved Reserved 0 1 RD# = A16 All addresses 128-Kbyte External Address Space 1 0 P3.7 only All addresses One additional port pin 1 1 ≤ 7F:FFFFH ≥ 80:0000H Compatible with MCS 51 microcontrollers
1	PAGE	Page Mode Select: Clear this bit for page-mode (A15:8/D7:0 on P2, and A7:0 on P0). Set this bit for nonpage-mode (A15:8 on P2, and A7:0/D7:0 on P0 (compatible with 44-lead PLCC MCS 51 microcontrollers)).
0	SRC	Source Mode/Binary Mode Select: Set this bit for source mode. Clear this bit for binary mode (binary-code compatible with MCS 51 microcontrollers).

Figure 16. Configuration Byte 0

CONFIG1

7							0
—	—	—	INTR	WSB	—	—	EMAP

Bit Number	Bit Mnemonic	Function
7:5	—	Reserved; set these bits when writing to CONFIG1.
4	INTR	Interrupt Mode: If this bit is set, interrupts push 4 bytes onto the stack (the 3 bytes of the PC register and the PSW1 register). If this byte is clear, interrupts push 2 bytes onto the stack (the 2 lower bytes of the PC register).
3	WSB	Wait State B: Clear this bit to generate one external wait state for memory region 01:. Set this bit for no wait states for region 01:.
2:1		Reserved; set these bits when writing to CONFIG1.
0	EMAP	EPROM MAP: Clearing this bit maps the upper 8 Kbytes of on-chip code memory (FF:2000H–FF:3FFFH) to 00:E000H–00:FFFFH. If this bit is set, the upper 8 Kbytes of on-chip code memory are mapped only to FF:2000H–FF:3FFFH.

Figure 17. Configuration Byte 1

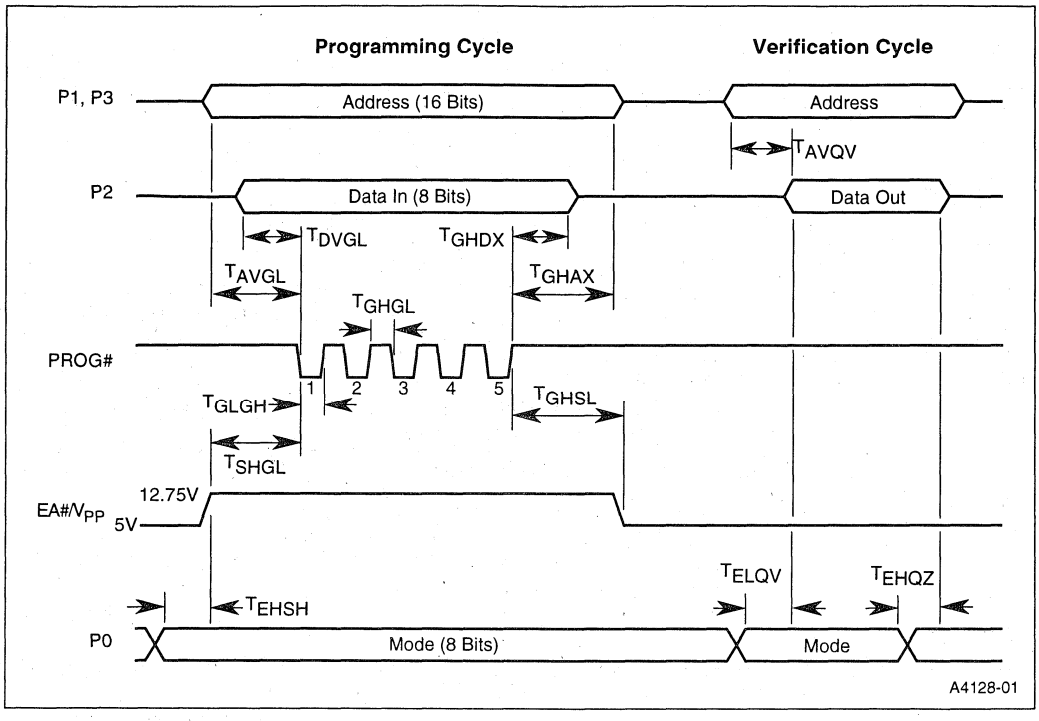


Figure 18. Timing for Programming and Verification of Nonvolatile Memory

Table 13. Nonvolatile Memory Programming and Verification Characteristics at T_A = 21 – 27 °C, V_{CC} = 5 V, and V_{SS} = 0 V

Symbol	Definition	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
F_{OSC}	Oscillator Frequency	4.0	6.0	MHz
T_{AVGL}	Address Setup to PROG# Low	$48T_{OSC}$		
T_{GHAX}	Address Hold after PROG#	$48T_{OSC}$		
T_{DVGL}	Data Setup to PROG# Low	$48T_{OSC}$		
T_{GHDX}	Data Hold after PROG#	$48T_{OSC}$		
T_{EHSH}	ENABLE High to V_{PP}	$48T_{OSC}$		
T_{SHGL}	V_{PP} Setup to PROG# Low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{GLGH}	PROG# Width	90	110	µs
T_{AVQV}	Address to Data Valid		$48T_{OSC}$	
T_{ELQV}	ENABLE Low to Data Valid		$48T_{OSC}$	
T_{EHQZ}	Data Float after ENABLE	0	$48T_{OSC}$	
T_{GHGL}	PROG# High to PROG# Low	10		µs

NOTE: Notation for timing parameters:

A = Address D = Data E = Enable G = PROG# H = High L = Low
Q = Data out S = Supply (V_{PP}) V = Valid X = No Longer Valid Z = Floating

Table 14. Contents of the Signature Bytes

Device	Address		
	30H	31H	60H
83C251SB	89H	40H	7BH
87C251SB	89H	40H	FBH

DATASHEET REVISION HISTORY

The following differences exist between the -001 revision and this -002 revision of the 8XC251SB datasheet:

1. All EXPRESS temperature information is removed.
2. The term "EC1" (PCA External Clock Input) in Table 7 is correctly stated as "ECI".
3. The description of bits RD0 and RD1 in configuration byte CONFIG1 (Table 7) correctly identifies states for 00 and 11 and matches other datasheet and user manual information.
4. The WR# (Write) bus control signal description is added to Table 7.
5. The V_{OH2} description is included in Table 8.
6. The RST (reset) resistor is correctly stated as a "pulldown" in Table 8.
7. The I_{PD}, I_{DL}, I_{CC}, T_{RLDV}, T_{AVDV1}, T_{AVDV2}, T_{AVDV3} Maximum specifications are revised.
8. An I_{PD} test condition replaces the I_{CC} test condition in Figure 4 and its caption.
9. T_{RLRH}, T_{WLWH}, T_{LHAX}, T_{AVRL}, T_{QVWH} Minumum specifications are revised.
10. T_{LHRL}, T_{RHLH} are deleted.
11. T_{LLRL}, T_{RHLH1}, T_{RHLH2} are new.
12. T_{RLAZ} is revised.
13. T_{AVWL1} is revised.
14. All timing diagrams relative to the foregoing changes are redrawn.
15. The Serial Port Waveform — Shift Register Mode figure is redrawn to indicate Set TI and Set RI.
16. Table 13, "Configuration Bit Values for 80C251SB and 80C251SB-16," is deleted.
17. The 12 MHz test condition for C_{IO} is now 16 MHz.

FUNCTIONAL DEVIATIONS

This section describes the functional deviations associated with the 8XC251SB -002 datasheet.

1. Certain instructions (listed below) result in register values incorrectly affecting the Negative Flag (N) of PSW1. These register values should set or clear the Negative Flag based on the value of result bit 15. The 8XC251SB ALU currently sets and clears the Negative Flag based on result bit seven when using these specific instructions. Follow affected instructions with an ANL WRj,WRj operation. This forces the ALU Negative Flag to operate on the value of result bit 15. The net impact is the additional ANL instruction time to gain correct Negative Flag results. The following Instructions are affected by this deviation:

SRL WRj
SRA WRj
SLL WRj
INC WRj,#short
DEC WRj,#short

2. WSb in the CONFIG1 configuration register controls the number of wait states for MOVX instructions in memory locations 01:0000H through 01:FFFFH. This includes both MOVX @DPTR as well as the MOVX @Ri instruction. The device currently uses WSa in the CONFIG0 configuration register for the MOVX @Ri instruction. If possible, configure both WSa and WSb to the same value. This results in identical wait-state operation for both MOVX @DPTR and MOVX @Ri. If the two CONFIGx bits must be configured differently, restrict the use of MOVX commands to the MOVX @DPTR format.

3. Use of EJMP instructions for extended jumps between 64-Kbyte regions do not result in the correct destination. Do not use the EJMP instruction.

4. Jump instructions with an address range of +127/-128 do not jump across the FF:XXXXH to FE:XXXXH 64-Kbyte region boundary. Issuing a jump instruction within range of this boundary results in a destination within the same FF:XXXXH region. Do not use jump instructions to cross this memory boundary. All +127/-128 jump instructions issued across other 64-Kbyte region boundaries operate as described. The affected instructions for the FF:XXXXH to FE:XXXXH region jump deviation are SJMP, CJNE, DJNZ, JB, JBC, JC, JE, JG, JLE, JNB, JNC, JNE, JNZ, JSG, JSGE, JSL, JSLE, and JZ.

PRELIMINARY

8XC251SA/SB/SP/SQ HIGH-PERFORMANCE CHMOS MICROCONTROLLER

Commercial/Express

- Real-time and Programmed Wait State Bus Operation
- Binary-code Compatible with MCS® 51
- Pin Compatible with 44-pin PLCC and 40-pin PDIP MCS 51 Sockets
- Register-based MCS® 251 Architecture
  - 40-byte Register File
  - Registers Accessible as Bytes, Words, or Double Words
- Enriched MCS 51 Instruction Set
  - 16-bit and 32-bit Arithmetic and Logic Instructions
  - Compare and Conditional Jump Instructions
  - Expanded Set of Move Instructions
- Linear Addressing
- 256-Kbyte Expanded External Code/Data Memory Space
- ROM/OTPROM/EPROM Options: 16 Kbytes (SB/SQ), 8 Kbytes (SA/SP), or without ROM/OTPROM/EPROM
- 16-bit Internal Code Fetch
- 64-Kbyte Extended Stack Space
- On-chip Data RAM Options: 1-Kbyte (SA/SB) or 512-Byte (SP/SQ)
- 8-bit, 2-clock External Code Fetch in Page Mode
- Fast MCS 251 Instruction Pipeline
- User-selectable Configurations:
  - External Wait States (0-3 wait states)
  - Address Range & Memory Mapping
  - Page Mode
- 32 Programmable I/O Lines
- Seven Maskable Interrupt Sources with Four Programmable Priority Levels
- Three Flexible 16-bit Timer/counters
- Hardware Watchdog Timer
- Programmable Counter Array
  - High-speed Output
  - Compare/Capture Operation
  - Pulse Width Modulator
  - Watchdog Timer
- Programmable Serial I/O Port
  - Framing Error Detection
  - Automatic Address Recognition
- High-performance CHMOS Technology
- Static Standby to 16-MHz Operation
- Complete System Development Support
  - Compatible with Existing Tools
  - New MCS 251 Tools Available: Compiler, Assembler, Debugger, ICE
- Package Options (PDIP, PLCC, and Ceramic DIP)

A member of the Intel family of 8-bit MCS 251 microcontrollers, the 8XC251SA/SB/SP/SQ is binary-code compatible with MCS 51 microcontrollers and pin compatible with 40-pin PDIP and 44-pin PLCC MCS 51 microcontrollers. MCS 251 microcontrollers feature an enriched instruction set, linear addressing, and efficient C-language support. The 8XC251SA/SB/SP/SQ has 512 bytes or 1 Kbyte of on-chip RAM and is available with 8 Kbytes or 16 Kbytes of on-chip ROM/OTPROM/EPROM, or without ROM/OTPROM/EPROM. A variety of features can be selected by new user-programmable configurations.

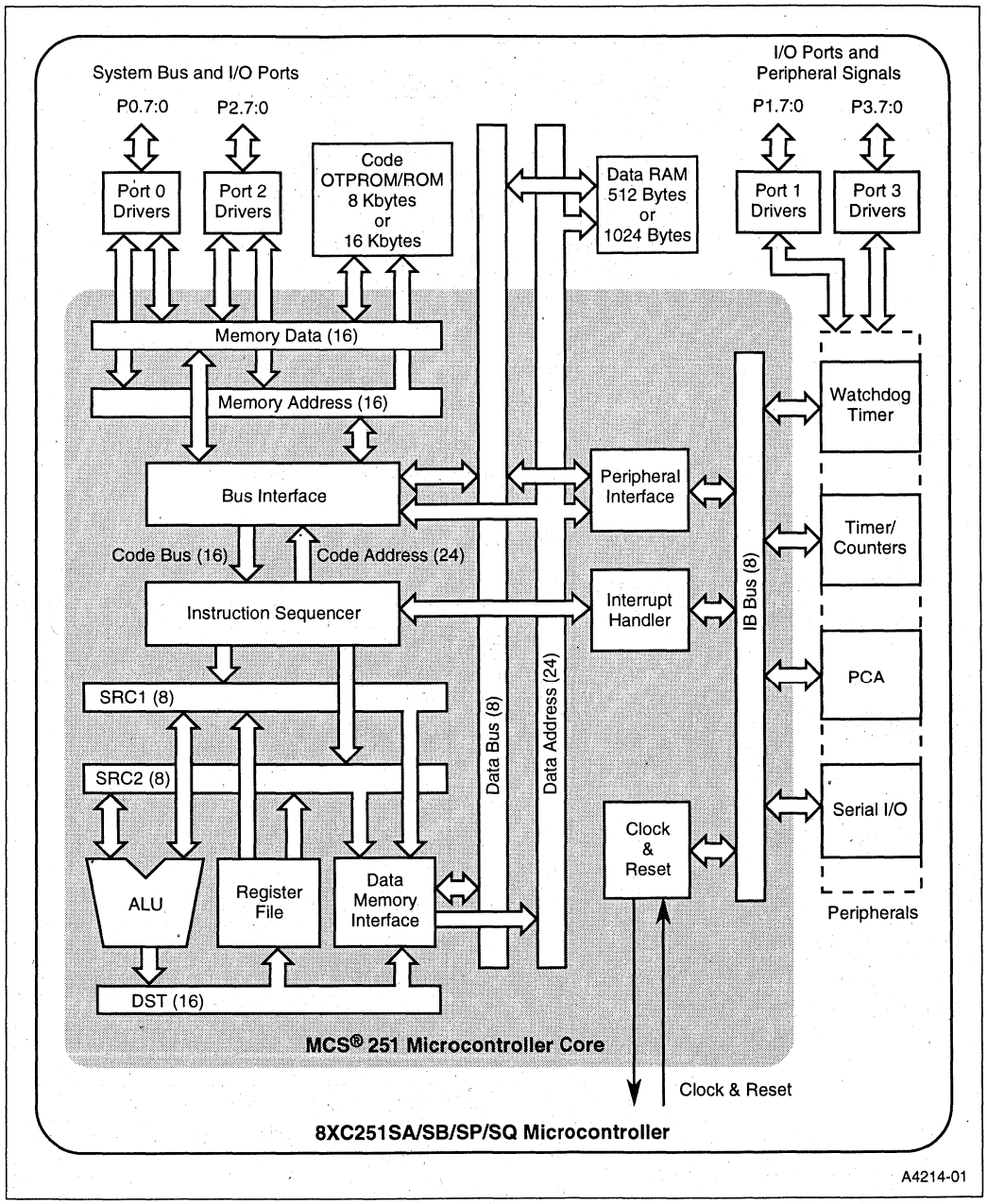


Figure 1. 8XC251SA/SB/SP/SQ Block Diagram

1.0 NOMENCLATURE

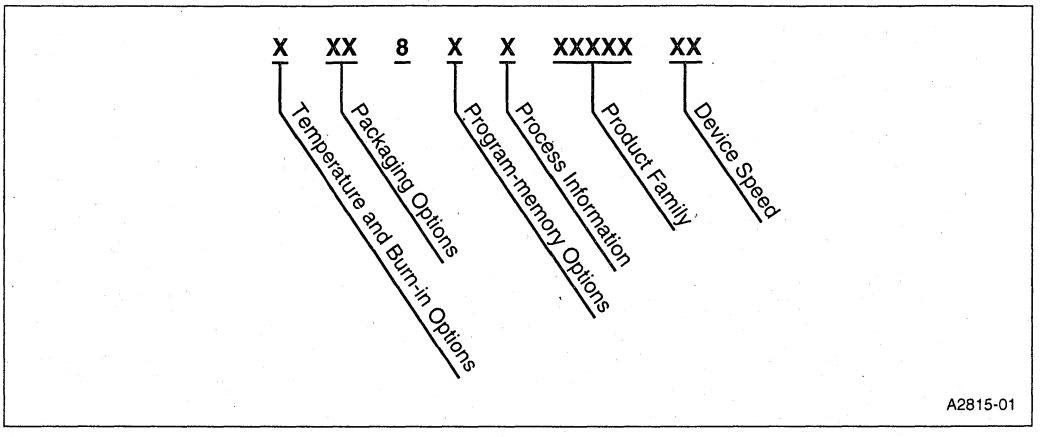


Figure 2. The 8XC251SA/SB/SP/SQ Family Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
	T	Express operating temperature range (-40°C to 85°C) with Intel standard burn-in.
Packaging Options	N	44-pin Plastic Leaded Chip Carrier (PLCC)
	P	40-pin Plastic Dual In-line Package (PDIP)
	C	40-pin Ceramic Dual In-line Package (Ceramic DIP)
Program Memory Options	0	Without ROM/OTPROM/EPROM
	3	ROM
	7	User programmable OTPROM/EPROM
Process Information	C	CHMOS
Product Family	251	8-bit control architecture
Device Memory Options	SA	1-Kbyte RAM/8-Kbyte ROM/OTPROM/EPROM
	SB	1-Kbyte RAM/16-Kbyte ROM/OTPROM/EPROM or without ROM/OTPROM/EPROM
	SP	512-byte RAM/8-Kbyte ROM/OTPROM/EPROM
	SQ	512-byte RAM/16-Kbyte ROM/OTPROM/EPROM or without ROM/OTPROM/EPROM
Device Speed	16	External clock frequency

Table 2 lists the proliferation options. See Figure 2 for the 8XC251SA/SB/SP/SQ family nomenclature.

Table 2. Proliferation Options

8XC251SA/SB/SP/SQ (0 – 16 MHz; 5 V ±10%)	
80C251SB16	CPU-only
80C251SQ16	CPU-only
83C251SA16	ROM
83C251SB16	ROM
83C251SP16	ROM
83C251SQ16	ROM
87C251SA16	OTPROM/EPROM
87C251SB16	OTPROM/EPROM
87C251SP16	OTPROM/EPROM
87C251SQ16	OTPROM/EPROM

Table 3 lists the 8XC251SA/SB/SP/SQ packages.

Table 3. Package Information

Pkg.	Definition	Temperature
N	44 ld. PLCC	0°C to +70°C
P	40 ld. Plastic DIP	0°C to +70°C
C	40 ld. Ceramic DIP	0°C to +70°C
TN	44 ld. PLCC	-40°C to +85°C
TP	40 ld. Plastic DIP	-40°C to +85°C

2.0 PINOUT

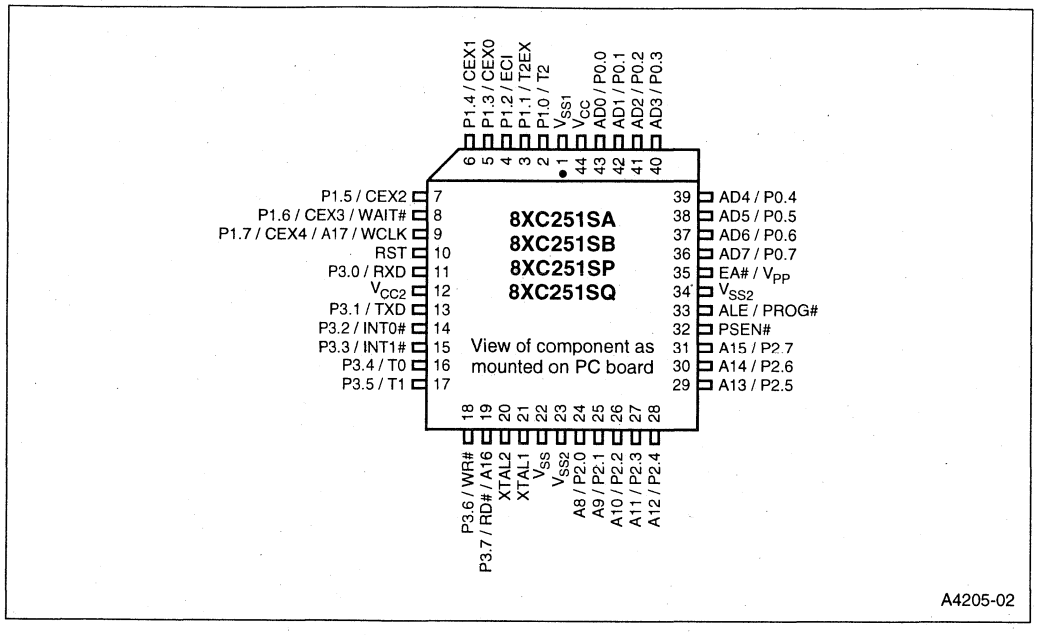


Figure 3. 8XC251SA/SB/SP/SQ 44-pin PLCC Package

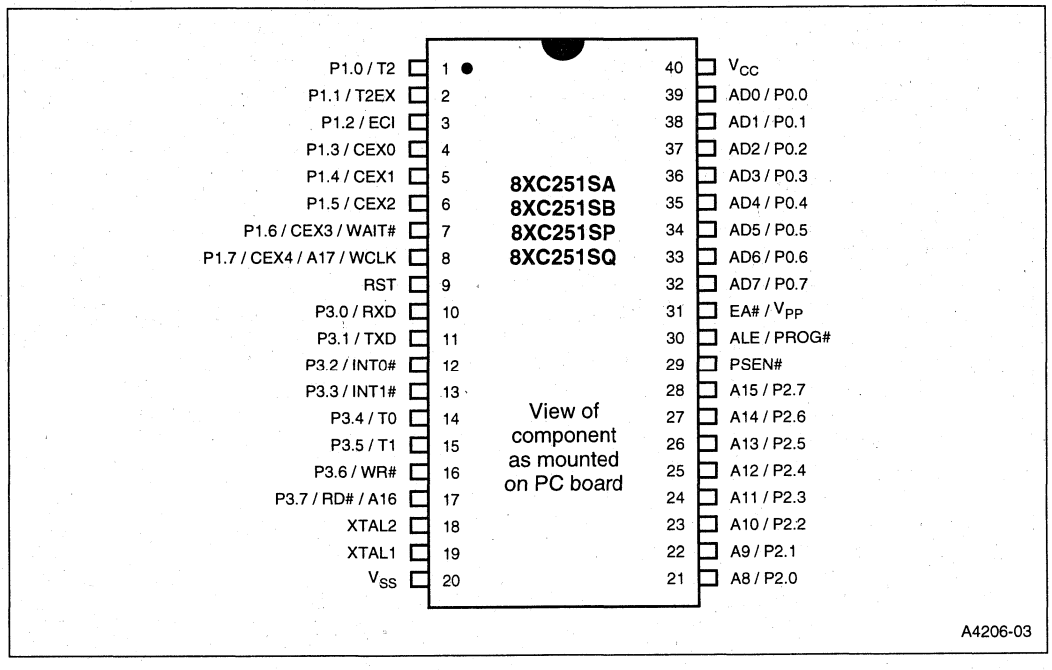


Figure 4. 8XC251SA/SB/SP/SQ 40-pin PDIP and Ceramic DIP Packages

Table 4. 8XC251SA/SB/SP/SQ Pin Assignment

PLCC	DIP	Name
1		V_{SS1}
2	1	P1.0/T2
3	2	P1.1/T2EX
4	3	P1.2/ECI
5	4	P1.3/CEX0
6	5	P1.4/CEX1
7	6	P1.5/CEX2
8	7	P1.6/CEX3/WAIT#
9	8	P1.7/CEX4/A17/WCLK
10	9	RST
11	10	P3.0/RXD
12		V_{CC2}
13	11	P3.1/TXD
14	12	P3.2/INT0#
15	13	P3.3/INT1#
16	14	P3.4/T0
17	15	P3.5/T1
18	16	P3.6/WR#
19	17	P3.7/RD#/A16
20	18	XTAL2
21	19	XTAL1
22	20	V_{SS}

PLCC	DIP	Name
23		V_{SS2}
24	21	A8/P2.0
25	22	A9/P2.1
26	23	A10/P2.2
27	24	A11/P2.3
28	25	A12/P2.4
29	26	A13/P2.5
30	27	A14/P2.6
31	28	A15/P2.7
32	29	PSEN#
33	30	ALE/PROG#
34		V_{SS2}
35	31	EA#/V_{PP}
36	32	AD7/P0.7
37	33	AD6/P0.6
38	34	AD5/P0.5
39	35	AD4/P0.4
40	36	AD3/P0.3
41	37	AD2/P0.2
42	38	AD1/P0.1
43	39	AD0/P0.0
44	40	V_{CC}

Table 5. 8XC251SA/SB/SP/SQ PLCC/DIP Pin Assignments Arranged by Functional Category

Address & Data		
Name	**PLCC**	**DIP**
AD0/P0.0	43	39
AD1/P0.1	42	38
AD2/P0.2	41	37
AD3/P0.3	40	36
AD4/P0.4	39	35
AD5/P0.5	38	34
AD6/P0.6	37	33
AD7/P0.7	36	32
A8/P2.0	24	21
A9/P2.1	25	22
A10/P2.2	26	23
A11/P2.3	27	24
A12/P2.4	28	25
A13/P2.5	29	26
A14/P2.6	30	27
A15/P2.7	31	28
P3.7/RD#/A16	19	17
P1.7/CEX4/A17/WCLK	9	8

Input/Output		
Name	**PLCC**	**DIP**
P1.0/T2	2	1
P1.1/T2EX	3	2
P1.2/ECI	4	3
P1.3/CEX0	5	4
P1.4/CEX1	6	5
P1.5/CEX2	7	6
P1.6/CEX3/WAIT#	8	7
P1.7/CEX4/A17/WCLK	9	8
P3.0/RXD	11	10
P3.1/TXD	13	11
P3.4/T0	16	14
P3.5/T1	17	15

Power & Ground		
Name	**PLCC**	**DIP**
V_{CC}	44	40
V_{CC2}	12	
V_{SS}	22	20
V_{SS1}	1	
V_{SS2}	23, 34	
EA#/V_{PP}	35	31

Processor Control		
Name	**PLCC**	**DIP**
P3.2/INT0#	14	12
P3.3/INT1#	15	13
EA#/V_{PP}	35	31
RST	10	9
XTAL1	21	18
XTAL2	20	19

Bus Control & Status		
Name	**PLCC**	**DIP**
P3.6/WR#	18	16
P3.7/RD#/A16	19	17
ALE/PROG#	33	30
PSEN#	32	29

3.0 SIGNALS

Table 6. Signal Descriptions

Signal Name	Type	Description	Alternate Function
A17	O	**18th Address Bit (A17).** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0 (see Chapter 4, "Device Configuration," of the 8XC251SA/SB/SP/SQ Embedded Microcontroller User's Manual). See also RD# and PSEN#.	P1.7/CEX4/ WCLK
A16	O	**Address Line 16.** See RD#.	RD#
A15:8†	O	**Address Lines.** Upper address lines for the external bus.	P2.7:0
AD7:0†	I/O	**Address/Data Lines.** Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable.** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	PROG#
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Pins.** These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.6:3 P1.7/A17/ WAIT#
EA#	I	**External Access.** Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is to on-chip ROM/OTPROM/EPROM if the address is within the range of the on-chip ROM/OTPROM/EPROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without on-chip ROM/OTPROM/EPROM, EA# must be strapped to ground.	V_{PP}
ECI	I	**PCA External Clock Input.** External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1.** These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
PROG#	I	**Programming Pulse.** The programming pulse is applied to this pin for programming the on-chip OTPROM.	ALE
P0.7:0	I/O	**Port 0.** This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1.** This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI CEX3:0 CEX4/A17/ WAIT#/ WCLK
P2.7:0	I/O	**Port 2.** This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-pin PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 6. Signal Descriptions (Continued)

Signal Name	Type	Description	Alternate Function
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3.** This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#/A16
PSEN#	O	**Program Store Enable.** Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte UCONFIG0 (see RD# and Chapter 4, "Device Configuration," in the 8XC251SA/SB/SP/SQ Embedded Microcontroller User's Manual).	—
RD#	O	**Read or 17th Address Bit (A16).** Read signal output to external data memory or 17th external address bit (A16), depending on the values of bits RD0 and RD1 in configuration byte UCONFIG0. (See PSEN# and Chapter 4, "Device Configuration," in the 8XC251SA/SB/SP/SQ Embedded Microcontroller User's Manual).	P3.7/A16
RST	I	**Reset.** Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this pin and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data.** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
T1:0	I	**Timer 1:0 External Clock Inputs.** When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output.** For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input.** In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data.** TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
V_{CC}	PWR	**Supply Voltage.** Connect this pin to the +5V supply voltage.	—
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this pin to the +5V supply voltage is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-pin PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 6. Signal Descriptions (Continued)

Signal Name	Type	Description	Alternate Function
V_{PP}	I	**Programming Supply Voltage**. The programming supply voltage is applied to this pin for programming the on-chip OTPROM/EPROM.	EA#
V_{SS}	GND	**Circuit Ground**. Connect this pin to ground.	—
V_{SS1}	GND	**Secondary Ground**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SA/SB/SP/SQ as a pin-for-pin replacement for the 8XC51BH, V_{SS1} can be unconnected without loss of compatibility. (Not available on DIP)	—
V_{SS2}	GND	**Secondary Ground 2**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility. (Not available on DIP)	—
WAIT#	I	**Real-time Wait State Input.** The real-time WAIT# input is enabled by writing a logical '1' to the WCON.0 (RTWE) bit at S:A7H. During bus cycles, the external memory system can signal 'system ready' to the microcontroller in real time by controlling the WAIT# input signal on the port 1.6 input.	P1.6/CEX3
WCLK	O	**Wait Clock Output.** The real-time WCLK output is driven at port 1.7 (WCLK) by writing a logical '1' to the WCON.1 (RTWCE) bit at S:A7H. When enabled, the WCLK output produces a square wave signal with a period of one-half the oscillator frequency.	P1.7/CEX4/ A17
WR#	O	**Write**. Write signal output to external memory.	P3.6
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	—
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	—

† The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-pin PLCC and 40-pin DIP MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Memory Signal Selections (RD1:0)

RD1:0	P1.7/CEX/ A17/WCLK	P3.7/RD#/A16	PSEN#	WR#	Features
0 0	A17	A16	Asserted for all addresses	Asserted for writes to all memory locations	256-Kbyte external memory
0 1	P1.7/CEX4/ WCLK	A16	Asserted for all addresses	Asserted for writes to all memory locations	128-Kbyte external memory
1 0	P1.7/CEX4/ WCLK	P3.7 only	Asserted for all addresses	Asserted for writes to all memory locations	64-Kbyte external memory. One additional port pin.
1 1	P1.7/CEX4/ WCLK	RD# asserted for addresses ≤ 7F:FFFFH	Asserted for ≥ 80:0000H	Asserted only for writes to MCS 51 microcontroller data memory locations.	64-Kbyte external memory. Compatible with MCS 51 micro-controllers.

4.0 ADDRESS MAP

Table 8. 8XC251SA/SB/SP/SQ Address Map

Internal Address)	Description	Notes
FF:FFFFH FF:4000H	External Memory except the top eight bytes (FF:FFF8H–FF:FFFFH) which are reserved for the configuration array.	1, 3, 10
FF:3FFFH FF:0000H	External memory or on-chip nonvolatile memory (8Kbytes FF:0000H - FF:1FFFH, 16Kbytes FF:0000H - FF:3FFFH).	3, 4, 5
FE:FFFFH FE:0000H	External Memory	3
FD:FFFFH 02:0000H	Reserved	6
01:FFFFH 01:0000H	External Memory	3
00:FFFFH 00:E000H	External memory or with configuration bit EMAP# = 0, addresses in this range access on-chip code memory in region FF: (16 Kbyte devices only).	5, 7
00:DFFFH 00:0420H	External Memory	7
00:041FH 00:0080H	On-chip RAM (512 bytes 00:0020H - 00:021FH, 1024 bytes 00:0020H - 00:041FH)	7
00:007FH 00:0020H	On-chip RAM	8
00:001FH 00:0000H	Storage for R0–R7 of Register File	2, 9

NOTES:
1. 18 address lines are bonded out (A15:0, A16:0, or A17:0 selected during chip configuration).
2. The special function registers (SFRs) and the register file have separate internal address spaces.
3. Data in this area is accessible by indirect addressing only.
4. Devices reset into internal or external starting locations depending on the state of EA# and configuration byte information See EA#. See also UCONFIG1:0 bit definitions in the 8XC251SA/SB/SP/SQ Embedded Microcontroller User's Manual.
5. The 16-Kbyte ROM/OTPROM/EPROM devices allow internal locations FF:2000H–FF:3FFFH to map into region 00:. In this case, if EA# = 1, a data read to 00:E000H–00:FFFFH is redirected to internal ROM/OTPROM/EPROM (see bit 1 in UCONFIG0). This is not available for 8-Kbyte ROM/OTPROM/EPROM devices.
6. This reserved area returns indeterminate values.
7. Data is accessible by direct and indirect addressing.
8. Data is accessible by direct, indirect, and bit addressing.
9. Data is accessible by direct, indirect, and register addressing.
10. Eight addresses at the top of all external memory maps are reserved for current and future device configuration byte information.

5.0 ELECTRICAL CHARACTERISTICS

NOTICE: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Voltage on EA#/V_{PP} Pin to V_{SS}	0 V to +13.0 V
Voltage on Any other Pin to V_{SS}	-0.5 V to +6.5 V
I_{OL} per I/O Pin	15 mA
Power Dissipation	1.5 W

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias):	
Commercial	0°C to +70°C
Express	-40°C to +85°C
V_{CC} (Digital Supply Voltage)	4.5 V to 5.5 V
V_{SS}	0 V

† ***WARNING**: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTE

Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

5.1 D.C. Characteristics

Parameter values apply to all devices unless otherwise indicated.

Table 9. DC Characteristics at V_{CC} = 4.5 – 5.5 V

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	-0.5		$0.2V_{CC} - 0.1$	V	
V_{IL1}	Input Low Voltage (EA#)	0		$0.2V_{CC} - 0.3$	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (Note 1, Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (Note 1, Note 2)
V_{OH}	Output High Voltage (Port 1, 2, 3, ALE, PSEN#)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA (Note 3)

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   - port 0: 26 mA
   - ports 1–3: 15 mA

   Maximum Total I_{OL} for all output pins: 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.

Table 9. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Continued)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{OH2}	Output High Voltage (Port 2 in External Address during Page Mode)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)			-50	µA	VIN = 0.45 V
I_{LI}	Input Leakage Current (Port 0)			+/-10	µA	0.45 < VIN < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Port 1, 2, 3)			-650	µA	VIN = 2.0 V
R_{RST}	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10 (Note 4)		pF	F_{OSC} = 16 MHz T_A = 25 °C
I_{PD}	Powerdown Current		10 (Note 4)	20	µA	
I_{DL}	Idle Mode Current		12 (Note 4)	15	mA	F_{OSC} = 16 MHz
I_{CC}	Operating Current		45 (Note 4)	80	mA	F_{OSC} = 16 MHz

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   - port 0: 26 mA
   - ports 1–3: 15 mA

   Maximum Total I_{OL} for all output pins: 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25°C and are not guaranteed.

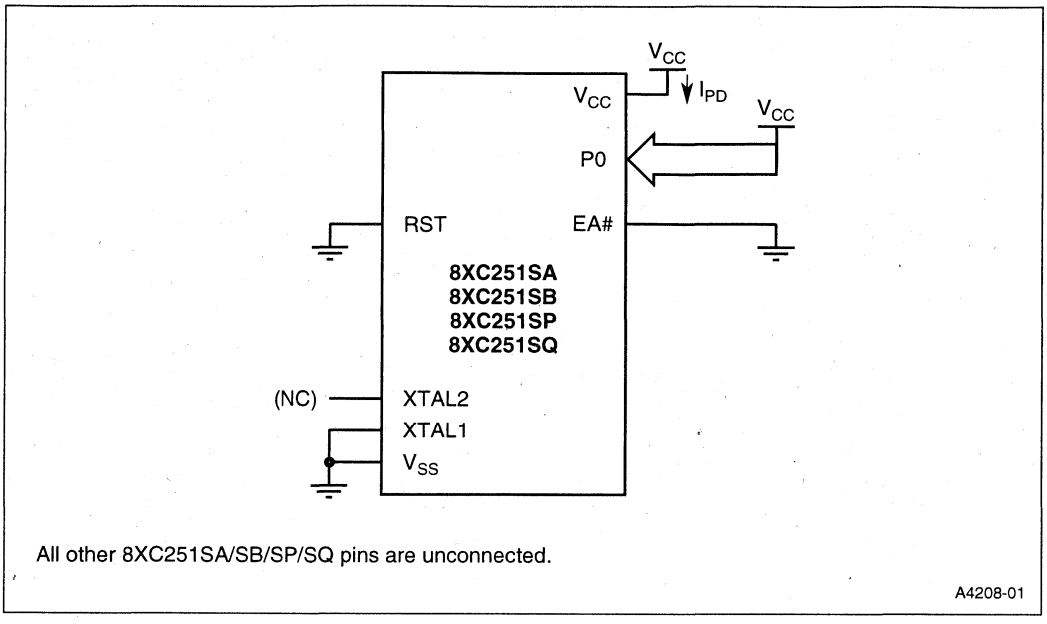


Figure 5. I_{PD} Test Condition, Powerdown Mode, V_{CC} = 2.0 – 5.5V

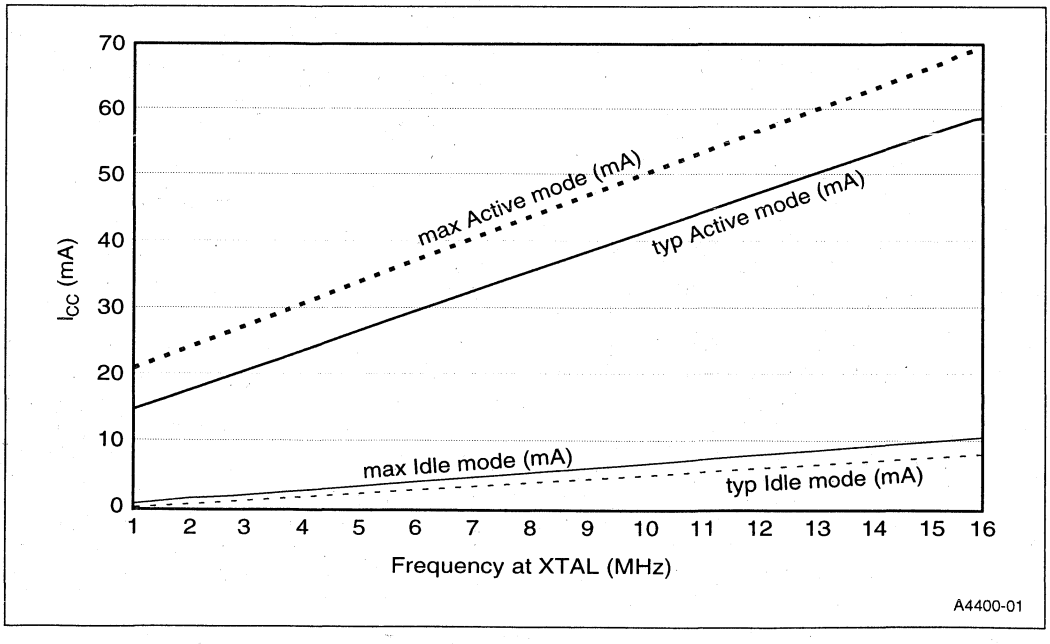


Figure 6. I_{CC} vs. Frequency (Mhz)

5.2 Definition of AC Symbols

Table 10. AC Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#/PSEN#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

5.3 A.C. Characteristics

Test Conditions: Capacitive load on all pins = 50 pF.

Table 11 lists AC timing parameters for the 8XC251SA/SB/SP/SQ with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and/or by extending ALE. In the table, Notes 3 and 5 mark parameters affected by an ALE wait state, and Notes 4 and 5 mark parameters affected by a PSEN#/RD#/WR# wait state.

Figures 8–10 show the bus cycles with the timing parameters.

Table 11. AC Characteristics

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
F_{OSC}	XTAL1 Frequency	N/A	N/A	0	16	MHz
T_{OSC}	$1/F_{OSC}$ @ 12 MHz @ 16 MHz	N/A	N/A	 83.3 62.5		ns
T_{LHLL}	ALE Pulse Width @ 12 MHz @ 16 MHz	 73.3 52.5		 (1+2M) $T_{osc}-10$		ns (3)
T_{AVLL}	Address Valid to ALE Low @ 12 MHz @ 16 MHz	 58.3 37.5		 (1+2M) $T_{osc}-25$		ns (3)
T_{LLAX}	Address Hold after ALE Low @ 12 MHz @ 16 MHz	 15 15		 15		ns

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M=Number of wait states (0 or 1) for ALE.
4. In the formula, N=Number of wait states (0,1,2, or 3) for RD#/PSEN#/WR#.
5. "Typical" specifications are untested and not guaranteed.

Table 11. AC Characteristics (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{RLRH} (2)	RD# or PSEN# Pulse Width @ 12 MHz @ 16 MHz	 146.6 105		 2(1+N) T_{osc} – 20		ns (4)
T_{WLWH}	WR# Pulse Width @ 12 MHz @ 16 MHz	 146.6 105		 2(1+N) T_{osc} – 20		ns (4)
T_{LLRL} (2)	ALE Low to RD# or PSEN# Low @ 12 MHz @ 16 MHz	 58.3 37.5		 T_{osc} – 25		ns
T_{LHAX}	ALE High to Address Hold @ 12 MHz @ 16 MHz	 83.3 62.5		 (1+2M)T_{osc}		ns (3)
T_{RLDV} (2)	RD#/PSEN# Low to valid Data/Instruction In @ 12 MHz @ 16 MHz		 106.6 65		 2(1+N) Tosc – 60	ns (4)
T_{RHDX} (2)	Data/Instruction Hold Time. Occurs after RD#/PSEN# are exerted to V_{OH}	0		0		ns
T_{RLAZ} (2)	RD#/PSEN# Low to Address Float	Typ.=0 (5)	2	Typ. = 0 (5)	2	ns
T_{RHDZ1}	Instruction Float after RD#/PSEN# High commercial @ 12 MHz and 16 MHz express @ 12 MHz and 16 MHz	 Typ.=2 5 Typ.=2 5 (5)	 18 10	 Typ.=25 Typ.=25 (5)	 18 10	ns
T_{RHDZ2}	Data Float after RD#/PSEN# High @ 12 MHz @ 16 MHz		 156.6 115		 2Tosc – 10	ns
T_{RHLH1}	RD#/PSEN# High to ALE High (Instruction) @ 12 MHz @ 16 MHz	 10 10		 10		ns
T_{RHLH2}	RD#/PSEN# High to ALE High (Data) @ 12 MHz @ 16 MHz	 156.6 115		 $2T_{osc}$ - 10		ns
T_{WHLH}	WR# High to ALE High @ 12 MHz @ 16 MHz	 171.6 130		 $2T_{osc}$ + 5		ns

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M=Number of wait states (0 or 1) for ALE.
4. In the formula, N=Number of wait states (0,1,2, or 3) for RD#/PSEN#/WR#.
5. "Typical" specifications are untested and not guaranteed.

Table 11. AC Characteristics (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{AVDV1}	Address (P0) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 243.2 160		 4(1+M/2) T_{osc} – 90	ns (3)
T_{AVDV2}	Address (P2) Valid to Valid Data/Instruction In @ 12 MHz @ 16 MHz		 268.2 185		 4(1+M/2) T_{osc} – 65	ns (3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In @ 12 MHz @ 16 MHz		 116.6 75		 $2T_{osc}$ – 50	ns
T_{AVRL} (2)	Address Valid to RD#/PSEN# Low @ 12 MHz @ 16 MHz	 121.6 80		 2(1+M) T_{osc} – 45		ns (3)
T_{AVWL1}	Address (P0) Valid to WR# Low @ 12 MHz @ 16 MHz	 126.6 85		 2(1+M) T_{osc} – 40		ns (3)
T_{AVWL2}	Address (P2) Valid to WR# Low @ 12 MHz @ 16 MHz	 146.6 105		 2(1+M) T_{osc} – 20		ns (3)
T_{WHQX}	Data Hold after WR# High @ 12 MHz @ 16 MHz	 63.3 42.5		 T_{osc} – 20		ns
T_{QVWH}	Data Valid to WR# High @ 12 MHz @ 16 MHz	 138.6 97		 2(1+N) T_{osc} – 28		ns (4)
T_{WHAX}	WR# High to Address Hold @ 12 MHz @ 16 MHz	 156.6 115		 $2T_{osc}$ – 10		ns

NOTES:
1. 16 MHz.
2. Specifications for PSEN# are identical to those for RD#.
3. In the formula, M=Number of wait states (0 or 1) for ALE.
4. In the formula, N=Number of wait states (0,1,2, or 3) for RD#/PSEN#/WR#.
5. "Typical" specifications are untested and not guaranteed.

5.3.1 EXTERNAL BUS CYCLES, NONPAGE MODE

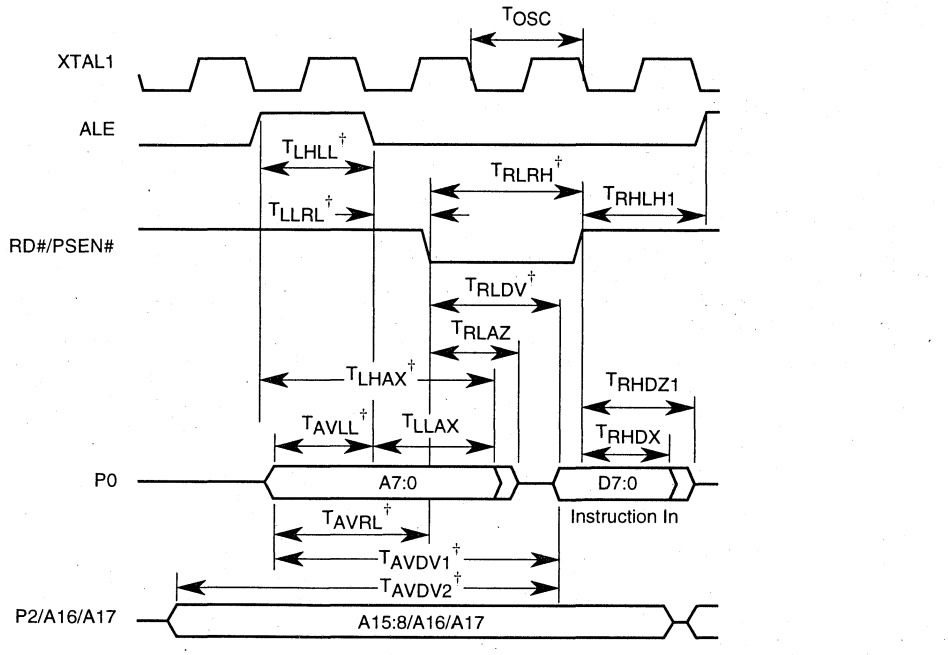


Figure 7. External Bus Cycle: Code Fetch (Nonpage Mode)

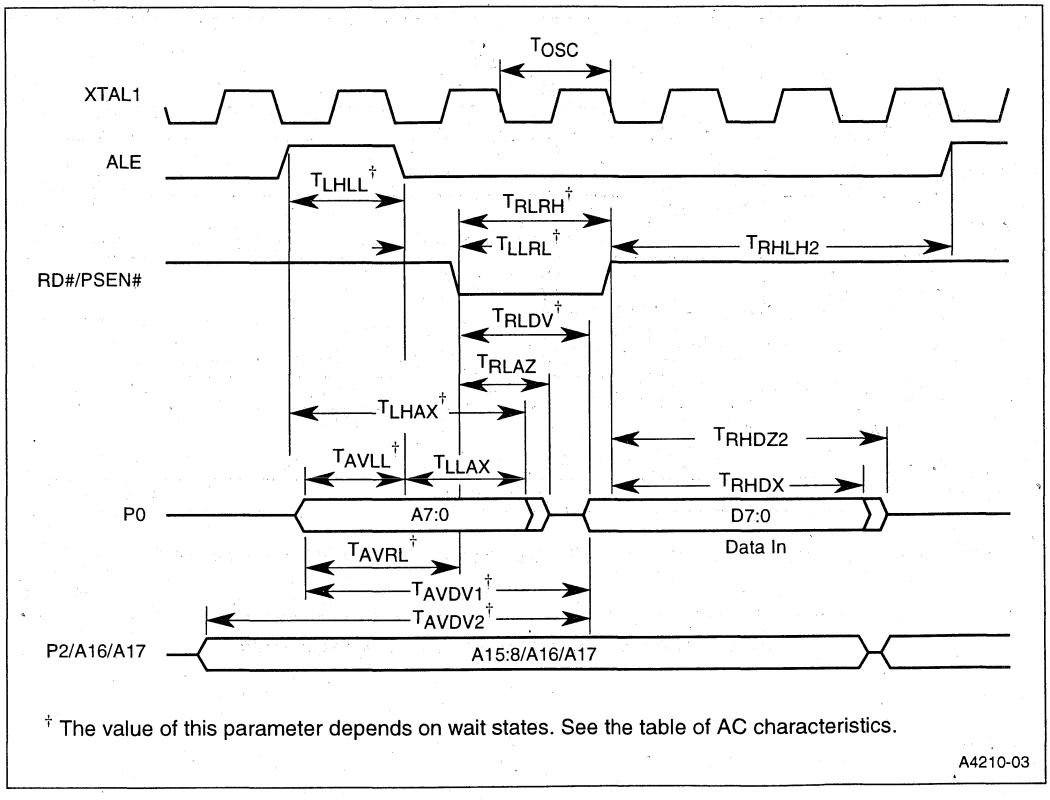


Figure 8. External Bus Cycle: Data Read (Nonpage Mode)

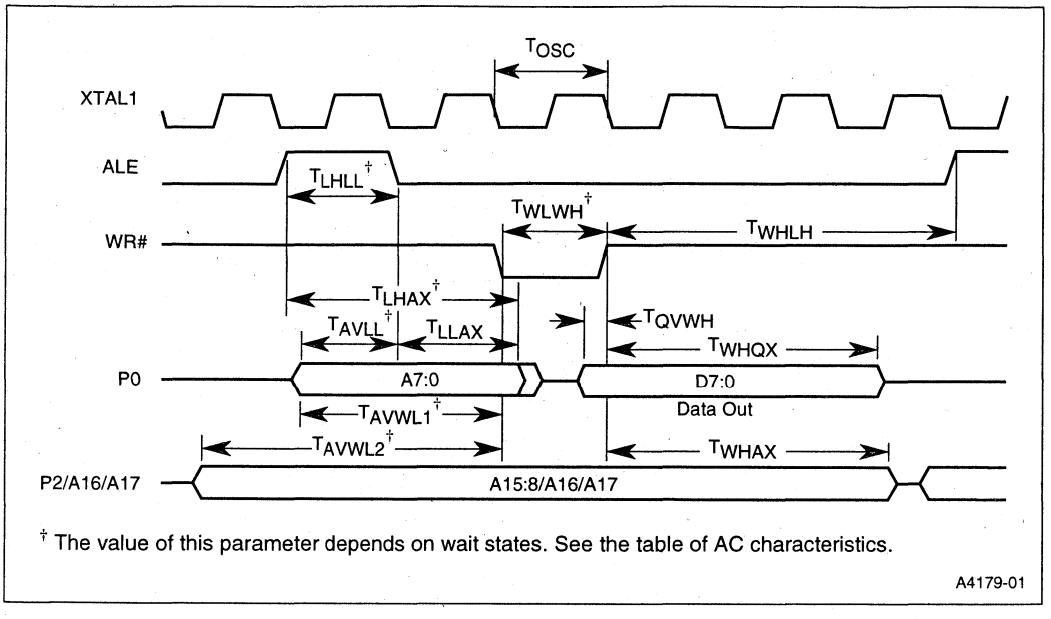
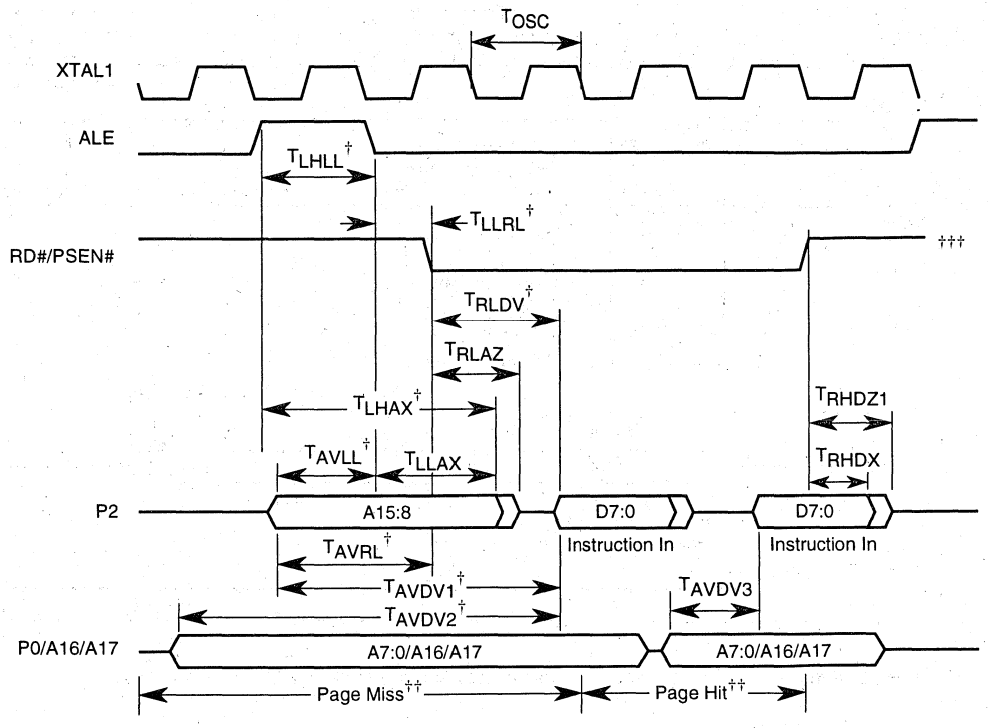


Figure 9. External Bus Cycle: Data Write (Nonpage Mode)

5.3.2 EXTERNAL BUS CYCLES, PAGE MODE



† The value of this parameter depends on wait states. See the table of AC characteristics.

†† A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).

††† During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

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Figure 10. External Bus Cycle: Code Fetch (Page Mode)

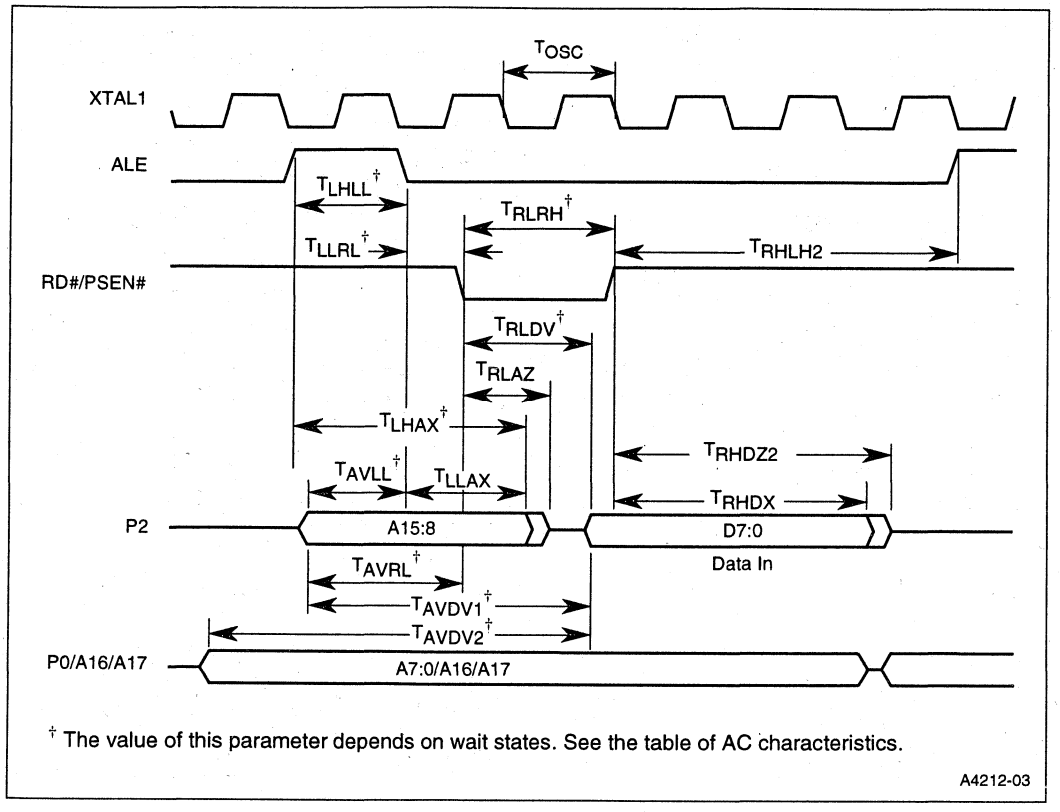


Figure 11. External Bus Cycle: Data Read (Page Mode)

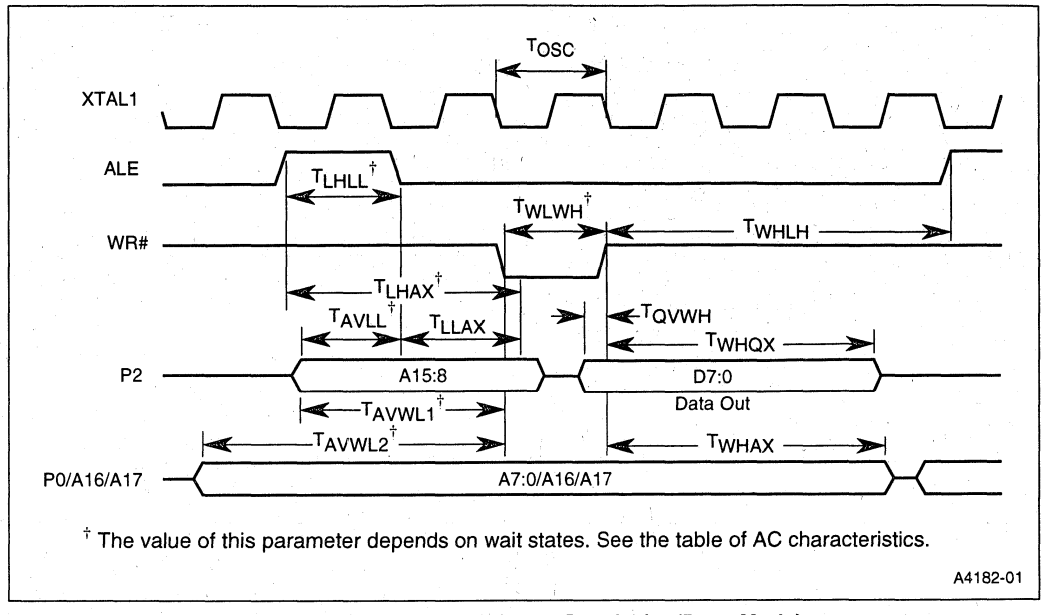


Figure 12. External Bus Cycle: Data Write (Page Mode)

5.3.3 DEFINITION OF REAL-TIME WAIT SYMBOLS

Table 12. Real-time Wait Timing Symbol Definitions

Signals	
A	Address
D	Data
C	WCLK
Y	WAIT#
W	WR#
R	RD#/PSEN#

Conditions	
L	Low
X	Hold
V	Setup

5.3.4 EXTERNAL BUS CYCLES, REAL-TIME WAIT STATES

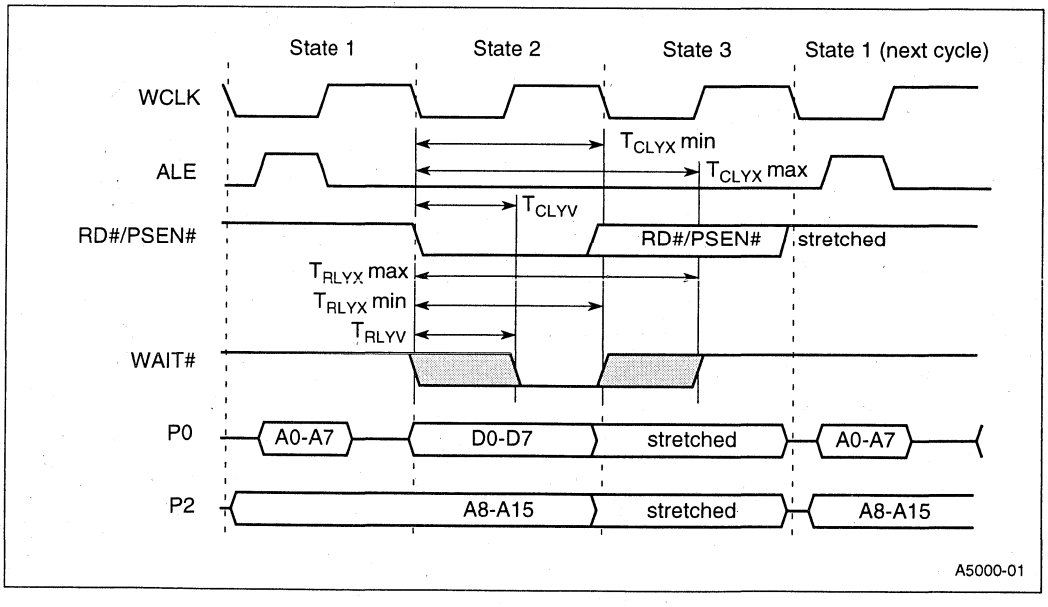


Figure 13. External Bus Cycle: Code Fetch/Data Read (Nonpage Mode)

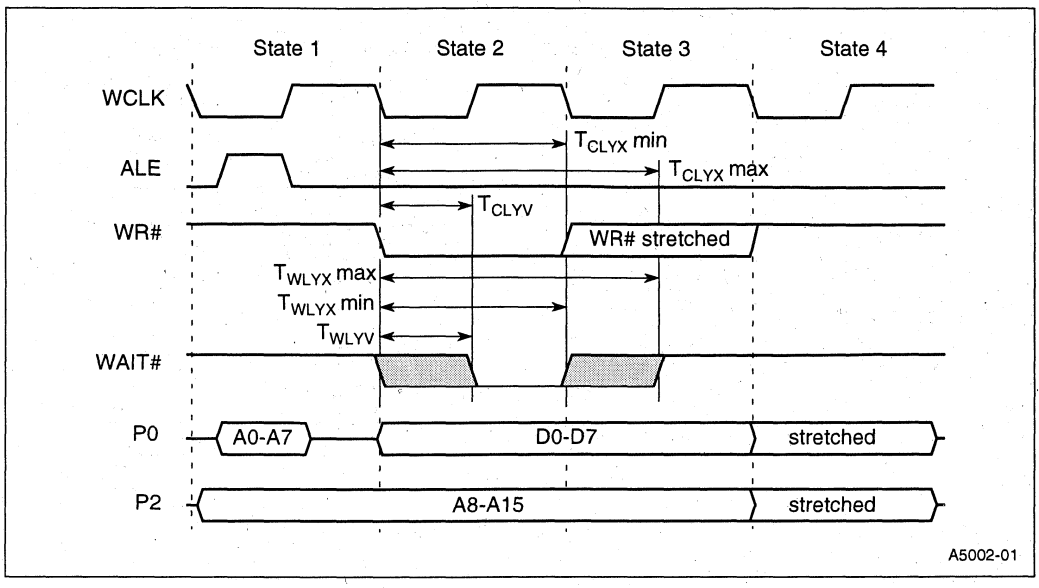


Figure 14. External Bus Cycle: Data Write (Nonpage Mode)

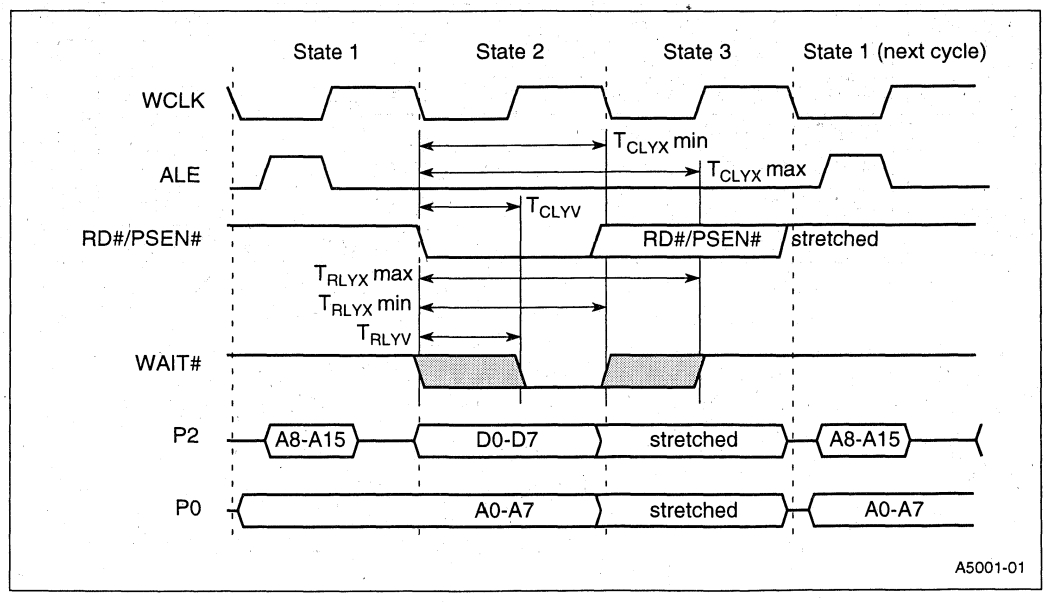


Figure 15. External Bus Cycle: Code Fetch/Data Read (Page Mode)

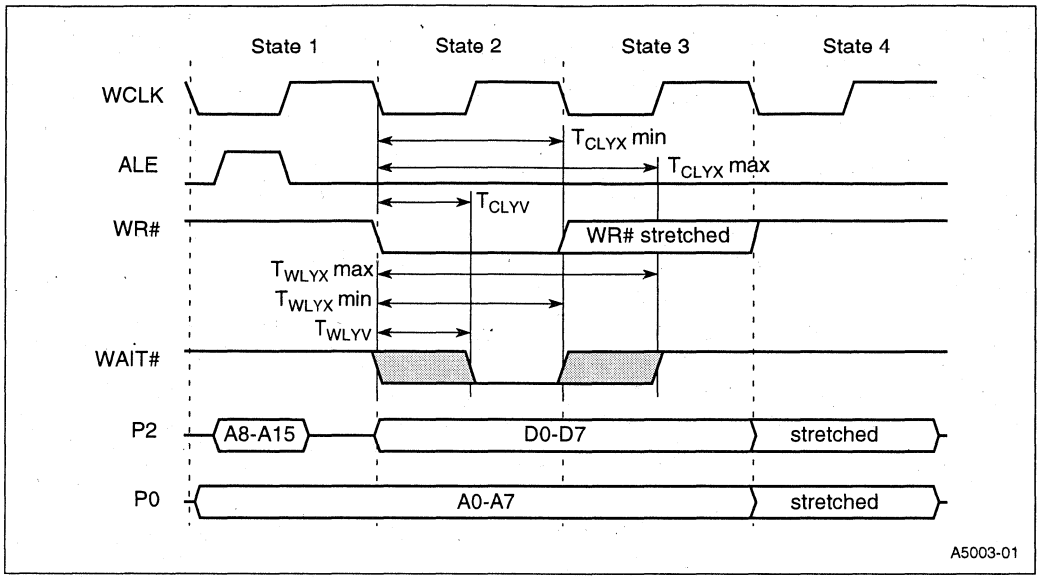


Figure 16. External Bus Cycle: Data Write (Page Mode)

Table 13. Real-time Wait AC Timing

Symbol	Parameter	Min	Max	Units
T_{CLYV}	Wait Clock Low to Wait Set-up	0	$T_{OSC} - 20$	ns
T_{CLYX}	Wait Hold after Wait Clock Low	$(2W)T_{OSC} + 5$	$(1+2W)T_{OSC} - 20$	ns
T_{RLYV}	PSEN#/RD# Low to Wait Set-up	0	$T_{OSC} - 20$	ns
T_{RLYX}	Wait Hold after PSEN#/RD# Low	$(2W)T_{OSC} + 5$	$(1+2W)T_{OSC} - 20$	ns
T_{WLYV}	WR# Low to Wait Set-up	0	$T_{OSC} - 20$	ns
T_{WLYX}	Wait Hold after WR# Low	$(2W)T_{OSC} + 5$	$(1+2W)T_{OSC} - 20$	ns

5.4 AC Characteristics — Serial Port, Shift Register Mode

Table 14. Serial Port Timing — Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns

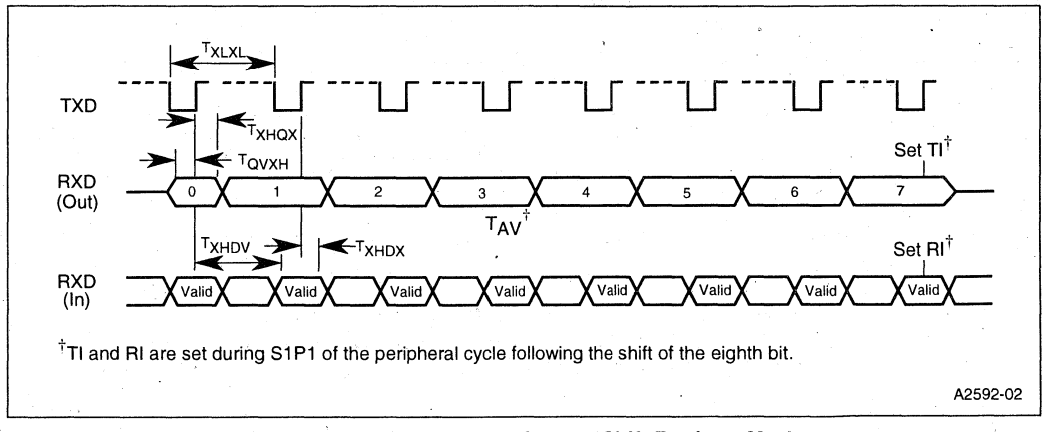


Figure 17. Serial Port Waveform — Shift Register Mode

5.5 External Clock Drive

Table 15. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency (F_{OSC})		16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

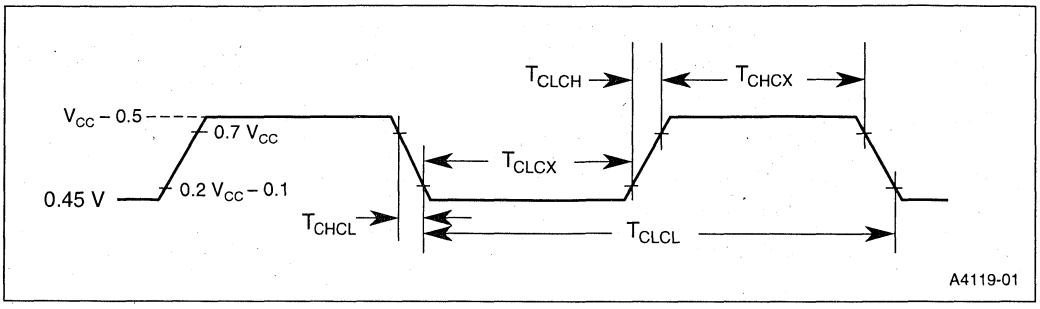


Figure 18. External Clock Drive Waveforms

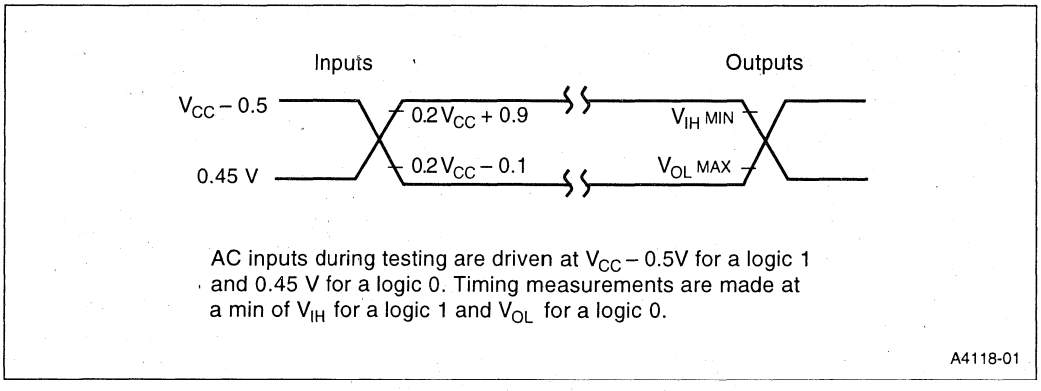


Figure 19. AC Testing Input, Output Waveforms

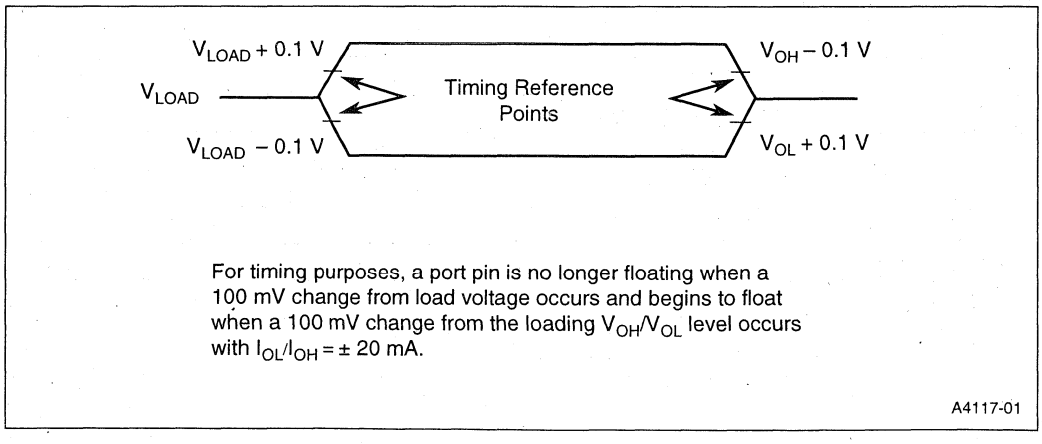


Figure 20. Float Waveforms

6.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 16. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
44-pin PLCC	46°C/W	16°C/W
40-pin PDIP	45°C/W	16°C/W
40-pin Ceramic DIP	30.5°C/W	10°C/W

7.0 NONVOLATILE MEMORY PROGRAMMING AND VERIFICATION CHARACTERISTICS

7.1 Definition of Nonvolatile Memory Symbols

Table 17. Nonvolatile Memory Timing Symbol Definitions

Signals	
A	Address
D	Data In
Q	Data Out
S	Supply
G	PROG#
E	Enable

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

7.2 Programming and Verification Timing for Nonvolatile Memory

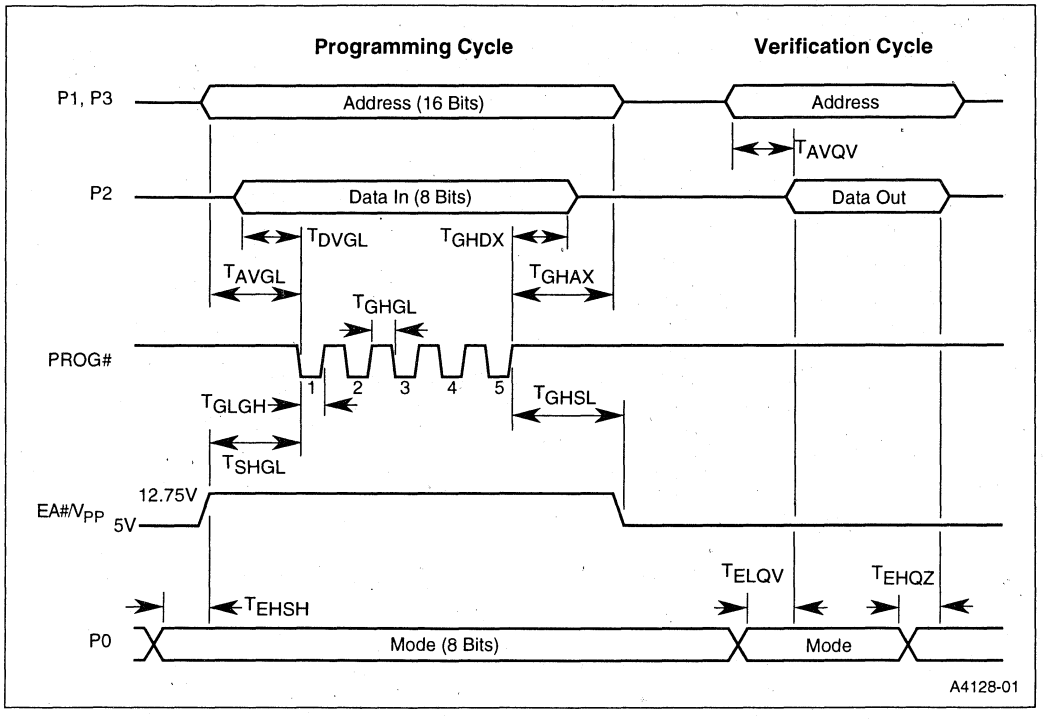


Figure 21. Timing for Programming and Verification of Nonvolatile Memory

Table 18. Nonvolatile Memory Programming and Verification Characteristics at T_A = 21 – 27 °C, V_{CC} = 5 V, and V_{SS} = 0 V

Symbol	Definition	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.5	D.C. Volts
I_{PP}	Programming Supply Current		75	mA
F_{OSC}	Oscillator Frequency	4.0	6.0	MHz
T_{AVGL}	Address Setup to PROG# Low	$48T_{OSC}$		
T_{GHAX}	Address Hold after PROG#	$48T_{OSC}$		
T_{DVGL}	Data Setup to PROG# Low	$48T_{OSC}$		
T_{GHDX}	Data Hold after PROG#	$48T_{OSC}$		
T_{EHSH}	ENABLE High to V_{PP}	$48T_{OSC}$		
T_{SHGL}	V_{PP} Setup to PROG# Low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{GLGH}	PROG# Width	90	110	µs

Table 18. Nonvolatile Memory Programming and Verification Characteristics at T_A = 21 – 27 °C, V_{CC} = 5 V, and V_{SS} = 0 V(Continued)

T_{AVQV}	Address to Data Valid		$48T_{OSC}$	
T_{ELQV}	ENABLE Low to Data Valid		$48T_{OSC}$	
T_{EHQZ}	Data Float after ENABLE	0	$48T_{OSC}$	
T_{GHGL}	PROG# High to PROG# Low	10		µs

8.0 ERRATA

There are no known errata for this product.

9.0 REVISION HISTORY

This (-003) revision of the 8XC251SA/SB/SP/SQ datasheet contains information on products with "[M] [C] '94 '95 C" as the last line of the topside marking. This datasheet replaces earlier product information. The following changes appear in the -003 datasheet:

1. Real-time wait state operation is described in the datasheet.
2. Memory map reserved locations are newly defined and the Memory Map is now referred to as the "Address Map."
3. AC Characteristics have been updated. The following AC parameters have changed: T_{LLAX}, T_{RLRH}, T_{WLWH}, T_{LLRL}, T_{RLDV}, T_{RHDZ1}, T_{RHDZ2}, T_{RHLH2}, T_{WHLH}, T_{AVDV1}, T_{AVDV2}, T_{AVRL}, T_{AVWL1}, T_{AVWL2}, T_{QVWH}, and T_{WHAX}.
4. DC Characteristics have been updated. The following DC specs have changed: I_{PD} max, I_{DL} typical, I_{DL} max, I_{CC} typical, and I_{CC} max.
5. An I_{CC} vs. Frequency graph is included.
6. Process information is no longer contained in the datasheet.
7. The section "Programming and Verifying Nonvolatile Memory" has been deleted. See the 8XC251SA/SB/SP/SQ Embedded Microcontroller User's Manual. Timing and Characteristics for Programming and Verifying Nonvolatile memory have been retained in this datasheet.
8. Signature Byte information has been deleted. See the 8XC251SA/SB/SP/SQ Embedded Microcontroller User's Manual.
9. Sections in the datasheet are numbered.
10. New sections have been created to provide better organization. These include "Nomenclature," "Pinout," "Signals," "Address Map," "Electrical Characteristics," "Thermal Characteristics," "Nonvolatile Memory Programming and Verification Characteristics", "Errata," and "Revision History"
11. Proliferation Options and Package Options are in the Nomenclature section.
12. Temperature range is contained in the Electrical Characteristics section under "Operating Conditions"
13. Bus timing diagrams have been organized into subsections.

The (-002) revision of the 8XC251SA/SB/SP/SQ datasheet contains information on products with "[M] [C] '94 '95 B" as the last line of the topside marking. This datasheet replaces earlier product information. The following changes appear in the -002 datasheet:

1. A corrected PDIP diagram appears on page 7.
2. A corrected formula to calculate T_{LHLL} is described on page 17.
3. The RD#/PSEN# waveform is changed in Figure 11 on page 25.

intel®

4

MCS®51 and MCS®96 Microcontroller Packaging Family

intel®

MCS®-96 Architectural Overview

November 1994

Order Number: 272109-002

1.0 INTRODUCTION

The MCS-96 family members are all high performance microcontrollers with a 16-bit CPU and at least 230 bytes of on-chip RAM. The Intel MCS-96 family easily handles high speed calculations and fast input/output (I/O) operations. Typical applications include closed-loop control and mid-range digital signal processing. Modems, motor control system, printers, engine control system, photocopiers, anti-lock brakes, air conditioner control systems, disk drives and medical instrumentation all use MCS-96 products.

All of the MCS-96 components share a common instruction set and architecture. However, the CHMOS components have enhancements to provide higher performance with lower power consumption. To further decrease power usage, idle and power-down modes are available on these devices. These microcontrollers contain dedicated I/O subsystems and perform 16-bit arithmetic instructions including multiply and divide operations.

This overview briefly describes the MCS-96 instruction set and architecture and provides descriptions for the 8X9X, 80C196KB, 80C196KC and 80C196KR key features. Comprehensive user's guides that contain more information about these devices are available. Figure 1.1 shows a block diagram of the MCS-96 architecture.

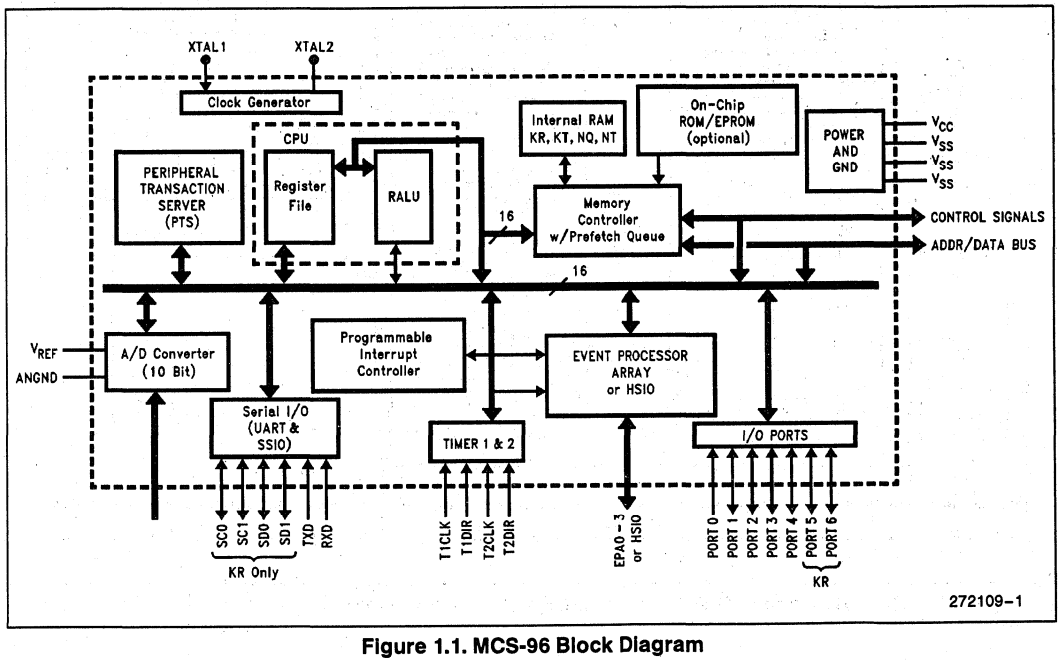


Figure 1.1. MCS-96 Block Diagram

2.0 THE CPU

The major components of the MCS-96 CPU are the Register File and the Register/Arithmetic Logic Unit (RALU). Locations 00H through 17H are the I/O control registers or Special Function Registers (SFRs). Locations 18H and 19H contain the stack pointer, which can serve as general purpose RAM when not performing stack operations. The remaining bytes of the register file serve as general purpose RAM, accessible as bytes, words or double-words.

Calculations performed by the CPU take place in the RALU. The RALU shown in Figure 2.1 contains a 17-bit ALU, the Program Status Word (PSW), a loop counter and three temporary registers. The RALU operates directly on the Register File, thus eliminating accumulator bottleneck and providing for direct control of I/O operations through the SFRs.

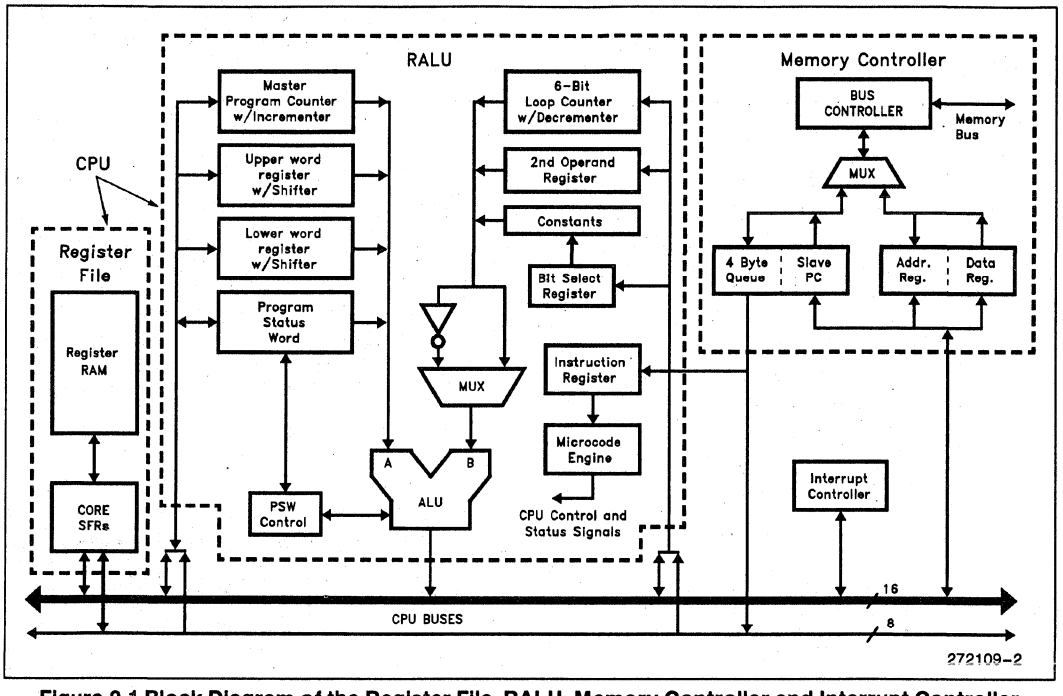


Figure 2.1 Block Diagram of the Register File, RALU, Memory Controller and Interrupt Controller

3.0 THE ARCHITECTURE

The MCS-96 supports a complete instruction set which includes bit operations, byte operations, word operations, double-word operations (unsigned 32-bit), long operations (signed 32-bit), flag manipulations as well as jump and call instructions. All the standard logical and arithmetic instructions function as both byte and word operations. The Jump Bit Set and Jump Bit Clear instructions can operate on any of the SFRs or bytes in the lower register file. These fast bit manipulations allow for rapid I/O functions.

Byte and word operations make-up most of the instruction set. The assembly language ASM-96 uses a "B" suffix on a mnemonic for a byte operation, otherwise the mnemonic refers to a word operation. One, two or three operand forms exist for many of the instructions.

Long and double-word operations include shifts, normlize, multiply and divide. The divide instruction functions as a 32-bit by 16-bit divide that generates a 16-bit quotient and 16-bit remainder. The word multiply operates as a 16-bit by 16-bit multiply with a 32-bit result. Both operations can function in either the signed or unsigned mode. The normalize instruction and sticky bit flag provide hardware support for the software floating point package (FPAL-96).

3.1 Addressing Modes

The MCS-96 instruction set supports the following addressing modes: register-direct, indirect, indirect with auto-increment, immediate, short-indexed and long-indexed. These modes increase the flexibility and overall execution speed of the MCS-96 devices. Each instruction uses at least one of the addressing modes. These modes and formats are shown in Figure 3.1.

```
Mnem      Dest or Srcl                ;One operand direct
Mnem      Dest, Srcl                  ;Two operand direct
Mnem      Dest, Srcl, Src2            ;Three operand direct

Mnem      #Srcl                       ;One operand immediate
Mnem      Dest, #Srcl                 ;Two operand immediate
Mnem      Dest, Srcl, #Src2           ;Three operand immediate

Mnem      [addr]                      ;One operand indirect
Mnem      [addr]+                     ;One operand indirect auto-increment
Mnem      Dest, [addr]                ;Two operand indirect
Mnem      Dest, [addr]+               ;Two operand indirect auto-increment
Mnem      Dest, Srcl, [addr]          ;Three operand indirect
Mnem      Dest, Srcl, [addr]+         ;Three operand indirect auto-increment

Mnem      Dest, offs[addr]            ;Two operand indexed (short or long)
Mnem      Dest, Srcl, offs[addr]      ;Three operand indexed (short or long)
```

```
Where:
Mnem = instruction mnemonic
Dest = destination register
Srcl, Src2 = source registers
addr = word register used in computing the address of an operand
offs = offset used in computing the address of an operand
```

Figure 3.1 Instruction Format

The register-direct and immediate addressing modes execute faster than the other addressing modes. The register-direct addressing mode provides access to the addresses in the register file and the SFRs. The indexed modes provide for direct access to the remainder of the 64K address space. Immediate addressing uses the data following the opcode as the operand.

Both of the indirect addressing modes use the value in a word register as the address of the operand. The indirect auto-increment mode increments a word address by one after a byte operation and two after a word operation. This addressing mode provides easy access into look-up tables.

The long-indexed addressing mode provides direct access to any of the locations in the 64K address space. This mode forms the address of the operand by adding a 16-bit 2's complement value to the contents of a word register. Indexing with the zero register allows "direct" addressing to any location. The short-indexed addressing mode forms the address of the operand by adding an 8-bit 2's complement value to the contents of a word register.

The 8XC196NT has 9 new instructions which have been implemented to support addressing the extended 1 Mbyte address space of the 8XC196NT family. Four extended load and store instructions using indirect, indirect auto increment, or extended indexed addressing, can be used to address the 1 Mbyte address space. Three instructions are for extended calls, branches, and jumps. An extended version of the interruptible and non-interruptible block moves have also been implemented.

The multiple addressing modes of the MCS-96 make it easy to program in assembly language and provide an excellent interface to high-level languages. The instructions accepted by the assembler consist of mnemonics followed by either addresses or data. Refer to the Quick Reference section for Instruction Summary tables for each device. The MCS-96 Macro Assembler Users Guide contains additional ASM96 information.

4.0 8X9X PERIPHERALS

Standard I/O Ports—The 8X9X has five 8-bit I/O ports. Port 0 is an input port that is also the anlog input for the A/D converter. Port 1 is a quasi-bidirectional port. Port 2 contains three types of port lines: quasi-bidirectional, input and output. Other functions on the 8X9X share the input and output lines with Port 2. Ports 3 and 4 are open-drain bidirectional ports that share their pins with the address/data bus.

Timers—The 8X9X has two 16-bit timers, Timer1 and Timer2. An internal clock increments the Timer1 value every 8 state times. (A state time is 3 oscillator periods.) An external clock increments Timer2 on every positive and negative transition. Either an internal or external source can reset Timer2. Timer1 and Timer2 can generate an interrupt when crossing the 0FFFFH/0000H boundary. The 8X9X also includes separate, dedicated timers for the Serial Port baud rate generator and Watchdog Timer. The Watchdog Timer is an internal timer that resets the system if the software fails to operate properly.

Table 1. MCS-96 Family Devices

Product	Timers	HSIO /EPA	A/D CHS	Serial Port	Synch. Serial Port	PWMS	PTS	Slave Port	3-Phase Waveform Generator
8098	2	HSIO	4	YES		1			
8097BH	2	HSIO	8	YES		1			
8097JF	2	HSIO	8	YES		1			
80C198	2	HSIO	4	YES		1			
80C196KB	2	HSIO	8	YES		1			
80C196KC	2	HSIO	8	YES		3	YES		
80C196KD	2	HSIO	8	YES		3	YES		
80C196KR	2	EPA	8	YES	YES		YES	YES	
80C196KT	2	EPA	8	YES	YES		YES	YES	
80C196NT	2	EPA	4	YES	YES		YES	YES	
80C196MC	2	EPA	13	YES			YES		YES

High Speed Input Unit (HSI)—The 8X9X HSI unit can record times of external events with a 9 state time resolution. It can monitor four independently configurable HSI lines and capture the value of Timer1 when an event(s) takes place. The four types of events that can trigger captures include: rising edges only, falling edges only, rising or falling edges, or every eighth rising edge. The HSI unit can store up to 8 entries (Timer1 values). Reading the HSI holding register unloads the earliest entry placed in the FIFO. The HSI unit can generate an interrupt when loading an entry into the HSI holding register or loading the sixth entry into the FIFO.

High Speed Output Unit (HSO)—The 8X9X HSO unit can trigger events at specified times based on Timer1 or Timer2. These programmable events include: starting an A/D conversion, resetting Timer2, generating up to four software time delays, and setting or clearing one or more of the 6 HSO output lines. The HSO unit stores pending events and the specified times in a Content Addressable Memory (CAM) file. This file stores up to eight commands. Each command specifies the action time, the nature of the action, whether an interrupt is to occur, and whether Timer1 or Timer2 is the reference timer. Every 8 state times the HSO compares the CAM locations for time matches. The HSO unit triggers the specified event when it finds a time match. A command is cleared from the CAM as soon as it executes.

The Serial Port—The Serial Port on the 8X9X has one synchronous (Mode 0) and three asynchronous modes (Modes 1, 2 and 3). The asynchronous modes are full duplex, meaning they can transmit and receive data simultaneously. The receiver on the 8X9X is buffered so the reception of a second byte may begin before the first byte is read. The most common use of Mode 0, the synchronous mode, is to expand the I/O capability of the 8X9X using shift registers. Mode 1 is the standard asynchronous mode used for normal serial communication. The data frame for Mode 1 consists of 10 bits: a start bit, 8 data bits (LSB first) and a stop bit. If parity is enabled (PEN = 1), an even parity bit is sent instead of the 8th data bit. Modes 2 and 3 are 9-bit modes commonly used for multiprocessor communications. The data frame used in these modes consists of 11 bits: a start bit, nine data bits (LSB first) and a stop bit. Devices in Mode 2 will interrupt upon reception only if the 9th data bit is set. Devices in Mode 3 will always interrupt upon reception. Mode 3 also allows transmission of 8 data bits plus an even parity bit.

Pulse Width Modulator (PWM)—The PWM output waveform is a variable duty cycle pulse that repeats every 256 state times. The Pulse Width Modulator of the 8X9X can provide useful signals for a variety of applications. The PWM output can perform digital to analog conversions and drive several types of motors that require a PWM waveform for more efficient operation.

A/D Converter—The 8X9X A/D Converter converts an analog input to a 10-bit digital equivalent. The main components of the A/D Converter are: 8 analog inputs, an 8 to 1 multiplexer, a sample and hold capacitor and the resistor ladder. The A/D Quick Reference section defines the A/D terms. The A/D Converter can start a conversion immediately or the High Speed Output unit can trigger a conversion at a preprogrammed time. The A/D Converter performs a conversion in 88 state times. Upon completion of each conversion the converter can generate a conversion complete interrupt. The 8X9X provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 21 interrupt sources and 8 interrupt vectors on the 8X9X. When the interrupt controller detects one of the 8 interrupts it sets the corresponding bit in the interrupt pending register. Individual interrupts are enabled or disabled by setting or clearing bits in the interrupt mask register. When the interrupt controller decides to process an interrupt, it executes a "call" to an Interrupt Service Routine (ISR). The corresponding interrupt vector contains the address of the ISR. The interrupt controller then clears the associated pending bit.

5.0 8XC196KB PERIPHERALS

Standard I/O Ports—The 8XC196KB has five 8-bit I/O ports. Port 0 is an input port that is also the analog input for the A/D converter. Port 1 is a quasi-bidirectional port. Port 2 contains three types of port lines: quasi-bidirectional, input and output. Other functions on the 8XC196KB share the input and output lines with Port 2. Ports 3 and 4 are open-drain bidirectional ports that share their pins with the address/data bus.

Timers—The 8XC196KB has two 16-bit timers, Timer1 and Timer2. An internal clock increments the Timer1 value every 8 state times. (A state time is 2 oscillator periods.) An external clock increments or decrements Timer2 on every positive and negative transition. Either an internal or external source can reset Timer2. Timer1 can generate an interrupt when crossing the 0FFFFH/0000H boundary. Timer2 can generate an interrupt when crossing the 0FFFFH/0000H boundary or the 7FFFH/8000H boundary. The 8XC196KB also includes separate, dedicated timers for the baud rate generator and Watchdog Timer. The Watchdog Timer is an internal timer that resets the system if the software fails to operate properly.

High Speed Input Unit (HSI)—The 8XC196KB HSI unit can record times of external events with a 9 state time resolution. It can monitor four independently configurable HSI lines and capture the value of Timer1 when an event(s) takes place. The four types of events that can trigger captures include: rising edges only, falling edges only, rising or falling edges, or every eighth rising edge. The HSI unit can store up to 8 entries (Timer1 values), 7 in the 7-level FIFO and 1 in the HSI holding register. Reading the HSI holding register unloads the earliest entry placed in the FIFO. The HSI unit can generate an interrupt when: loading an entry into the HSI holding register, loading the fourth entry into the FIFO or loading the sixth entry into the FIFO.

High Speed Output Unit (HSO)—The 8XC196KB HSO unit can trigger events at specified times based on Timer1 or Timer2. These programmable events include: starting an A/D conversion, resetting Timer2, generating up to four software time delays, and setting or clearing one or more of the 6 HSO output lines. The HSO unit stores pending events and the specified times in a Content Addressable Memory (CAM) file. This file stores up to eight commands. Each command specifies the action time, the nature of the action, whether an interrupt is to occur, and whether Timer1 or Timer2 is the reference timer. Every 8 state times the HSO compares the CAM locations for time matches. The HSO unit triggers the specified event when it finds a time match. A command can either clear from the CAM as soon as it executes or remain in the CAM as a locked CAM entry and continue to execute whenever its time tag matches the reference timer. Locked entries are useful in applications requiring periodic or repetitive events to occur such as multiple PWMs.

The Serial Port—The Serial Port on the 8XC196KB has one synchronous (Mode 0) and three asynchronous modes (Modes 1, 2 and 3). The asynchronous modes are full duplex, meaning they can transmit and receive data simultaneously. The receiver on the 8XC196KB is buffered so the reception of a second byte may begin before the first byte is read. The transmitter is also double buffered and can generate continual transmissions. The most common use of Mode 0, the synchronous mode, is to expand the I/O capability of the 8XC196KB using shift registers. Mode 1 is the standard asynchronous mode used for normal serial communication. The data frame for Mode 1 consists of 10 bits: a start bit, 8 data bits (LSB first) and a stop bit. If parity is enabled (PEN = 1), an even parity bit is sent instead of the 8th data bit. Modes 2 and 3 are 9-bit modes commonly used for multiprocessor communications. The data frame used in these modes consists of 11 bits: a start bit, nine data bits (LSB first) and a stop bit. Devices in Mode 2 will interrupt upon reception only if the 9th data bit is set. Devices in Mode 3 will always interrupt upon reception. Mode 3 also allows transmission of 8 data bits plus an even parity bit.

Pulse Width Modulator (PWM)—The Pulse Width Modulator of the 8XC196KB can provide useful signals for a variety of applications. The PWM output can perform digital to analog conversions and drive several types of motors that require a PWM waveform for more efficient operaton. The PWM output waveform is a variable duty cycle pulse that repeats every 256 state times or 512 state times.

A/D Converter—The 8XC196KB A/D Converter converts an analog input to a 10-bit digital equivalent. The main components of the A/D Converter are: 8 analog inputs, an 8 to 1 multiplexer, a sample and hold capacitor and the resistor ladder. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. The A/D Converter can start a conversion immediately or the High Speed Output unit can trigger a conversion at a preprogrammed time. The A/D Converter can perform a conversion in either 91 state times for low crystal frequencies and 158 state times for higher crystal frequencies. Upon completion of each conversion the converter generates a conversion complete interrupt. The 8XC196KB provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 28 interrupt sources and 16 interrupt vectors on the 8XC196KB. Additionally, there are 2 special interrupt vectors for Software Trap and Unimplemented Opcodes. When the interrupt controller detects one of the 16 interrupts it sets the corresponding bit in one of two interrupt pending registers. Individual interrupts are enabled or disabled by setting or clearing bits in the interrupt mask registers. When the interrupt controller decides to process an interrupt, it executes a "call" to an Interrupt Service Routine (ISR). The corresponding interrupt vector contains the address of the ISR. The interrupt controller then clears the associated pending bit.

6.0 8XC196KC and 8XC196KD PERIPHERALS

Standard I/O Ports—The 8XC196KC/KD has five 8-bit I/O ports. Port 0 is an input port that is also the analog input for the A/D converter. Port 1 is a quasi-bidirectional port that shares pins with two PWM outputs. Port 2 contains three types of port lines: quasi-bidirectional, input and output. Other functions on the 8XC196KC/KD share the input and output lines with Port 2. Ports 3 and 4 are open-drain bidirectional ports that share their pins with the address/data bus.

Timers—The 8XC196KC/KD has two 16-bit timers, Timer1 and Timer2. An internal clock increments the Timer1 value every 8 state times. (A state time is 2 oscillator periods.) An internal clock or an external clock can drive Timer2. When clocked internally Timer2 can increment every 1 or 8 state times. When clocked externally Timer2 increments or decrements on every positive and negative transition. Either an internal or external source can reset Timer2. Timer1 can generate an interrupt when crossing the 0FFFFH/0000H boundary. Timer2 can generate an interrupt when crossing the 0FFFFH/0000H boundary or the 7FFFH/8000H boundary. The 8XC196KC/KD also includes separate, dedicated timers for the baud rate generator and Watchdog Timer. The Watchdog Timer is an internal timer that resets the system if the software fails to operate properly.

High Speed Input Unit (HSI)—The 8XC196KC/KD HSI unit can record times of external events with a 9 state time resolution. It can monitor four independently configurable HSI lines and capture the value of Timer1 when an event(s) takes place. The four types of events that can trigger captures include: rising edges only, falling edges only, rising or falling edges, or every eighth rising edge. The HSI unit can store up to 8 entries (Timer1 values), 7 in the 7-level FIFO and 1 in the HSI holding register. Reading the HSI holding register unloads the earliest entry placed in the FIFO. The HSI unit can generate an interrupt when: loading an entry into the HSI holding register, loading the fourth entry into the FIFO or loading the sixth entry into the FIFO.

High Speed Output Unit (HSO)—The 8XC196KC/KD HSO unit can trigger events at specified times based on Timer1 or Timer2. These programmable events include: starting an A/D conversion, resetting Timer2, generating up to four software timers, and setting or clearing one or more of the 6 HSO output lines. The HSO unit stores pending events and the specified times in a Content Addressable Memory (CAM) file. This file stores up to eight commands. Each command specifies the action time, the nature of the action, whether an interrupt is to occur, and whether Timer1 or Timer2 is the reference timer. Every 8 state times the HSO compares the CAM locations for time matches. The HSO unit triggers the specified event when it finds a time match. A command can either clear from the CAM as soon as it executes or remain in the CAM as a locked CAM entry and continue to execute whenever its time tag matches the reference timer. Locked entries are useful in applications requiring periodic or repetitive events to occur such as multiple PWMs.

The Serial Port—The Serial Port on the 8XC196KC/KD has one synchronous (Mode 0) and three asynchronous modes (Modes 1, 2 and 3). The asynchronous modes are full duplex, meaning they can transmit and receive data simultaneously. The receiver on the 8XC196KC/KD is buffered so the reception of a second byte may begin before the first byte is read. The transmitter is also double bufered and can generate continual transmissions. The most common use of Mode 0, the synchronous mode, is to expand the I/O capability of the 8XC196KC/KD using shift registers. Mode 1 is the standard asynchronous mode used for normal serial communication. The data frame for Mode 1 consists of 10 bits: a start bit, 8 data bits (LSB first) and a stop bit. If parity is enabled (PEN = 1), an even parity bit is sent instead of the 8th data bit. Modes 2 and 3 are 9-bit modes commonly used for multiprocessor communications. The data frame used in these modes consists of 11 bits: a start bit, nine data bits (LSB first) and a stop bit. Devices in Mode 2 will interrupt upon reception only if the 9th data bit is set. Devices in Mode 3 will always interrupt upon reception. Mode 3 also allows transmission of 8 data bits plus an even parity bit.

Pulse Width Modulator (PWM)—The 8CX196KC/KD has 3 PWM outputs. The output waveform is a variable duty cycle pulse which is selectable to repeat every 256 state times or 512 state times. Several types of motors require a PWM waveform for most efficient operation. Additionally, filtering this waveform will produce a DC level that can change in 256 steps by varying the duty cycle.

A/D Converter—The 8XC196KC/KD A/D Converter converts an analog input to a digital equivalent. Resolution is either 8 or 10 bits with programmable sample and convert times. The main components of the A/D Converter are: a sample and hold, an 8-channel multiplexer, and an 8-bit or 10-bit successive approximation analog-to-digital converter. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. The converter can start a conversion immediately or the High Speed Output unit can trigger a conversion at a preprogrammed time. Upon completion of each conversion the converter generates a conversion complete interrupt. The 8XC196KC/KD provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 28 interrupt sources and 16 interrupt vectors on the 8XC196KC/KD. In addition there are 2 special interrupt vectors (Software Trap and Unimplemented Opcode) used in Intel development tools or evaluation boards. When the interrupt controller detects one of the 16 interrupts it sets the corresponding bit in one of two interrupt pending registers. Individual interrupts are enabled or disabled by setting or clearing bits in the interrupt mask registers. When the interrupt controller decides to process an interrupt, it executes a "call" to an Interrupt Service Routine (ISR). The corresponding interrupt vector contains the address of the ISR. The interrupt controller then clears the associated pending bit.

Peripheral Transaction Server (PTS)—The PTS is a microcoded hardware interrupt processor. It responds to interrupts with a fixed set of actions. These actions consist of: transferring data, starting an A/D conversion, reading the HSI FIFO and loading HSO events. The PTS completes these tasks much faster than using interrupt driven service routines. The PTS can service all interrupts except NMI, Trap and Unimplemented Opcode. Each interrupt managed by the PTS requires a block of data called the PTS Control Block (PTSCB). Each PTSCB requires 8 data bytes in register RAM. The PTSCB determines: the type of PTS, the number of PTS responses (if applicable), the source for data and the destination (if applicable). PTS cycles have a higher priority than interrupts and may temporarily suspend interrupt service routines.

7.0 8XC196KR and 8XC196KT PERIPHERALS

Standard I/O Ports—The 8XC196KR/KT has six 8-bit I/O ports. Each pin operates as a dedicated input or output. Most pins also have an alternate function. The KR/KT does not use the quasi-bidirectional port pins found on previous MCS-96 devices. As an input, the pin is a true high impedance with no pull-ups or pull-downs. Most ports (Ports 1, 2, 5 and 6) have direction registers (Px__DIR), mode registers (Px__MODE), data input registers (Px__PIN) and data output registers (Px__REG). This allows the user to configure each port pin as input, output, open-drain output or alternate function. Ports 3 and 4 have Px__PIN and Px__REG registers and lack internal pull-ups. As standard outputs, these pins can only function in open-drain mode and need external pull-ups. Ports 3 and 4 also are the multiplexed address/data bus. When emitting the address, an internal pull-up device is active and does not need external pull-ups. Port 0 is the analog input port, and only has a Px__PIN register because there are no output drivers. As a digital port, Port 0 pins can only function as inputs.

Event Processor Array (EPA)—The EPA performs input event capture and output event generation functions using Timer1 and Timer2. It consists of 10 capture/compare modules, 2 compare only modules and the 2 timers. In capture mode, when an external event occurs the EPA stores the value of the timer, generates an interrupt or both. A rising, falling, or any edge can trigger a capture. All captures are double buffered. In compare mode, when the timer matches the value in the compare register the EPA changes the state of an output pin, generates an interrupt, or both. The EPA sets, resets or toggles the pin when the compare occurs. The timers can count up or count down. The clock source to the timers can be internal or external. The clock also goes through a programmable prescaler. The prescaler divides the oscillator frequency within a range of 1 to 64. The EPA also allows two channels to control a single output pin that is useful for high-speed PWM generation.

Serial I/O Port (SIO)—The SIO (also known as the UART) supports 8- or 9-bit data frames with one synchronous mode and 3 asynchronous modes. The synchronous mode transmits or receives 8 bits of data without start or stop bits and generates a shift clock. All other devices must synchronize to the 8XC196KR/KT's shift clock. The asynchronous frames contain a start and stop bit, making them either 10 or 11 bits long. The 11-bit frames allow implementation of specialized multiprocessor communication interfaces. Two of the asynchronous modes support parity error detection. All three asynchronous modes support full or half duplex operation. Also included is a dedicated baud rate generator. The SIO on the 8XC196KR/KT is compatible with all MCS-96 and MCS-51 devices.

Synchronous Serial I/O Port (SSIO)—The SSIO includes two Serial I/O communication ports with separate data and clock pins. The data format is eight data bits only. The clock and data pins can be inputs or outputs. This peripheral supports several standard synchronous serial protocols. A handshake mode allows two serial channels to transfer data without requiring extra lines to convey their status. The handshake mode also permits servicing of the SSIO by the PTS. The serial channel includes a dedicated baud rate generator. Each channel has a single byte buffer. If clocked externally, both channels can simultaneously operate at different frequencies. Maximum baud rate is $\frac{1}{8}$ the oscillator frequency. The transmission or reception of a byte sets an interrupt pending flag.

A/D Converter—Converts analog inputs to a digital equivalent. Resolution is either 8 or 10 bits with programmable sample and convert times. The main components of the A/D converter are: 8 analog inputs, 8 to 1 multiplexer, sample and hold capacitor and the resistor ladder. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. Another function implemented with the A/D converter is threshold detection. The converter generates an interrupt when the analog input is greater than or less than a programmed digital value. The KR/KT provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 37 interrupt sources and 18 interrupt vectors on the 8XC196KR/KT. With so many more sources than vectors, the KR/KT implements indirect interrupts. 17 of the interrupts are direct, which means each interrupt has one source and a dedicated vector location. The remaining 20 interrupt sources are the indirect interrupts. The term indirect is used because they share the same interrupt vector and another register identifies the interrupt source. The register, EPAIPV, contains the highest ending interrupt. EPAIPV is read to determine the interrupt needing sevice. The TIJMP instruction with EPAIPV simplifies the servicing of indirect interrupts. The direct interrupts include: NMI, External Interrupt, Trap, Unimplemented Opcode, SIO interrupts, SSIO interrupts, slave port interrupts, A/D converter and the lower 4 EPA channels. The indirect interrupts include: the upper 6 EPA channels, the 2 compare channels, all 10 EPA overruns and both timer overflows.

Peripheral Transaction Server (PTS)—The PTS is a microcoded hardware interrupt processor. It responds to interrupts with a fixed set of actions. These actions consist of: transferring data, starting an A/D conversion or generating PWM outputs. The PTS completes these tasks much faster than using interrupt driven service routines. The PTS can service all interrupts except NMI, Trap and Unimplemented Opcode. The register PTSSEL selects the interrupts handled by the PTS. Each interrupt managed by the PTS requires a block of data called the PTS Control Block (PTSCB). Each PTSCB requires 8 data bytes in register RAM. The PTSCB determines: the type of PTS, the number of PTS responses (if applicable), the source for data and the destination (if applicable). PTS cycles have a higher priority than interrupts and may temporarily suspend interrupt service routines.

Slave Port—The slave port is an interface between the KR/KT and a microprocessor. The KR/KT sits on the address/data bus of the processor and is accessed as a memory mapped peripheral. The slave port includes: a chip select input, 8-bit bidirectional data bus, an address input line, ALE input (to latch the address), $\overline{WR}$ and $\overline{RD}$ inputs to input/output data and an interrupt output. The address line and the $\overline{RD}/\overline{WR}$ select which registers are accessed (Output data, Status output, Input data or Command input). The various control signals and port structure allow the KR/KT and the processor to communicate with each other without having to be synchronized.

8.0 8XC196NT PERIPHERALS

Extended Address Port (EPORT)—The 80C196NT is the first member of the MCS-96 family to offer addressing that exceeds 64 Kbytes. The 80C196NT has a 1 Mbyte liner address space which is implemented through 4 address lines added by the EPORT. EPORT lines are individually assigned to function as either address or I/O. When assigned as I/O, they have the same functionality as a standard I/O port. As an input, the pin is a true high-impedance with no pull-ups or pull-downs. As an output, the pin is either complementary or open-drain. When assigned as address, the EPORT outputs address A16–A19. The address is strongly driven through the entire bus cycle, eliminating the need for an address latch.

Standard I/O Ports—The 8XC196NT has six 8-bit I/O ports. Each pin operates as a dedicated input or output. Most pins also have an alternate function. The NT does not use the quasi-bidirectional port pins found on previous MCS-96 devices. As an input, the pin is a true high impedance with no pull-ups or pull-downs. Most ports (Ports 1, 2, 5 and 6) have direction registers (Px__DIR), mode registers (Px__MODE), data input registers (Px__PIN) and data output registers (Px__REG). This allows the user to configure each port pin as input, output, open-drain output or alternate function. Ports 3 and 4 have Px__PIN and Px__REG registers and lack internal pull-ups. As standard outputs, these pins can only function in open-drain mode and need external pull-ups. Ports 3 and 4 also are the multiplexed address/data bus. When emitting the address, an internal pull-up device is active and does not need external pull-ups. Port 0 is the analog input port, and only has a Px__PIN register because there are no output drivers. As a digital port, Port 0 pins can only function as inputs.

Event Processor Array (EPA)—The EPA performs input event capture and output event generation functions using Timer1 and Timer2. It consists of 10 capture/compare modules, 2 compare only modules and the 2 timers. In capture mode, when an external event occurs the EPA stores the value of the timer, generates an interrupt or both. A rising, falling, or any edge can trigger a capture. All captures are double buffered. In compare mode, when the timer matches the value in the compare register the EPA changes the state of an output pin, generates an interrupt, or both. The EPA sets, resets or toggles the pin when the compare occurs. The timers can count up or count down. The clock source to the timers can be internal or external. The clock also goes through a programmable prescaler. The prescaler divides the oscillator frequency within a range of 1 to 64. The EPA also allows two channels to control a single output pin that is useful for high-speed PWM generation.

Serial I/O Port (SIO)—The SIO (also known as the UART) supports 8- or 9-bit data frames with one synchronous mode and 3 asynchronous modes. The synchronous mode transmits or receives 8 bits of data without start or stop bits and generates a shift clock. All other devices must synchronize to the 8XC196NT's shift clock. The asynchronous frames contain a start and stop bit, making them either 10 or 11 bits long. The 11-bit frames allow implementation of specialized multiprocessor communication interfaces. Two of the asynchronous modes support parity error detection. All three asynchronous modes support full or half duplex operation. Also included is a dedicated baud rate generator. The SIO on the 8XC196NT is compatible with all MCS-96 and MCS-51 devices.

Synchronous Serial I/O Port (SSIO)—The SSIO includes two Serial I/O communication ports with separate data and clock pins. The data format is eight data bits only. The clock and data pins can be inputs or outputs. This peripheral supports several standard synchronous serial protocols. A handshake mode allows two serial channels to transfer data without requiring extra lines to convey their status. The handshake mode also permits servicing of the SSIO by the PTS. The serial channel includes a dedicated baud rate generator. Each channel has a single byte buffer. If clocked externally, both channels can simultaneously operate at different frequencies. Maximum baud rate is $1/8$ the oscillator frequency. The transmission or reception of a byte sets an interrupt pending flag.

A/D Converter—Converts analog inputs to a digital equivalent. Resolution is either 8 or 10 bits with programmable sample and convert times. The main components of the A/D converter are: 4 analog inputs, 4 to 1 multiplexer, sample and hold capacitor and the resistor ladder. Refer to the data sheet for all specifications on A/D performance. The A/D Quick Reference section defines the A/D terms. Another function implemented with the A/D converter is threshold detection. The converter generates an interrupt when the analog input is greater than or less than a programmed digital value. The NT provides separate V_{REF} and ANGND supply pins to isolate noise on the V_{CC} or V_{SS} lines.

Interrupts—There are 37 interrupt sources and 18 interrupt vectors on the 8XC196NT. With so many more sources than vectors, the NT implements indirect interrupts. 17 of the interrupts are direct, which means each interrupt has one source and a dedicated vector location. The remaining 20 interrupt sources are the indirect interrupts. The term indirect is used because they share the same interrupt vector and another register identifies the interrupt source. The register, EPAIPV, contains the highest ending interrupt. EPAIPV is read to determine the interrupt needing service. The TIJMP instruction with EPAIPV simplifies the servicing of indirect interrupts. The direct interrupts include: NMI, External Interrupt, Trap, Unimplemented Opcode, SIO interrupts, SSIO interrupts, slave port interrupts, A/D converter and the lower 4 EPA channels. The indirect interrupts include: the upper 6 EPA channels, the 2 compare channels, all 10 EPA overruns and both timer overflows.

Peripheral Transaction Server (PTS)—The PTS is a microcoded hardware interrupt processor. It responds to interrupts with a fixed set of actions. These actions consist of: transferring data, starting an A/D conversion or generating PWM outputs. The PTS completes these tasks much faster than using interrupt driven service routines. The PTS can service all interrupts except NMI, Trap and Unimplemented Opcode. The register PTSSEL selects the interrupts handled by the PTS. Each interrupt managed by the PTS requires a block of data called the PTS Control Block (PTSCB). Each PTSCB requires 8 data bytes in register RAM. The PTSCB determines: the type of PTS, the number of PTS responses (if applicable), the source for data and the destination (if applicable). PTS cycles have a higher priority than interrupts and may temporarily suspend interrupt service routines.

Slave Port—The slave port is an interface between the NT and a microprocessor. The NT sits on the address/data bus of the processor and is accessed as a memory mapped peripheral. The slave port includes: a chip select input, 8-bit bidirectional data bus, an address input line, ALE input (to latch the address), $\overline{WR}$ and $\overline{RD}$ inputs to input/output data and an interrupt output. The address line and the $\overline{RD}/\overline{WR}$ select which registers are accessed (Output data, Status output, Input data or Command input). The various control signals and port structure allow the NT and the processor to communicate with each other without having to be synchronized.

9.0 8XC196MC PERIPHERALS

On-Chip Peripherals—The 8XC196MC's on-chip peripherals provide special functions useful in a variety of applications. The peripherals are monitored and controlled via special function registers (SFRs) that can be accessed indirectly or windowed and thereby treated as CPU "accumulators."

I/O Ports—The 8XC196MC has 7 I/O ports, labeled 0–6. Individual port pins are multiplexed to serve for standard I/O or to carry special signals. All ports are 8-bit except port 1 which is a 5-bit port.

Ports 0, 1, 2 and 6 are controlled by SFRs that can be directly addressed by the RALU through a window in the register file. Ports 0 and 1 serve as input to the 13-channel A/D, and can also be read as digital inputs. Port 2 can be configured either as standard I/O ports or to serve special functions. Port 6 is the output port for the PWM and WG units.

Ports 3, 4 and 5 are memory mapped and cannot be windowed. These ports are accessed only via 16-bit addresses. Ports 3 and 4 also serve as the 16-bit external address/data bus. The Port 5 lines can be selected for standard I/O or to serve as system bus control pins.

Timers and the Event Processor Array (EPA)—The Event Processor Array (EPA) performs input and output functions associated with timers 1 and 2. In the input mode the EPA monitors an input pin for signal transitions and records the timer value when the event occurs. The "captured" event is thus tagged with its time. In the output mode the EPA waits until the timer matches a stored time value and then sets, clears or toggles an output pin. This is a "compare" event. Both capture and compare events initiate interrupts which can be handled by a normal service routine or the PTS. The 8XC196MC has 4 capture/compare modules and 4 compare-only modules.

The two 16-bit timers can be clocked by the internal clock generator or by external sources. An external "quadrature clocking" mode is available for monitoring speed and direction from a position encoder.

Pulse Width Modulation Unit—The 8XC196MC has a PWM module that provides two PWM outputs. This module is in addition to the waveform generator. The

duty cycle and the period of each output is programmable through a respective 8-bit register. The module has an 8-bit counter, two 8-bit PWM compare registers and an 8-bit period register. The PWM output pins are controlled with bits in the output control register of the waveform generator.

A/D Converter—The 13-channel A/D converter can perform 10-bit conversions or faster 8-bit conversions. Automated A/D conversions and result storage are facilitated by the A/D scan mode of the PTS. The sample-and-hold times and the conversion times are programmable. The A/D can also act as a programmable comparator and issue an interrupt when the input crosses a threshold. Conversions can be performed on the analog ground and reference voltage, and the results can be used to calculate gain and zero offset errors. The zero offset compensation circuit is also programmable, enabling automatic offset adjustment.

Interrupt Controller and Peripheral Transaction Server (PTS)—The 8XC196MC's flexible interrupt handling system has two main components: the programmable interrupt controller and the Peripheral Transaction Server (PTS). The interrupt controller has a hardware priority scheme that can be modified by user software. These interrupts are serviced by user-written interrupt service routines. The user can select most interrupts to be serviced by the PTS instead of the programmable interrupt controller. The PTS has several microcoded hardware interrupt service routines whose execution is interleaved with normal instruction execution. The result is high-speed, low-overhead interrupt handling. The PTS can perform single and burst transfers of bytes or 16-bit words between any memory locations, manage multiple analog-to-digital (A/D) conversions and control a software serial channel which allows either synchronous or asynchronous operations.

Waveform Generator—The Waveform Generator (WG) produces 3 pairs of complimentary PWM signals. This peripheral is optimized for controlling 3-phase induction AC motors. It can also control brushless DC motors and DC to AC inverters. A dead-time generator and phase inverter circuit provide non-overlapping on-timers for each PWM output pair. Each signal is independently programmable.

intel®

MCS®-96 A/D Converter Quick Reference

October 1991

Order Number: 272115-001

1.0 The MCS-96 A/D Converter

Analog inputs to the MCS-96 family are handled by the A/D converter system. As shown in Figure 1, the converter system has an 8 channel multiplexer, a sample and hold, and a 10-bit successive approximation A/D converter. Conversions can be performed on one of 8 channels, the inputs of which share pins with port 0.

There are various versions of the A/D converter, depending on the specific device type. The 8X9X family offers a 10-bit fixed conversion time. The 8XC196KB family offers a 10-bit conversion with either a fast or slow conversion time. The 8XC196KC family offers an 8- or 10-bit conversion with programmable sample and convert times. The 8XC196KR has all of the KC features, with the addition of offset correction and internal conversion of V_{ref} and ANGND. The 8XC196MC includes all of the KR features, and the multiplexer has been expanded to 13 analog input channels.

This chapter describes the basic operation and terminology of the A/D converter. The different devices control the A/D in different ways, but the principals of operation remain the same throughout.

1.1 A/D Conversion Process

The conversion process is initiated by an HSO or EPA command, or by writing a one to the GO Bit in the A/D Control Register. Either activity causes a start conversion signal to be sent to the A/D converter control logic.

Once the A/D unit receives a start conversion signal, there is a one state time delay before sampling (Sample Delay) while the successive approximation register is reset and the proper multiplexer channel is selected. After the sample delay, the multiplexer output is connected to the sample capacitor and remains connected for the sample time. After the "sample window" closes, the input to the sample capacitor is disconnected from the multiplexer so that changes on the input pin will not alter the stored charge while the conversion is in progress. The comparator is then auto-zeroed and the conversion begins. The sample delay and sample time uncertainties are each approximately ±50 ns, independent of clock speed.

To perform the actual analog-to-digital conversion the MCS-96 implements a successive approximation algorithm. The converter hardware consists of a 256-resistor ladder, a comparator, coupling capacitors and a 10-bit successive approximation register (SAR) with logic that guides the process. The resistor ladder provides 20 mV steps (V_{REF} = 5.12V), while capacitive coupling creates 5 mV steps within the 20 mV ladder voltages. Therefore, 1024 internal reference voltages are available for comparison against the analog input to generate a 10-bit conversion result.

A successive approximation conversion is performed by comparing a sequence of reference voltages, to the analog input, in a binary search for the reference voltage that most closely matches the input. The ½ full scale reference voltage is the first tested. This corresponds to a 10-bit result where the most significant bit is zero, and all other bits are ones (0111.1111.11b). If the analog input was less than the test voltage, bit 10 of the SAR is left a zero, and a new test voltage of ¼ full scale (0011.1111.11b) is tried. If this test voltage was lower than the analog input, bit 9 of the SAR is set and bit 8 is cleared for the next test (0101.1111.11b). This binary search continues until 10 tests have occurred, at which time the valid 10-bit conversion result resides in the SAR where it can be read by software.

1.2 A/D Interface Suggestions

The external interface circuitry to an analog input is highly dependent upon the application, and can impact converter characteristics. In the external circuit's design, important factors such as input pin leakage, sample capacitor size and multiplexer series resistance from the input pin to the sample capacitor must be considered.

These factors are idealized in Figure 1. The external input circuit must be able to charge a sample capacitor (C_S) through a series resistance (R_I) to an accurate voltage given a DC leakage (I_L). Typically C_S is around 2 pF, R_I is around 5 KΩ and I_L is specified as 3 μA. In determining the necessary source impedance R_S, the value of V_{BIAS} is not important.

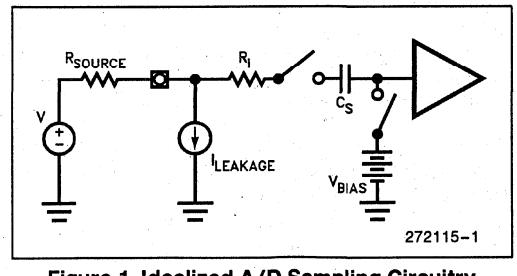


Figure 1. Idealized A/D Sampling Circuitry

External circuits with source impedances of 1 KΩ or less will be able to maintain an input voltage within a tolerance of about ±0.61 LSB (1.0 KΩ × 3.0 μA = 3.0 mV) given the DC leakage. Source impedances above 2 KΩ can result in an external error of at least one LSB due to the voltage drop caused by the 3 μA leakage. In addition, source impedances above 25 KΩ may degrade converter accuracy as a result of the internal sample capacitor not being fully charged during the sample window.

If large source impedances degrade converter accuracy because the sample capacitor is not charged during the sample time, an external capacitor connected to the pin compensates for this. Since the sample capacitor is 2 pF, a 0.005 μF capacitor (2048 * 2 pF) will charge the sample capacitor to an accurate input voltage of $\pm$0.5 LSB. An external capacitor does not compensate for the voltage drop across the source resistance, but charges the sample capacitor fully during the sample time.

Placing an external capacitor on each analog input will also reduce the sensitivity to noise, as the capacitor combines with series resistance in the external circuit to form a low-pass filter. In practice, one should include a small series resistance prior to the external capacitor on the analog input pin and choose the largest capacitor value practical, given the frequency of the signal being converted. This provides a low-pass filter on the input, while the resistor will also limit input current during over-voltage conditions.

Figure 2 shows a simple analog interface circuit based upon the discussion above. The circuit in the figure also provides limited protection against over-voltage conditions on the analog input. Should the input voltage inappropriately drop significantly below ground, diode D2 will forward bias at about 0.8 DCV. Since the specification of the pin on most devices has an absolute maximum low voltage of -0.3V, this will leave about 0.5V across the 270Ω resistor, or about 2 mA of current. This should limit the current to a safe amount. Note that if any input pins are driven much beyond V_{REF} or below ANGND, the accuracy of all analog input channels may be adversely affected. This is because the input protection circuit will start to conduct, thus injecting current into the internal reference circuitry and upsetting the reference voltage. Refer to the data sheet for exact device specifications.

However, before any circuit is used in an actual application, it should be thoroughly analyzed for applicability to the specific problem at hand.

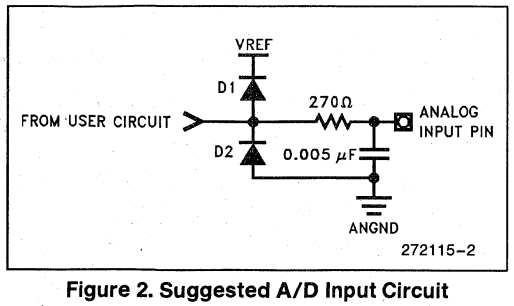


Figure 2. Suggested A/D Input Circuit

ANALOG REFERENCES

Reference supply levels and noise strongly influence the absolute accuracy of the conversion. For this reason, it is recommended that the ANGND pin be tied to the V_{SS} pins close to the device. Bypass capacitors should also be used between V_{REF} and ANGND. ANGND should be within about a tenth of a volt of V_{SS}. V_{REF} should be well regulated and used only for the A/D converter. The V_{REF} supply needs to be able to source around 5 mA.

Note that if only ratiometric information is desired, V_{REF} can be connected to V_{CC}. In addition, V_{REF} and ANGND must be connected even if the A/D converter is not being used. Remember that Port 0 receives its power from the V_{REF} and ANGND pins even when it is used as digital I/O.

1.3 The A/D Transfer Function

The conversion result is a 8- or 10-bit ratiometric representation of the input voltage, so the numerical value obtained from the conversion will be:

$$\text{INT}\ [255 \times (V_{IN} - \text{ANGND})/(V_{REF} - \text{ANGND})]\ \text{or}$$

$$\text{INT}\ [1023 \times (V_{IN} - \text{ANGND})/(V_{REF} - \text{ANGND})]$$

This produces a stair-stepped transfer function when the output code is plotted versus input voltage (see Figure 3). The resulting digital codes can be taken as simple ratiometric information, or they provide information about absolute voltages or relative voltage changes on the inputs. The more demanding the application is on the A/D converter, the more important it is to fully understand the converter's operation. For simple applications, knowing the absolute error of the converter is sufficient. However, closing a servo-loop with analog inputs necessitates a detailed understanding of an A/D converter's operation and errors.

The errors inherent in an analog-to-digital conversion process are many: quantizing error, zero offset, full-scale error, differential non-linearity and non-linearity. These are "transfer function" errors related to the A/D converter. In addition, converter temperature drift, V_{CC} rejection, sample-hold feedthrough, multiplexer off-isolation, channel-to-channel matching and random noise should be considered. Fortunately, one "Absolute Error" specification is available which describes the sum total of all deviations between the actual conversion process and an ideal converter. However, the various sub-components of error are important in many applications. These error components are described in the text below where ideal and actual converters are compared.

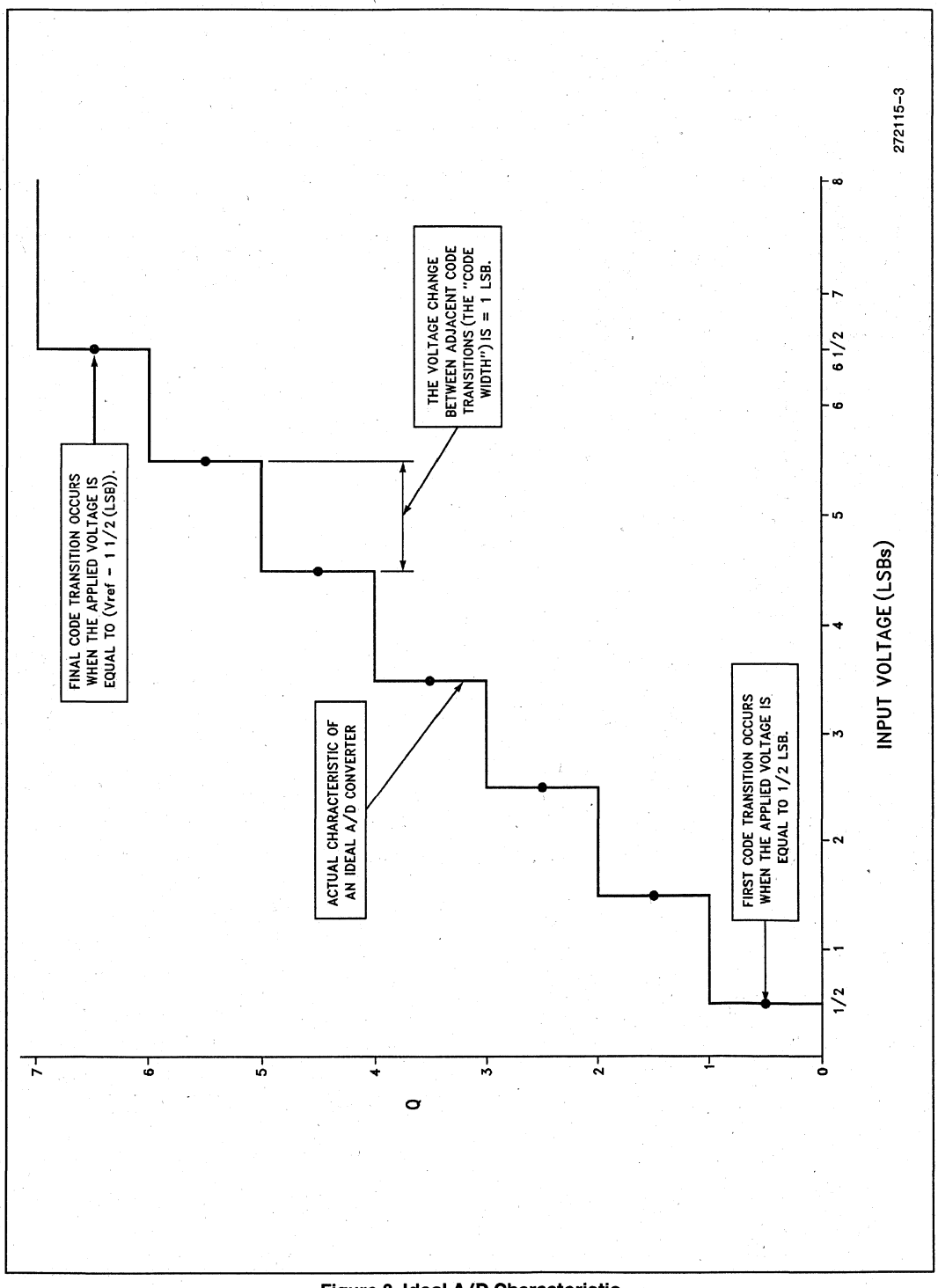


Figure 3. Ideal A/D Characteristic

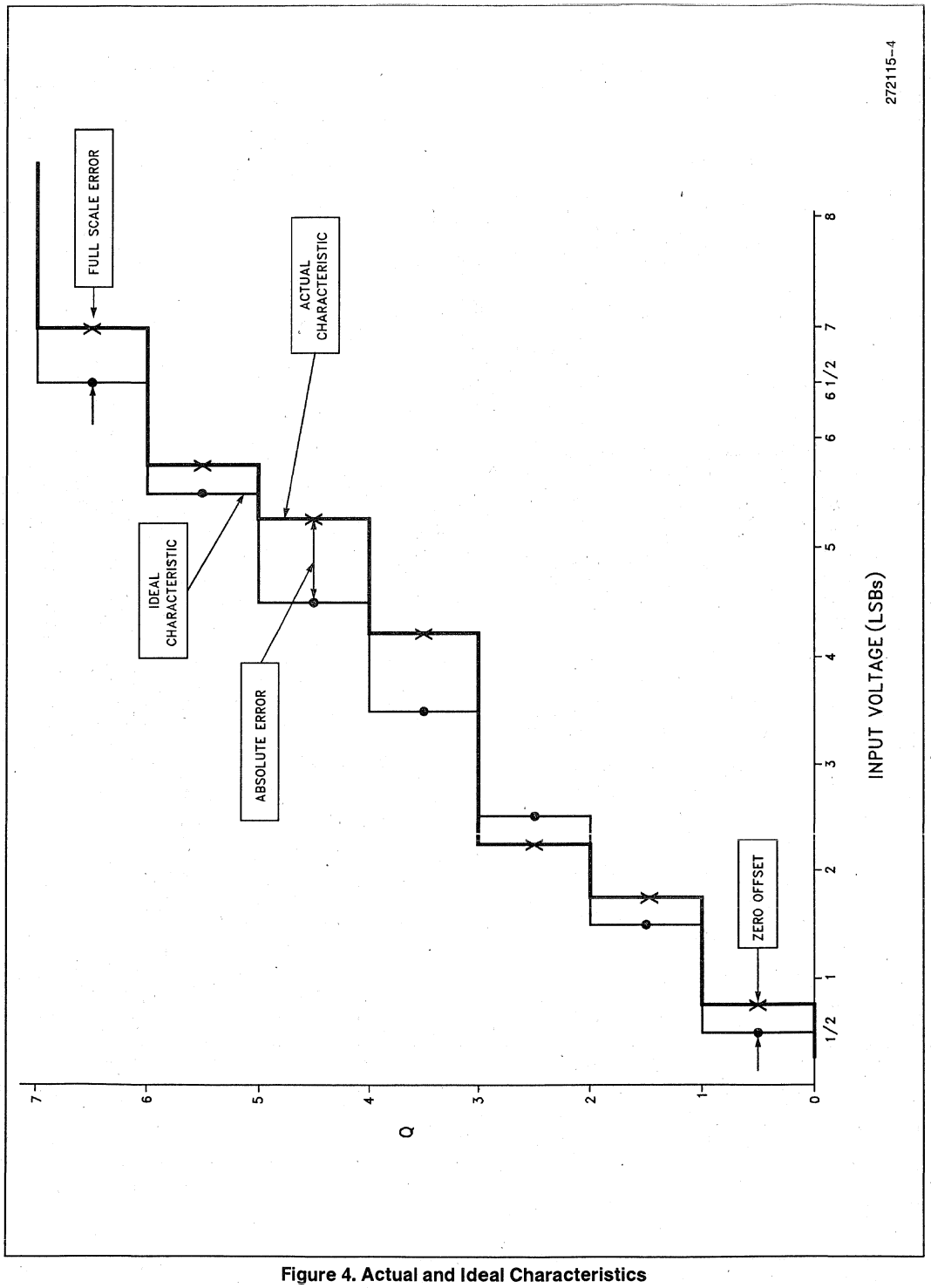


Figure 4. Actual and Ideal Characteristics

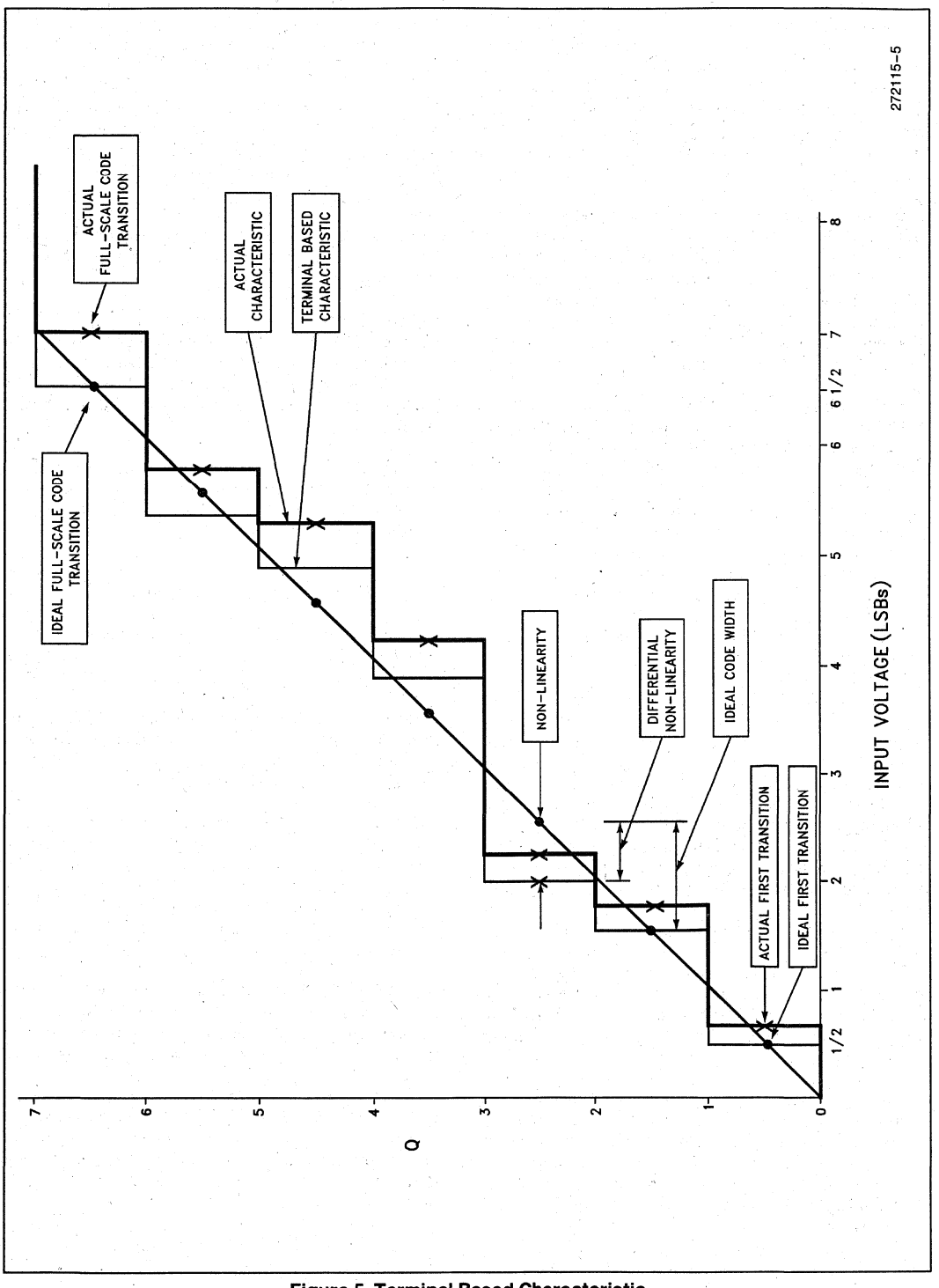


Figure 5. Terminal Based Characteristic

An unavoidable error simply results from the conversion of a continuous voltage to an integer digital representation. This error is called quantizing error, and is always ±0.5 LSB. Quantizing error is the only error seen in a perfect A/D converter, and is obviously present in actual converters. Figure 3 shows the transfer function for an ideal 3-bit A/D converter (i.e., the Ideal Characteristic).

Note that in Figure 3 the Ideal Characteristic possesses unique qualities: its first code transition occurs when the input voltage is 0.5 LSB; its full-scale code transition occurs when the input voltage equals the full-scale reference minus 1.5 LSB; and its code widths are all exactly one LSB. These qualities result in a digitization without offset, full-scale or linearity errors. In other words, a perfect conversion.

Figure 4 shows an Actual Characteristic of a hypothetical 3-bit converter, which is not perfect. When the Ideal Characteristic is overlaid with the imperfect characteristic, the actual converter is seen to exhibit errors in the location of the first and final code transitions and code widths. The deviation of the first code transition from ideal is called "zero offset", and the deviation of the final code transition from ideal is "full-scale error". The deviation of the code widths from ideal causes two types of errors. Differential Non-Linearity and Non-Linearity. Differential Non-Linearity is a local linearity error measurement, whereas Non-Linearity is an overall linearity error measure.

Differential Non-Linearity is the degree to which actual code widths differ from the ideal one LSB width. It gives the user a measure of how much the input voltage may have changed in order to produce a one count change in the conversion result. Non-Linearity is the worst case deviation of code transitions from the corresponding code transitions of the Ideal Characteristic. Non-Linearity describes how much Differential Non-Linearities could add up to produce an overall maximum departure from a linear characteristic. If the Differential Non-Linearity errors are too large, it is possible for an A/D converter to miss codes or exhibit non-monotonicity. Neither behavior is desirable in a closed-loop system. A converter has no missed codes if there exists for each output code a unique input voltage range that produces that code only. A converter is monotonic if every subsequent code change represents an input voltage change in the same direction.

Differential Non-Linearity and Non-Linearity are quantified by measuring the Terminal Based Linearity Errors. A Terminal Based Characteristic results when an Actual Characteristic is shifted and rotated to eliminate zero offset and full-scale error (see Figure 5). The Terminal Based Characteristic is similar to the Actual Characteristic that would be seen if zero offset and full-scale error were externally trimmed away. In practice, this is done by using input circuits which include gain and offset trimming. In addition, V_{REF} could also be closely regulated and trimmed within the specified range to affect full-scale error.

Other factors that affect a real A/D Converter system include sensitivity to temperature, failure to completely reject all unwanted signals, multiplexer channel dissimilarities and random noise. Fortunately these effects are small.

Temperature sensitivities are described by the rate at which typical specifications change with a change in temperature.

Undesired signals come from three main sources. First, noise on V_{CC}–V_{CC} Rejection. Second, input signal changes on the channel being converted after the sample window has closed–Feedthrough. Third, signals applied to channels not selected by the multiplexer–Off-Isolation.

Finally, multiplexer on-channel resistances differ slightly from one channel to the next causing Channel-to-Channel Matching errors, and random noise in general results in Repeatability errors.

1.4 A/D Glossary of Terms

Figures 3, 4 and 5 display many of these terms. Refer to AP-406 'MCS-96 Analog Acquisition Primer' for additional information on the A/D terms.

ABSOLUTE ERROR–The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

ACTUAL CHARACTERISTIC–The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An Actual Characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversion under the same conditions.

BREAK-BEFORE-MAKE–The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected. (e.g., the converter will not short inputs together.)

CHANNEL-TO-CHANNEL MATCHING–The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

CHARACTERISTIC–A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

CODE–The digital value output by the converter.

CODE CENTER–The voltage corresponding to the midpoint between two adjacent code transitions.

CODE TRANSITION–The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

CODE WIDTH–The voltage corresponding to the difference between two adjacent code transitions.

CROSSTALK–See "Off-Isolation".

DC INPUT LEAKAGE–Leakage current to ground from an analog input pin.

DIFFERENTIAL NON-LINEARITY–The difference between the ideal and actual code widths of the terminal based characteristic of a converter.

FEEDTHROUGH–Attenuation of a voltage applied on the selected channel of the A/D converter after the sample window closes.

FULL SCALE ERROR–The difference between the expected and actual input voltage corresponding to the full scale code transition.

IDEAL CHARACTERISTIC–A characteristic with its first code transition at V_{IN} = 0.5 LSB, its last code transition at V_{IN} = (V_{REF} − 1.5 LSB) and all code widths equal to one LSB.

INPUT RESISTANCE–The effective series resistance from the analog input pin to the sample capacitor.

LSB (LEAST SIGNIFICANT BIT)–The voltage value corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For a 10-bit converter with a reference voltage of 5.12 volts, one LSB is 5.0 mV. Note that this is different than digital LSBs, since an uncertainty of two LSBs, when referring to an A/D converter, equals 10 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 20 mV.)

MONOTONIC–The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

NO MISSED CODES–For each and every output code, there exists a unique input voltage range which produces that code only.

NON-LINEARITY–The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristics.

OFF-ISOLATION–Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

REPEATABILITY–The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

RESOLUTION–The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

SAMPLE DELAY–The delay from receiving the start conversion signal to when the sample window opens.

SAMPLE DELAY UNCERTAINTY–The variation in the Sample Delay.

SAMPLE TIME–The time that the sample window is open.

SAMPLE TIME UNCERTAINTY–The variation in the sample time.

SAMPLE WINDOW–Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

SUCCESSIVE APPROXIMATION–An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

TEMPERATURE COEFFICIENTS–Change in the stated variable per degree centigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effects of temperature drift.

TERMINAL BASED CHARACTERISTIC–An Actual Characteristic which has been rotated and translated to remove zero offset and full-scale error.

V_{CC} REJECTION–Ratio of the change in the A/D characteristic to the change in V_{CC}.

ZERO OFFSET–The difference between the expected and actual input voltage corresponding to the first code transition.

8XC196KB16
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

- 8 Kbytes of On-Chip ROM/OTP Available
- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 1.75 μs 16 x 16 Multiply (16 MHz)
- 3.0 μs 32/16 Divide (16 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- 16 MHz Standard
- Dedicated 15-Bit Baud Rate Generator
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol
- Extended Temperature Available

The 8XC196KB16 is a 16-bit microcontroller available in three different memory varieties: ROMless (80C196KB), 8K ROM (83C196KB) and 8K OTP (One Time Programmable—87C196KB). The 8XC196KB16 is a high performance member of the MCS® 96 microcontroller family. The 8XC196KB16 has the same peripheral set as the 8096BH and has a true superset of the 8096BH instructions. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

Bit, byte, word and some 32-bit operations are available on the 80C196KB. With a 16 MHz oscillator a 16-bit addition takes 0.50 μs, and the instruction times average 0.37 μs to 1.1 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

The 8XC196KB16 has a maximum guaranteed frequency of 16 MHz. The ROM device does not have a speed indicator at the end of the device name. Instead it has a ROM code number.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

Package Designators: N = 68-pin PLCC, S = 80-pin QFP (commercial only). Prefix Designators: T = Extended Temperature.

December 1996

Order Number: 270909-007

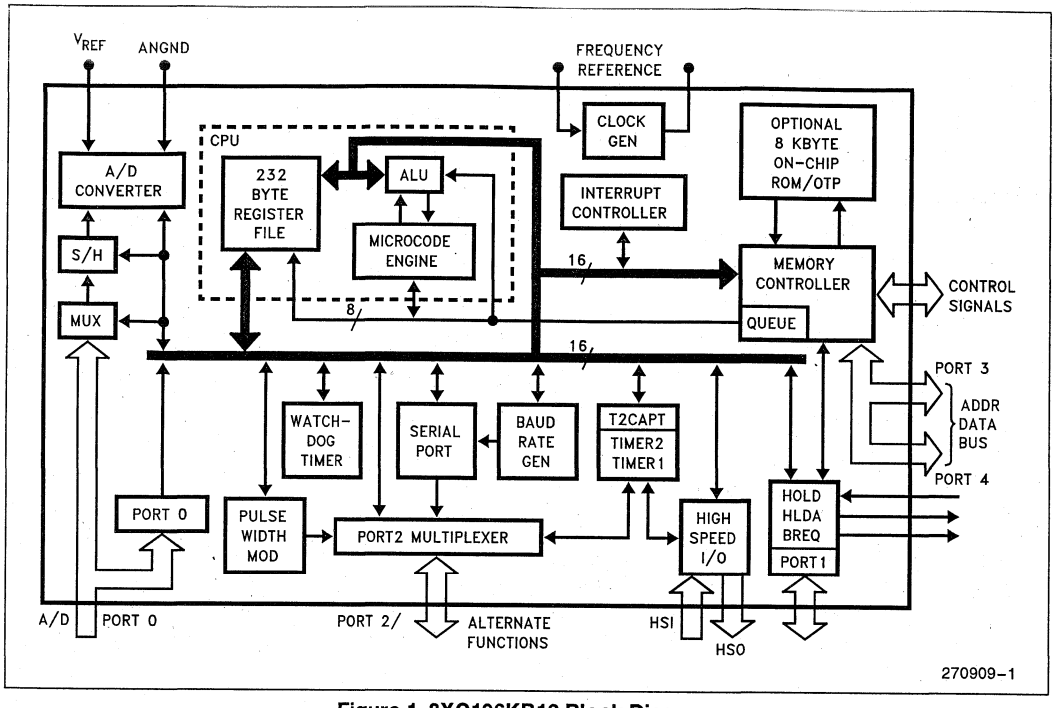
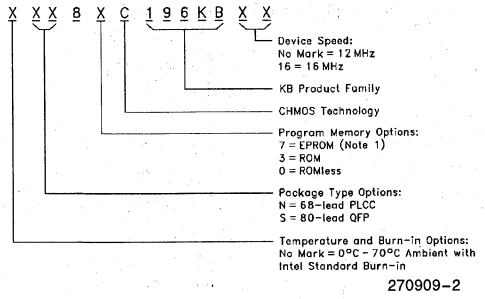


Figure 1. 8XC196KB16 Block Diagram

PROCESS INFORMATION

This device is manufactured on P629.0 and 629.1, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196KB16 is 68-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 2. The 8XC196KB16 Nomenclature

Table 1. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	70°C/W	4°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 2. 8XC196KB16 Memory Map

Description	Address
External Memory or I/O	0FFFFH 04000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	3FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4	1FFFH 1FFEH
External Memory	1FFDH 0100H
232 Bytes Register RAM (Note 1)	00FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 00FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KB16 quick reference for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

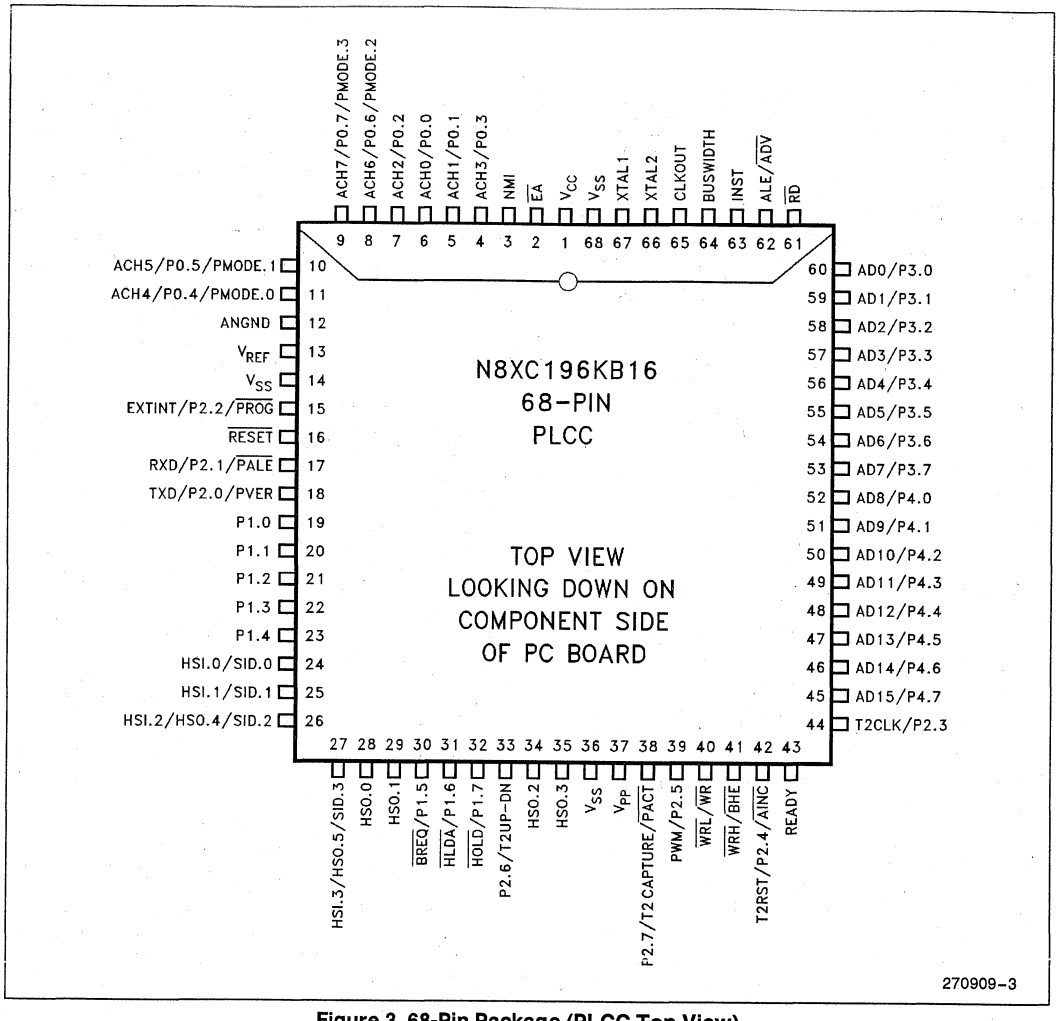
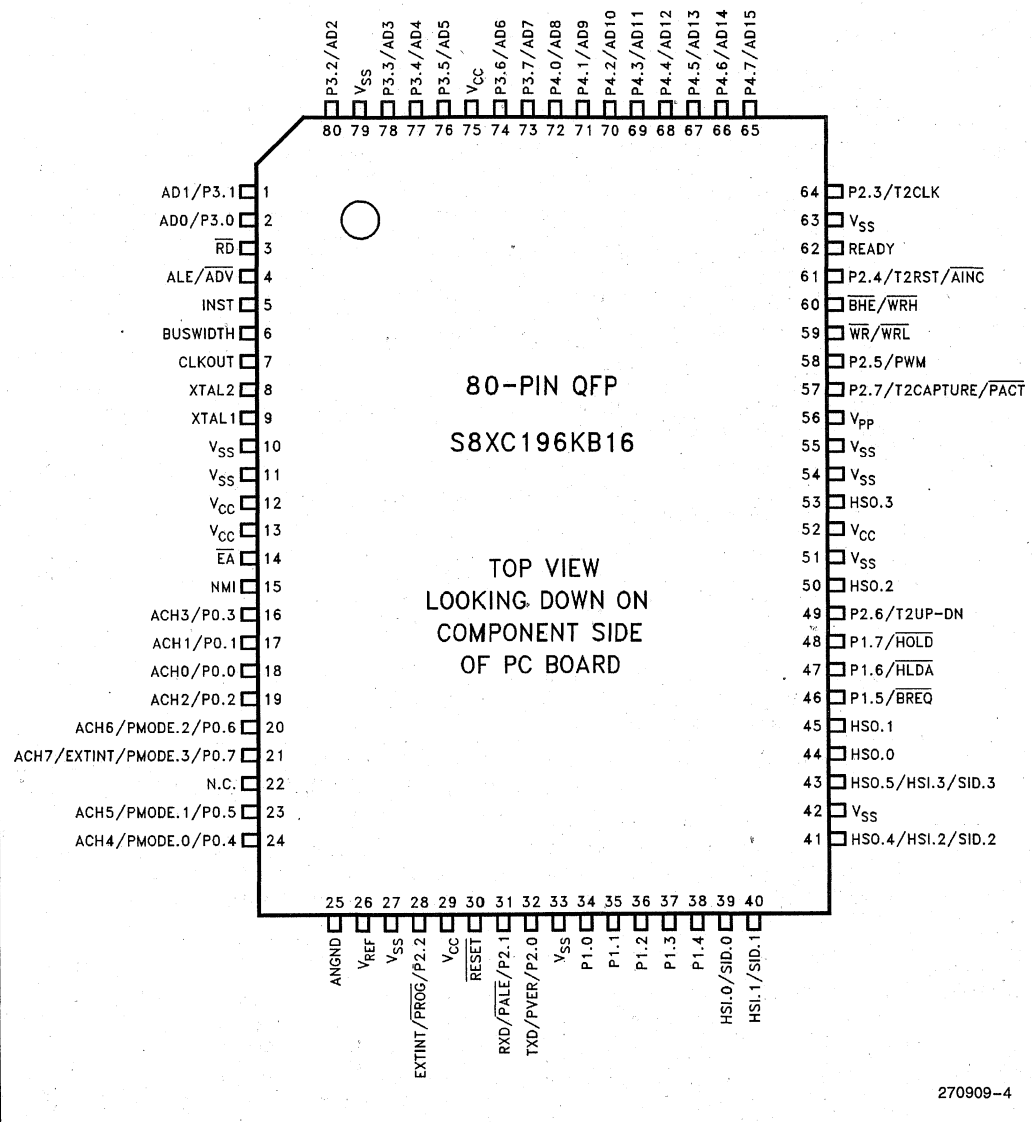


Figure 3. 68-Pin Package (PLCC Top View)

NOTE:
The above pin out diagram applies to the OTP (87C196KB) device. The OTP device uses all of the programming pins shown above. The ROM (83C196KB) device only uses programming pins: AINC, PALE, PMODE.n, and PROG. The ROMless (80C196KB) doesn't use any of the programming pins.



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 4. 80-Pin QFP Package

NOTE:
The above pin out diagram applies to the OTP (87C196KB) device. The OTP device uses all of the programming pins shown above. The ROM (83C196KB) device only uses programming pins: AINC, PALE, PMODE.n, and PROG. The ROMless (80C196KB) doesn't use any of the programming pins.

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of them must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}. Connect V_{SS} and ANGND at chip to avoid noise problems.
V_{PP}	Programming voltage. Also timing pin for the return from power down circuit.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time RESET sequence.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch and output low indicates a data fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/OTPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being addressed. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle (held not ready) is available in the CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. Three pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port. These pins are shared with $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 87C196KB. Pins P2.6 and P2.7 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus, which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus. Enabled by setting WSR.7.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. In Mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. In Mode 0 the pin functions as input or output data.
EXTINT	A rising edge on the EXTINT pin will generate an external interrupt.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2.
PWM	The pulse width modulator output.
T2UP-DN	The T2UPDN pin controls the direction of Timer2 as an up or down counter.
T2CAPTURE	A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register.
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
SID	Slave ID Number. Used to assign each slave a pin of Port 3 or 4 to use for passing programming verification acknowledgement.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PACT}}$	Programming Active. Used in the Auto Programming Mode to indicate when programming activity is complete.
$\overline{\text{PVAL}}$	Program Valid. This signal indicates the success or failure of programming in the Auto Programming Mode. A zero indicates successful programming.
PVER	Program Verification. Used in Slave Programming and Auto CLB Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
Ports 3 and 4 (Programming Mode)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory. Should have pullups to V_{CC} when used in slave programming mode.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V
Power Dissipation(1) 1.5W

NOTE:
1. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency **16 MHz**	3.5	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (All Pins except XTAL1 and RESET)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)(2)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)(1)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA
I_{LI}	Input Leakage Current (Std. Inputs)(3)		±10	µA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		+3	µA	0 < V_{IN} < V_{REF}
I_{TL}	1 to 0 Transition Current (QBD Pins)(1)		−800	µA	V_{IN} = 2.0V
I_{IL}	Logical 0 Input Current (QBD Pins)(1)		−50	µA	V_{IN} = 0.45V

DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(7)	Max	Units	Test Conditions
I_{IL1}	Logical 0 Input Current in Reset $\overline{BHE}$, $\overline{WR}$, P2.0			−850	μA	V_{IN} = 0.45V
I_{IL2}	Logical 0 Input Current in Reset ALE, $\overline{RD}$, INST			−7	mA	V_{IN} = 0.45V
I_{IH1}	Logical 1 Input Current on NMI Pin			100	μA	V_{IN} = 2.0V
Hyst.	Hysteresis on RESET Pin	300			mV	
I_{CC}	Active Mode Current in Reset		50	60	mA	XTAL1 = 16 MHz V_{CC} = V_{PP} = V_{REF} = 5.5V
I_{REF}	A/D Converter Reference Current		2	5	mA	
I_{IDLE}	Idle Mode Current		10	25	mA	
I_{PD}	Powerdown Mode Current		5	30	μA	V_{CC} = V_{PP} = V_{REF} = 5.5V
R_{RST}	Reset Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES: (Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   - I_{OL} on Output pins: 10 mA
   - I_{OH} on quasi-bidirectional pins: self limiting
   - I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and V_{REF} = V_{CC} = 5V.

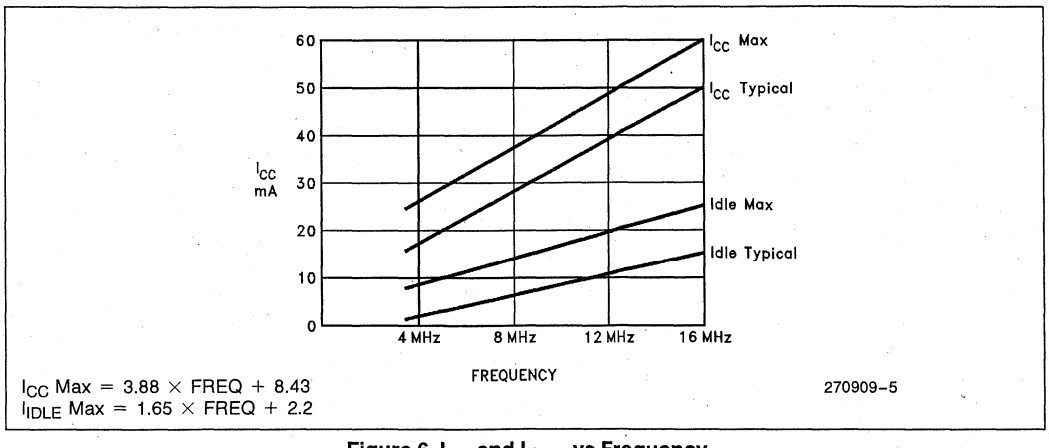


Figure 6. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 87C196KB:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{YLYH}	NonREADY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 75$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2T_{OSC} \times n$ where n = number of wait states.

AC CHARACTERISTICS (Continued)

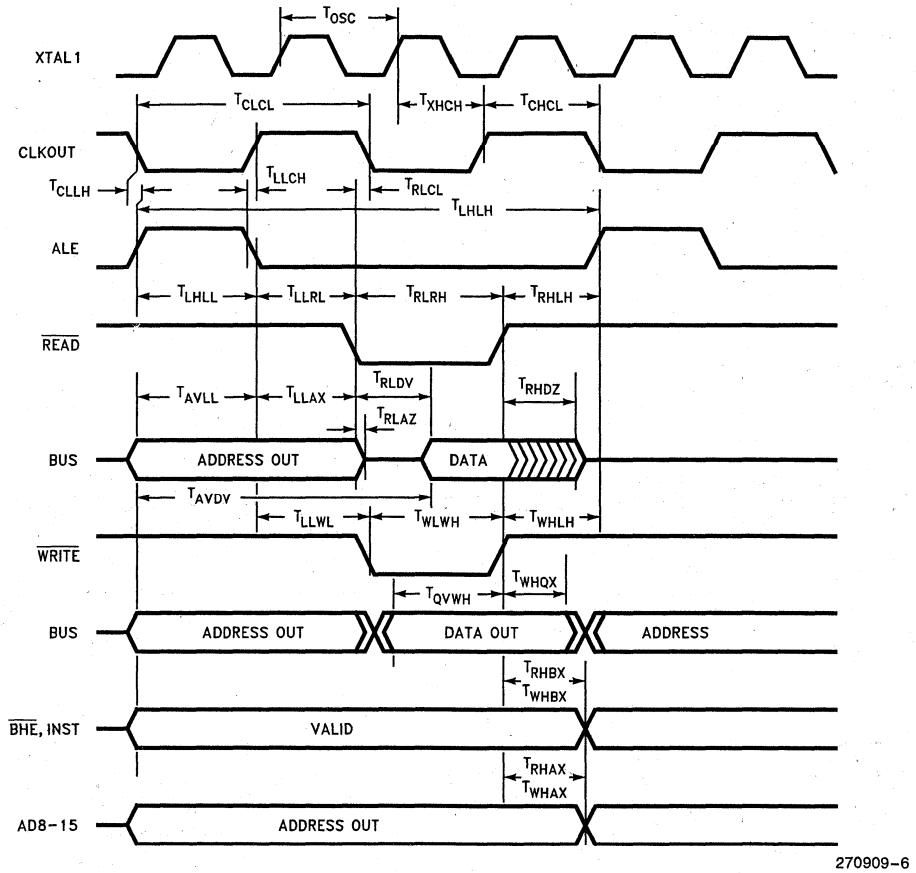
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The 87C196KB will meet these specifications:

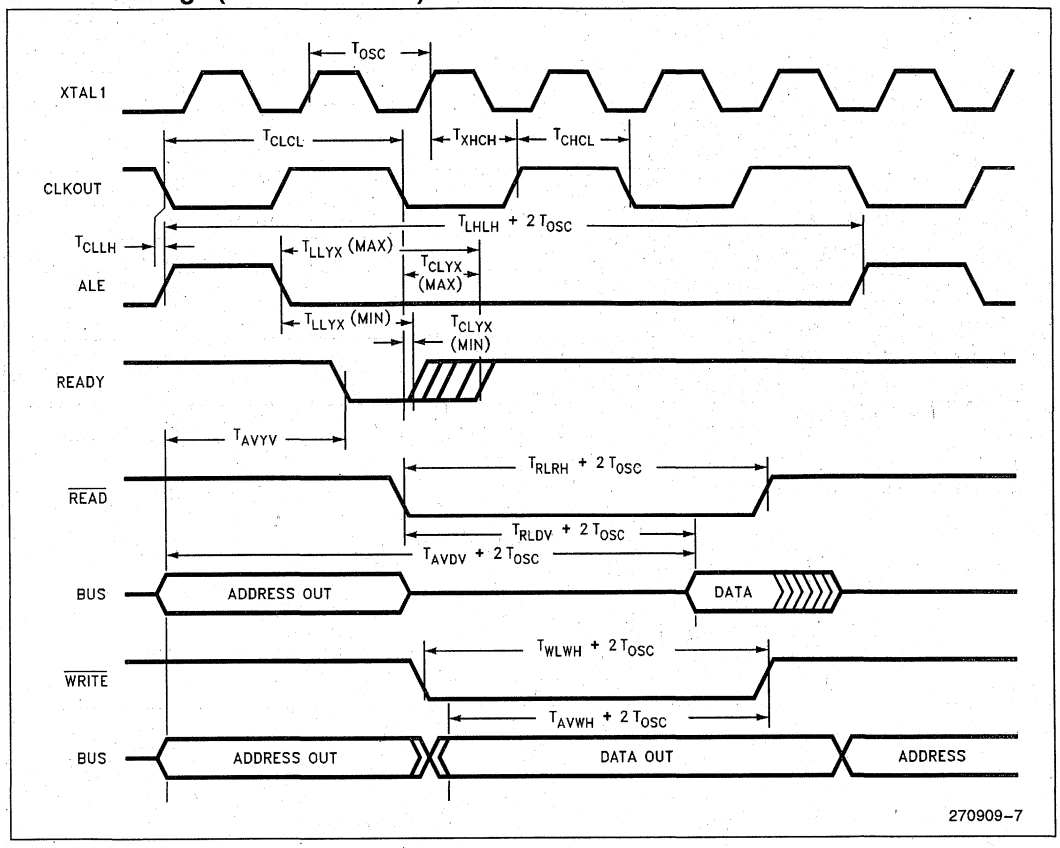
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **16 MHz**	3.5	16.0	MHz	(Note 2)
T_{OSC}	$1/F_{XTAL}$ **16 MHz**	62.5	286	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	+10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 3)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+25	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC}−5	T_{OSC} + 25	ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 1)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	(Note 3)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 15	T_{OSC} + 10	ns	(Note 1)
T_{WHBX}	$\overline{BHE}$, INST HOLD after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{RHBX}	$\overline{BHE}$, INST HOLD after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{RHAX}	AD8–15 hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:
1. Assuming back-to-back bus cycles.
2. Testing performed at 3.5 MHz, however, the device is static by design and will typically operate below 1 Hz.
3. When using wait states, all 2 T_{OSC}+ n where n = number of wait states.

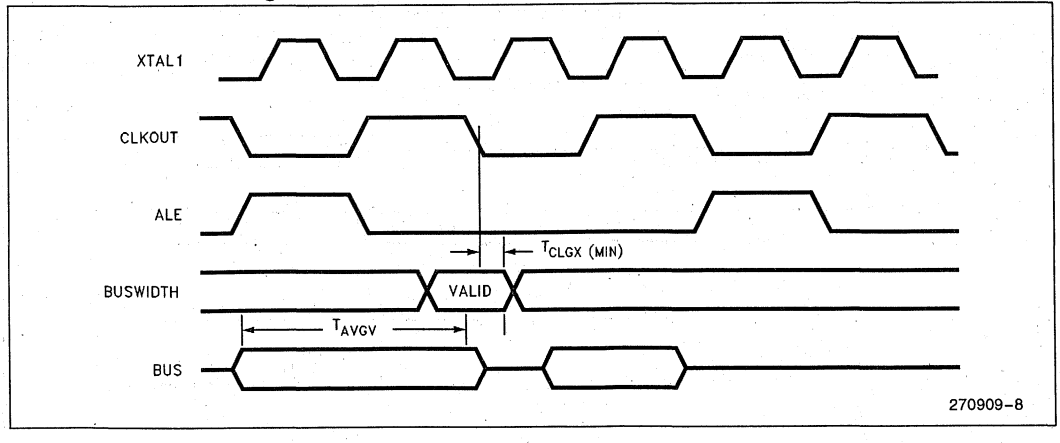
System Bus Timings



READY Timings (One Wait State)



Buswidth Bus Timings



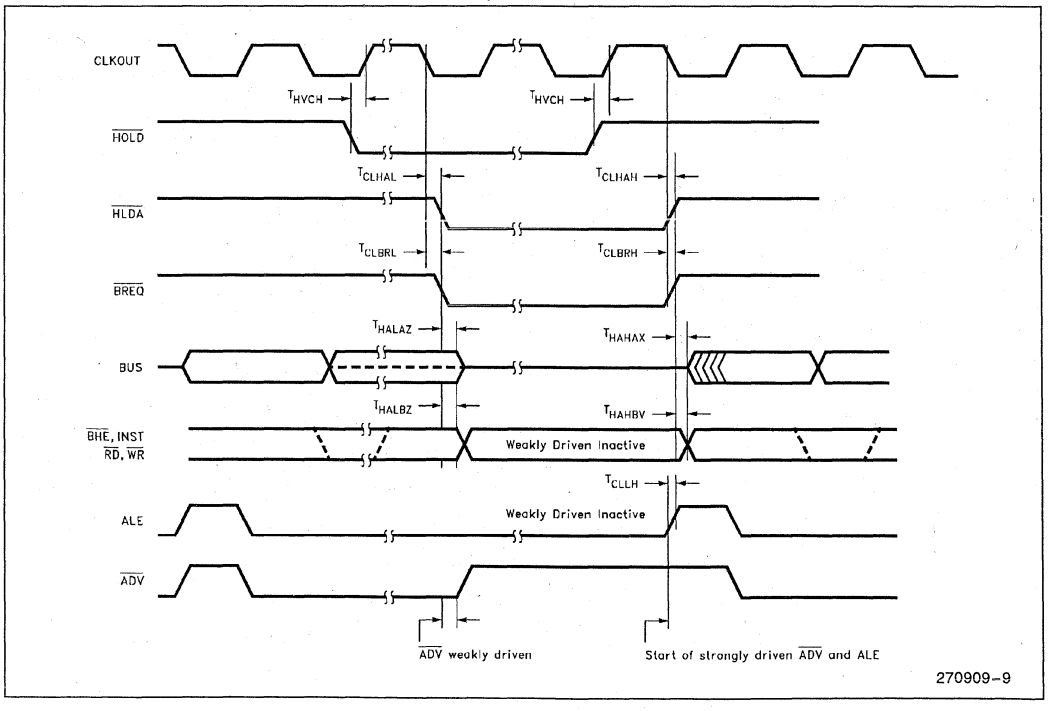
HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to HLDA Low		15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low		15	ns	
T_{HALAZ}	HLDA Low to Address Float		10	ns	
T_{HALBZ}	HLDA Low to BHE, INST, RD, WR Float		10	ns	
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	
T_{HAHAV}	HLDA High to Address Valid	0		ns	
T_{HAHBX}	HLDA High to BHE, INST, RD, WR No Longer Float	−20		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	0		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.

Maximum Hold Latency

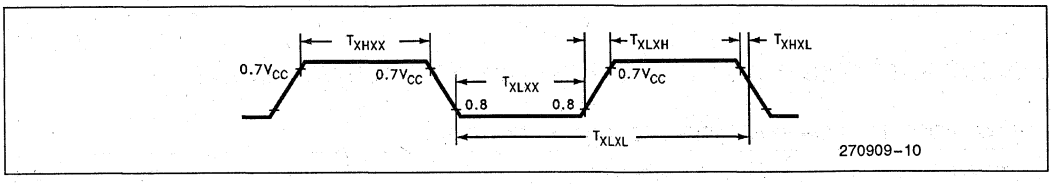
Bus Cycle Type	Latency
Internal Access	1.5 States
16-Bit External Execution	2.5 States
8-Bit External	4.5 States



EXTERNAL CLOCK DRIVE

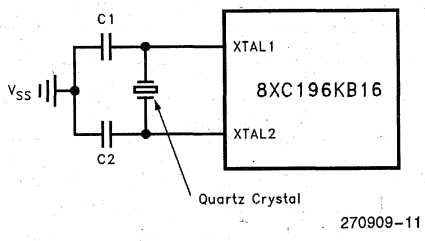
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency **16 MHz**	3.5	16	MHz
T_{XLXL}	Oscillator Period **16 MHz**	62.5	286	ns
T_{XHXX}	High Time	21.25		ns
T_{XLXX}	Low Time	21.25		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



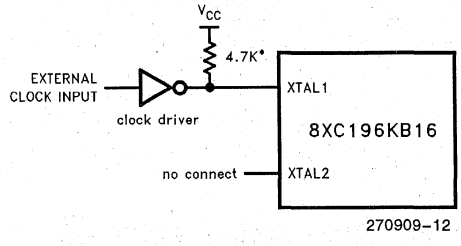
An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications, the capacitance will not exceed 20 pF.

EXTERNAL CRYSTAL CONNECTIONS



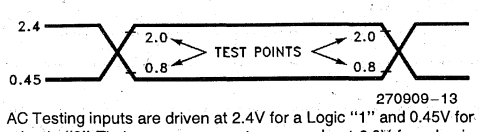
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

EXTERNAL CLOCK CONNECTIONS



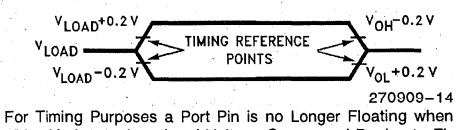
* Required if open-collector TTL driver used
Not needed if CMOS driver is used.

AC TESTING INPUT, OUTPUT WAVEFORMS



AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs; $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

Signals:

H	- High	A	- Address	G	- Buswidth	R	- $\overline{RD}$
L	- Low	B	- $\overline{BHE}$	H	- $\overline{HOLD}$	W	- $\overline{WR}/\overline{WRH}/\overline{WRL}$
V	- Valid	BR	- $\overline{BREQ}$	HA	- $\overline{HLDA}$	X	- XTAL1
X	- No Longer Valid	C	- CLKOUT	L	- ALE/$\overline{ADV}$	Y	- READY
Z	- Floating	D	- DATA IN	Q	- DATA OUT		

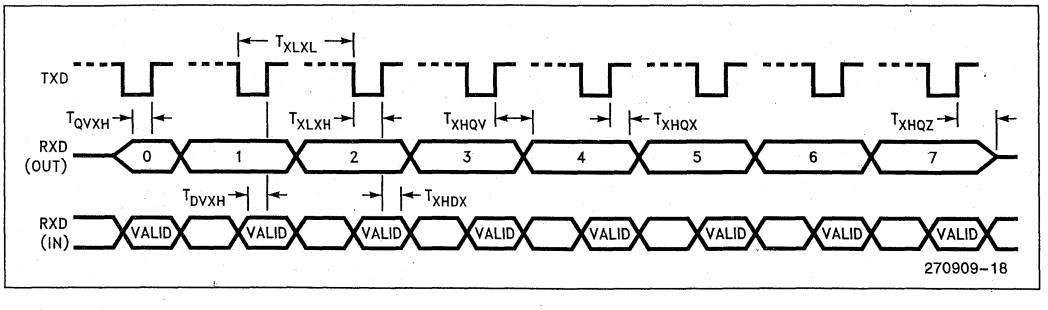
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} −50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} +50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		2 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)



10-BIT A/D CHARACTERISTICS

At a clock speed of 6 MHz or less, the clock prescaler should be disabled. This is accomplished by setting IOC2.4 = 1.

At higher frequencies (greater than 6 MHz) the clock prescaler should be enabled (IOC2.4 = 0) to allow the comparator to settle.

The table below shows two different clock speeds and their corresponding A/D conversion and sample times.

State times are calculated as follows:

$$\text{state time} = \frac{2}{\text{XTAL1}}$$

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

See the MCS-96 A/D Converter Quick Reference for definition of A/D terms.

Example Sample and Conversion Times

A/D Clock Prescaler	Clock Speed (MHz)	Sample Time (States)	Sample Time at Clock Speed (μs)	Conversion Time (States)	Conversion Time at Clock Speed (μs)
IOC2.4 = 0 → ON	16	15	1.875	156.5	19.6
IOC2.4 = 1 → OFF	6	8	2.667	89.5	29.8

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±3	LSBs	
Differential Non-Linearity Error		>−1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

OTPROM SPECIFICATIONS

OTPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages During Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	12.50	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
F_{OSC}	Oscillator Frequency **16 MHz**	6.0	16.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

AC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	40		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	50		T_{OSC}
T_{LLVL}	$\overline{PALE}$ Low to PVER Low		60	T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	40		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	120		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	120		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	40		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to PVER Low		90	T_{OSC}

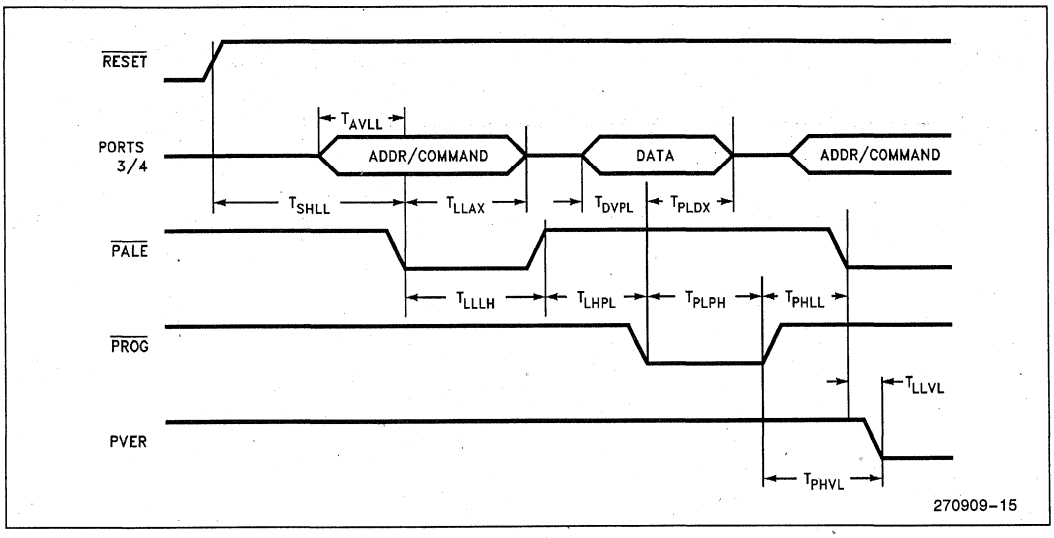
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

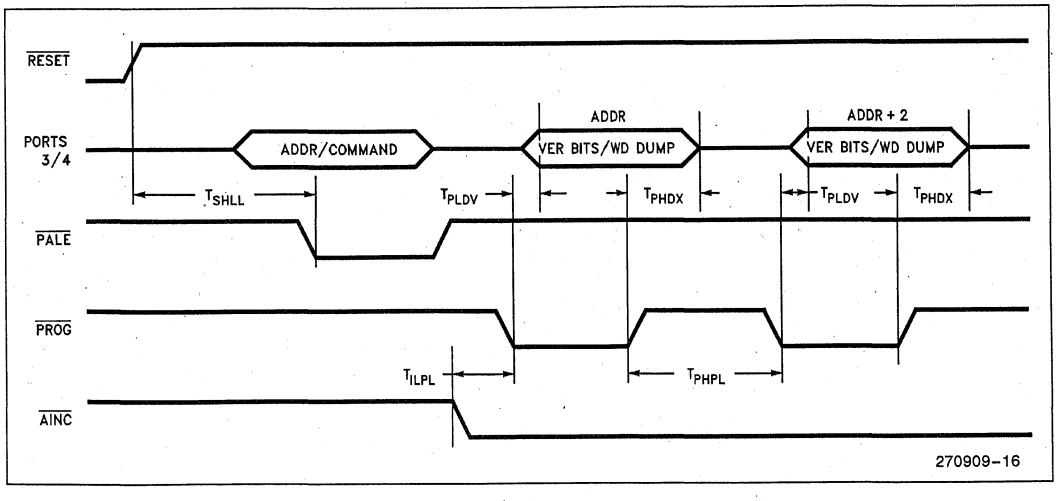
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

OTPROM PROGRAMMING WAVEFORMS

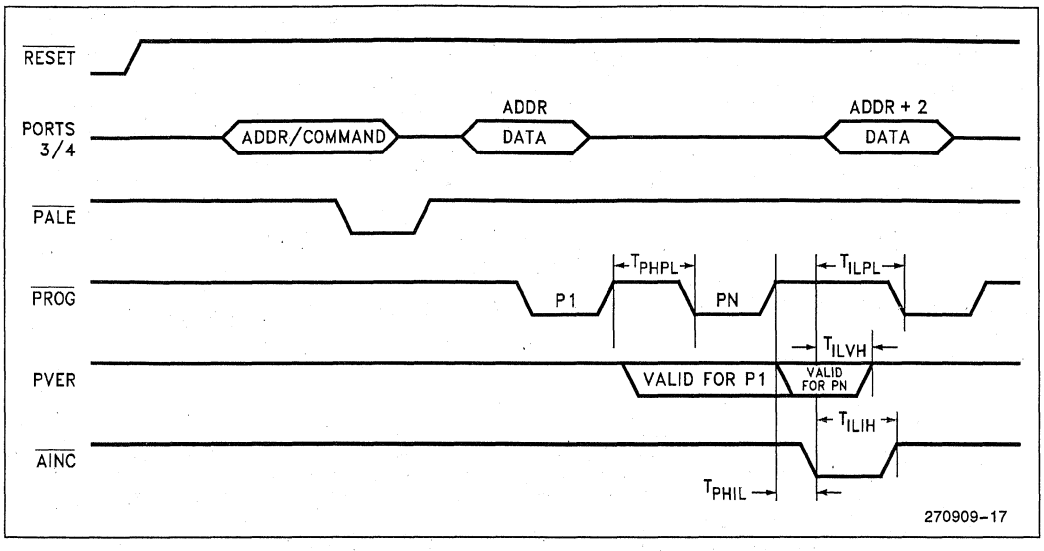
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



FUNCTIONAL DEVIATIONS

Devices marked with an "E", "F" or "G" have the following errata.

1. Missed Interrupt on P0.7, EXTINT

Interrupts occurring on P0.7 could be missed since the INT_PEND EXTINT bit may not be set. See techbit MC0893.

2. HSI_MODE Divide-by-Eight

See Faxback #2192

REVISION HISTORY

This data sheet (270909-006) is valid for devices with an "E", "F" or "G" at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (270909-006) and (270909-005):

1. Removed "Word Addressable Only" from Port 3 and 4 in Table 2.
2. Removed ICC1, active mode current at 3.5 MHz. This specification is not longer required.
3. Removed TLLYV and TLLGV from waveform diagrams.
4. The HSI errata and CMPL with R0 were removed as this is now considered normal operation.
5. The HSI_MODE divide-by-eight errata was added to the known errata section.

The following differences exist between this data sheet (270909-005) and (270909-004):

1. I_{TL} MAX was -650 µA (270909-004). Now I_{TL} MAX is -800 µA (270909-005).
2. I_{IL2} was named I_{IL1} (270909-004). Now I_{IL2} is correctly named (270909-005).
3. I_{IL1} was omitted (270909-004). I_{IL1} MAX was added. I_{IL1} MAX is -850 µA (270909-005).
4. T_{LLYV} and T_{LLGV} (270909-004) were removed. These timings are not required in high-speed system designs.
5. An errata was added to the known errata section. There is a possibility to miss an external interrupt on P0.7 EXTINT.

The following differences exist between this data sheet (270909-004) and (270909-003):

1. The ROM (80C196KB), and ROMless (83C196KB) were combined with this data sheet resulting in no specification differences.
2. The description of the prescalar bit for the A/D has been enhanced.
3. T_{HAHBV}MIN was -15 ns (270909-003). Now T_{HAHBV}MIN is -20 ns (270909-004).
4. T_{XHQZ}MAX was 1 TOSC (270909-003). Now T_{XHQZ}MAX is 2 TOSC (270909-004). This should have no impact on designs using synchronous serial mode 0.
5. The change indicators for the 80C196KB are "E", "F" and "G". Previously there was only one change indicator "E". The change indicator is used for tracking purposes. The change indicator is the last character in the FPO number. The FPO number is the second line on the top side of the device.

The following differences exist between (-003) and version (-002).

1. The 12 MHz and 16 MHz devices were combined in this data sheet. The 87C196KB 12 MHz only data sheet (272035-001) is now obsolete.
2. Changes were made to the format of the data sheet and the SFR descriptions were removed.
3. The -002 version of this data sheet was valid for devices marked with a "B" or a "D" at the end of the top side tracking number.
4. The OSCILLATOR errata was removed.
5. An errata was not documented in the -002 data sheet for devices marked with a "B" or a "D". This is the DIVIDE DURING HOLD/READY errata. When HOLD or READY is active and DIV/DIVB is the last instruction in the queue, the divide result may be incorrect.
6. T_{XCH} was changed from Min = 40 ns to Min = 20 ns.
7. T_{RLCL} was changed from Min = 5 ns to Min = 4 ns.
9. I_{IL1} was changed from Max = −6 mA to Max = −7 mA.
10. T_{HAHBV} was changed from Min = −10 ns to Min = −15 ns.

Differences between the -002 and -001 data sheets.

1. The -001 version of this data sheet was valid for devices marked with a "C" at the end of the top side tracking number.
2. Added 64L SDIP and 80L QFP packages.
3. Added IIH1.
4. Changed T_{CHWH} Min from − 10 ns to − 5 ns.
5. Changed T_{CHWH} Max from + 10 ns to + 15 ns.
6. Changed T_{WLWH} Min from T_{OSC} − 20 ns to T_{OSC} − 15 ns.
7. Changed T_{WHQX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
8. Changed T_{WHLH} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
9. Changed T_{WHLH} Max from T_{OSC} + 15 ns to T_{OSC} + 10 ns.
10. Changed T_{WHBX} Min from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
11. Changed T_{HVCH} Min from 85 ns to 55 ns.
12. Remove T_{HVCH} Max.
13. Changed T_{CLHAL} Min from − 10 ns to − 15 ns.
14. Changed T_{CLHAL} Max from 20 ns to 15 ns.
15. Changed T_{CLBRL} Min from − 10 ns to − 15 ns.
16. Changed T_{CLBRL} Max from 20 ns to 15 ns.
17. Changed T_{HAHAX} Min from − 10 ns to − 15 ns.
18. Added HSI description to Functional Deviations.
19. Added Oscillator description to Functional Deviations.

8XC198
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

8 Kbytes of OTPROM

- 8 Kbytes of On-Chip OTPROM or ROM
- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 1.75 μs 16 x 16 Multiply (16 MHz)
- 3.0 μs 32/16 Divide (16 MHz)
- Powerdown and Idle Modes
- 16-Bit Watchdog Timer
- 8-Bit External Bus
- 16 MHz Standard
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Counter
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with Sample/Hold
- Extended Temperature Available

The 8XC198 family offers low-cost entry into Intel's powerful MCS®-96 16-bit microcontroller architecture. Intel's CHMOS process provides a high performance processor along with low power consumption. To further reduce power requirements, the processor can be placed into Idle or Powerdown Mode.

The 8XC198 is the 8-bit bus version of the 8XC196KB. The prefixes mean: 80 (ROMless), 83 (ROM), 87 (OTP) One Time Programmable. The ROM and OTP are available in 8 Kbytes.

Bit, byte, word and some 32-bit operations are available on the 8XC198. With a 16 MHz oscillator a 16-bit addition takes 0.50 μs, and the instruction times average 0.37 μs to 1.1 μs in typical applications.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or counter. Also provided on-chip are an A/D converter, serial port, watchdog timer and a pulse-width-modulated output signal.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. Wth the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

October 1992

Order Number: 272034-003

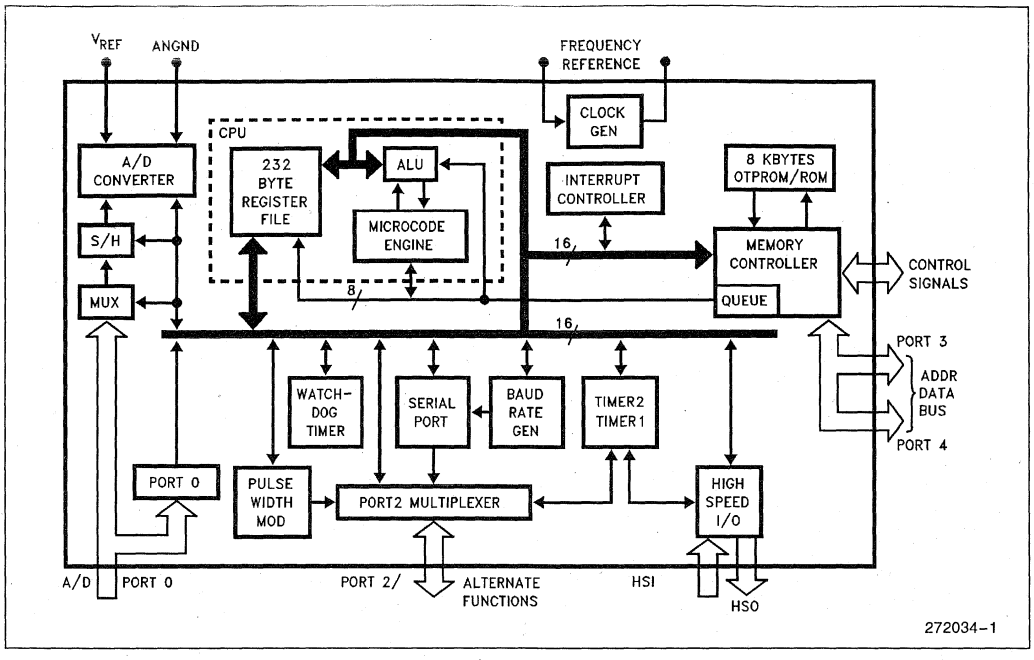


Figure 1. 87C198 Block Diagram

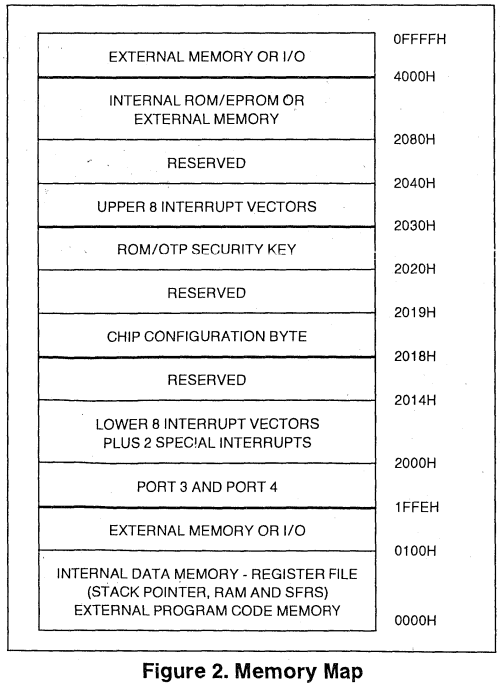


Figure 2. Memory Map

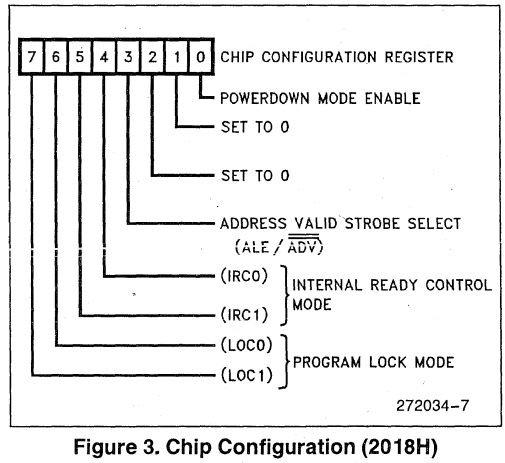


Figure 3. Chip Configuration (2018H)

WARNING:
Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

PACKAGING

The 8XC198 is available in a 52-pin PLCC package and an 80-pin QFP package. Contact your local sales office to determine the exact ordering code for the part desired.

Package Designators:
N = 52-pin PLCC
S = 80-pin QFP

Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	40°C/W	
QFP	70°C/W	4°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

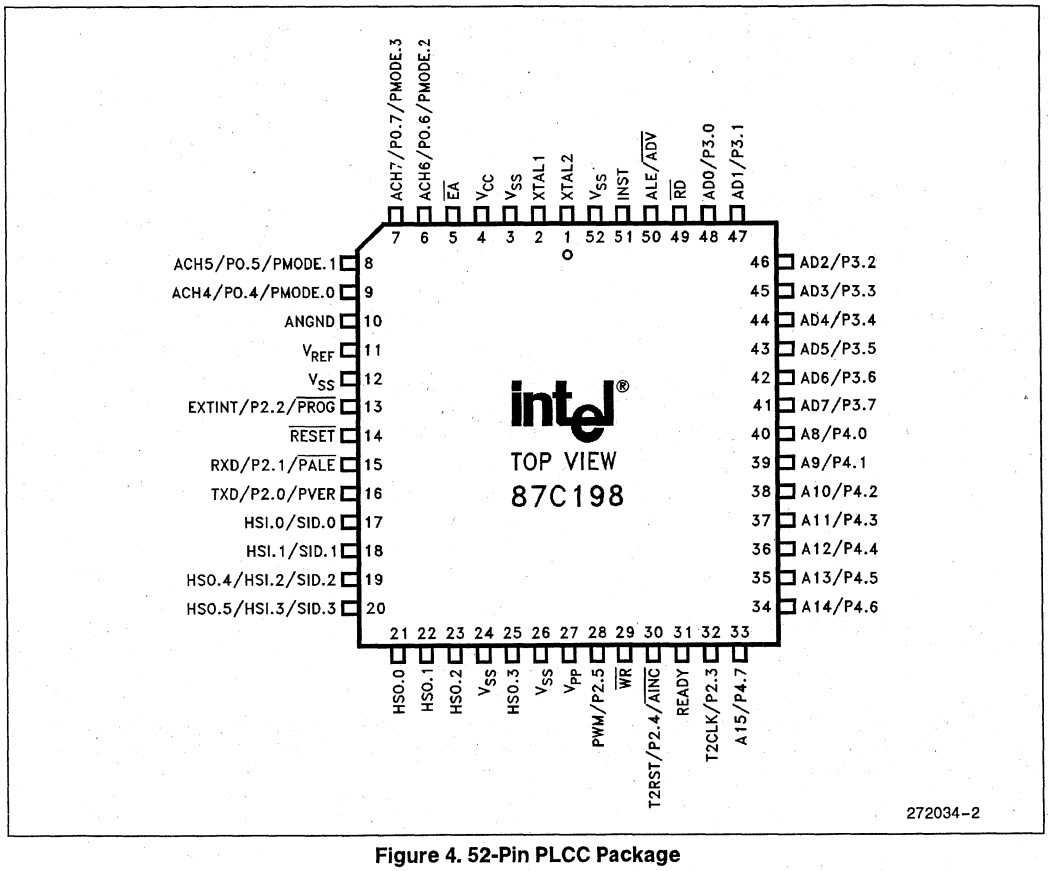
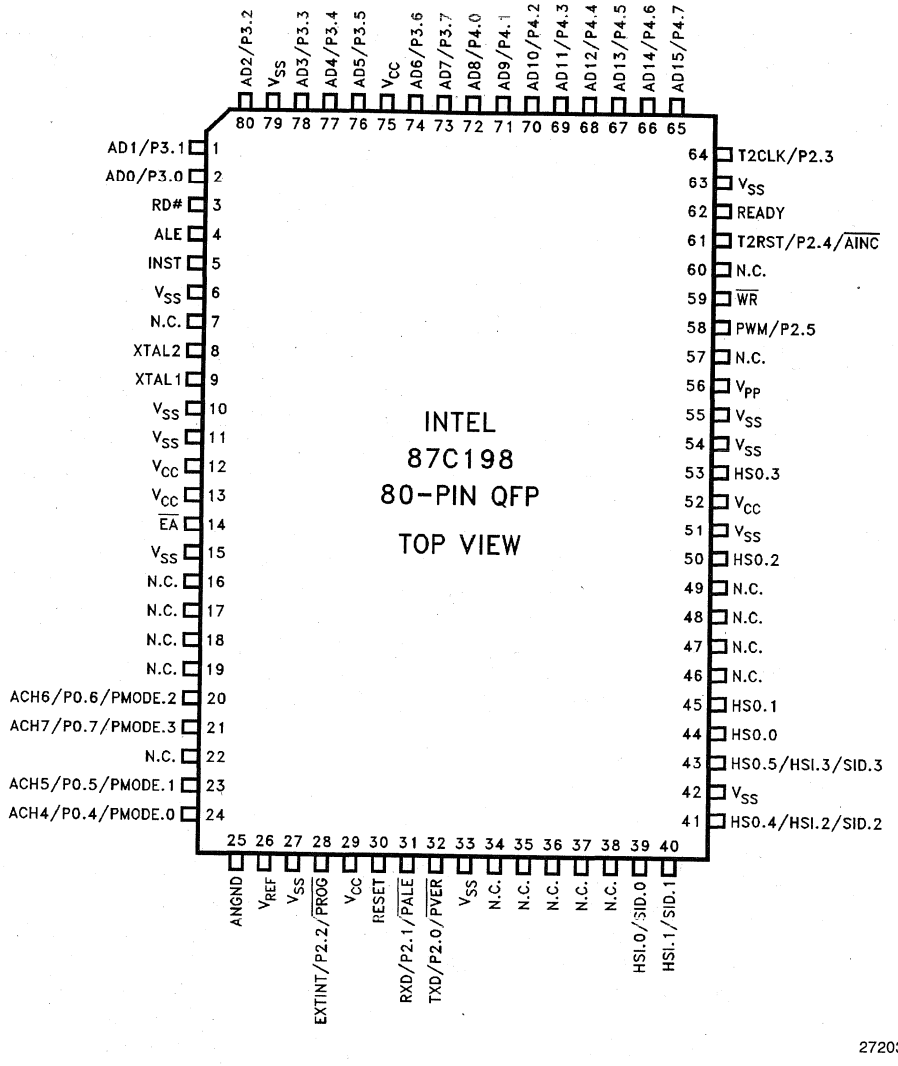


Figure 4. 52-Pin PLCC Package

NOTE:
The above pinout diagram applies to the OTP (87C198) device. The OTP device uses all of the programming pins shown above. The ROM (83C198) device only uses programming pins: **AINC, PALE, PMODE.n** and **PROG**. The ROMless (80C198) doesn't use any of the programming pins.



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 5. 80-Pin QFP Package

NOTE:
The above pinout diagram applies to the OTP (87C198) device. The OTP device uses all of the programming pins shown above. The ROM (83C198) device only uses programming pins: **AINC, PALE, PMODE.n** and **PROG**. The ROMless (80C198) doesn't use any of the programming pins.

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	The PLCC package has 5 V_{SS} pins and the QFP package has 12 V_{SS} pins. All must be connected to digital ground.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming Voltage. Also, timing pin for the return from powerdown circuit.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition commences the 10-state Reset Sequence.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$	Write output to external memory. $\overline{\text{WR}}$ will go low for every external write.
READY	Ready input to lengthen external memory cycles. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode on the EPROM device.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 2	Multi-functional port. All of its pins are shared with other functions in the 80C198.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Available as I/O only on the ROM and EPROM devices.
TxD	The TxD pin is used for serial port transmission in Modes 1, 2 and 3. In mode 0 the pin is used as the serial clock output.
RxD	Serial Port Receive pin used for serial port reception. In mode 0 the pin functions as input or output data.
EXTINT	A positive transition on the EXTINT pin will generate an external interrupt.
T2CLK	The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input.
T2RST	A rising edge on the T2RST pin will reset Timer2.
PWM	The PWM output.
PMODE	Programming Mode Select. Determines the EPROM programming algorithm that is performed. PMODE is sampled after a chip reset and should be static while the part is operating.
SID	Slave ID Number. Used to assign each slave a pin of Port 3 or 4 to use for passing programming verification acknowledgement.
$\overline{\text{PALE}}$	Programming ALE Input. Accepted by the 87C196KB when it is in Slave Programming Mode. Used to indicate that Ports 3 and 4 contain a command/address.
$\overline{\text{PROG}}$	Programming. Falling edge indicates valid data on PBUS and the beginning of programming. Rising edge indicates end of programming.
$\overline{\text{PVAL}}$	Program Valid. This signal indicates the success or failure of programming in the Auto Programming Mode. A zero indicates successful programming.
PVER	Program Verification. Used in Slave Programming and Auto CLB Programming Modes. Signal is low after rising edge of PROG if the programming was not successful.
$\overline{\text{AINC}}$	Auto Increment. Active low signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.
PORTS 3 and 4 (when programming)	Address/Command/Data Bus. Used to pass commands, addresses, and data to and from slave mode 87C196KBs. Used by chips in Auto Programming Mode to pass command, addresses and data to slaves. Also used in the Auto Programming Mode as a regular system bus to access external memory. Should have pullups to V_{CC} (15 kΩ).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +150°C

Voltage on V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.3V to +13.0V

Voltage on Any Other Pin to V_{SS} .. −0.5V to +7.0V

Power Dissipation(1) 1.5W

NOTE:
1. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

(All characteristics in this data sheet apply to these operating conditions unless otherwise noted.)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency **16 MHz**	3.5	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (1)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 32 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	µA	0 < V_{IN} < V_{CC} − 0.3V
I_{LI1}	Input Leakage Current (Port 0)		+3	µA	0 < V_{IN} < V_{REF}
I_{IL1}	Logical 0 Input Current in Reset (ALE, $\overline{RD}$, INST)		−6	mA	V_{IN} = 0.45 V
Hyst	Hysteresis on RESET Pin	300		mV	

NOTE:
1. All pins except RESET and XTAL1.

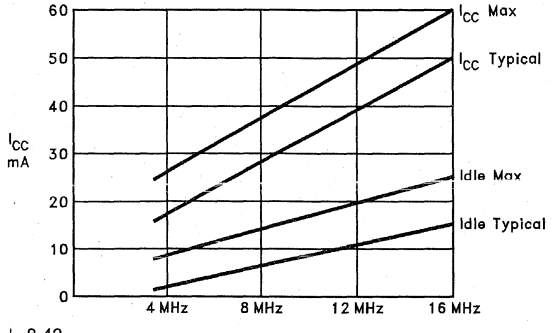
DC CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ(6)	Max	Units	Test Conditions
I_{CC}	Active Mode Current in Reset		50	60	mA	XTAL1 = 16 MHz
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current		10	25	mA	
I_{CC1}	Active Mode Current		15	25	mA	XTAL1 = 3.5 MHz
I_{PD}	Powerdown Mode Current		5	30	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
(Notes apply to all specifications)
1. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, INST, HSO pins, PWM/P2.5, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
2. Standard Inputs include HSI pins, $\overline{EA}$, READY, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
3. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below V_{CC} − 0.7V:
   I_{OL} on Output pins: 10 mA
   I_{OH} on Standard Output pins: 10 mA
4. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
5. During normal (non-transient) conditions the following total current limits apply:

HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, $\overline{WR}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST	I_{OL}: 13 mA	I_{OH}: 13 mA

6. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.



I_{CC} Max = 3.88 × FREQ + 8.43
I_{IDLE} Max = 1.65 × FREQ + 2.2

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Figure 8. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The system must meet these specifications to work with the 87C198:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to Ready Setup		$2T_{OSC} - 75$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 2)
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. When using wait states, add $2T_{OSC} \times n$, where n = number of wait states.

AC CHARACTERISTICS

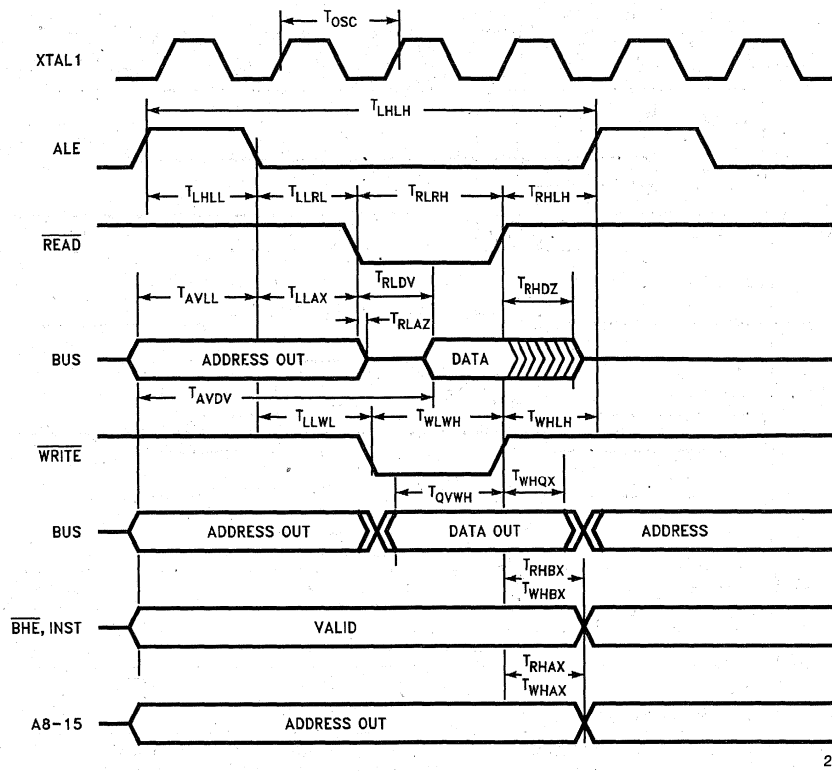
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 12/16 MHz

The 87C198 will meet these specifications:

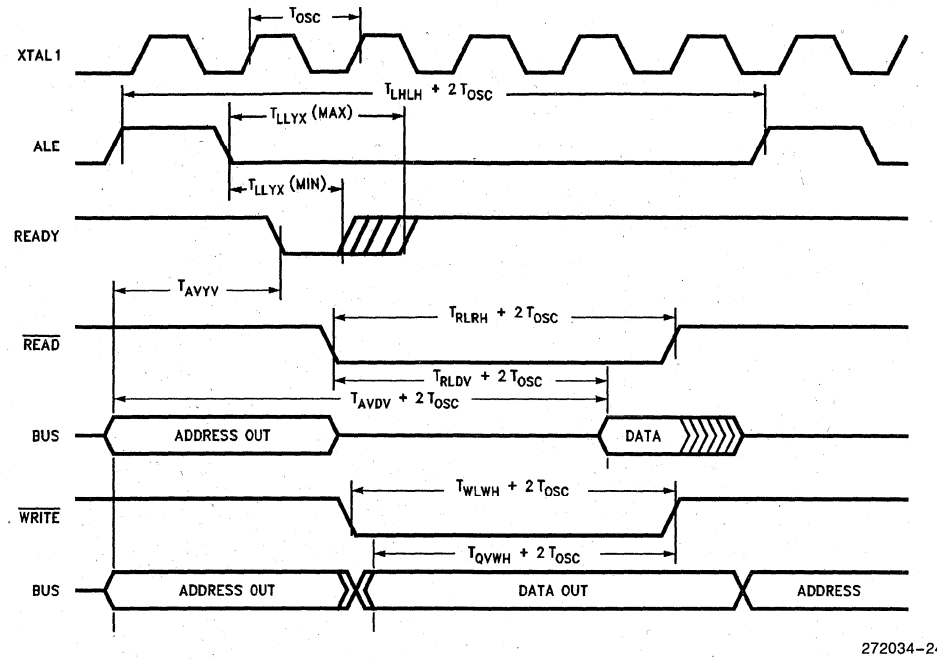
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **12 MHz**	3.5	12	MHz	(Note 1)
F_{XTAL}	Frequency on XTAL1 **16 MHz**	3.5	16	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$ **12 MHz**	83.3	286	ns	
T_{OSC}	$1/F_{XTAL}$ **16 MHz**	62.5	286	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 3)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	(Note 3)
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 15	T_{OSC} + 10	ns	(Note 2)
T_{WHBX}	INST Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{LLBX}	INST Hold after ALE Rising Edge	T_{OSC} − 10		ns	
T_{RHBX}	INST Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:
1. Testing performed at 3.5 MHz. However, the part is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. When using wait states, add 2 T_{OSC} × n, where n = number of wait states.

System Bus Timings



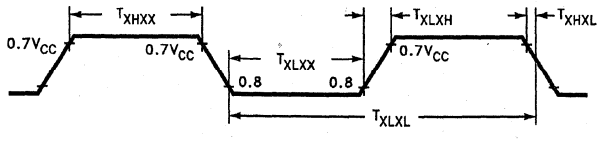
READY Timings (One Wait State)



EXTERNAL CLOCK DRIVE

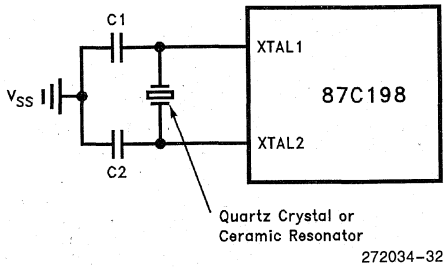
Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency **12 MHz**	3.5	12.0	MHz
$1/T_{XLXL}$	Oscillator Frequency **16 MHz**	3.5	16.0	MHz
T_{XLXL}	Oscillator Period **12 MHz**	83.3	286	ns
T_{XLXL}	Oscillator Period **16 MHz**	62.5	286	ns
T_{XHXX}	High Time	21.25		ns
T_{XLXX}	Low Time	21.25		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

EXTERNAL CRYSTAL CONNECTIONS



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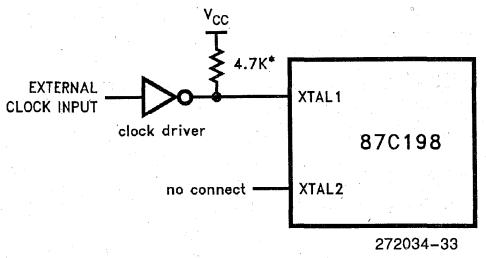
NOTE:
Keep oscillator components close to chip and use short direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators consult manufacturer for recommended capacitor values.

EXTERNAL CLOCK CONNECTIONS



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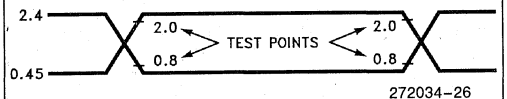
NOTE:
*Required if open collector TTL driver used. Not needed if CMOS driver is used.

AC TESTING INPUT, OUTPUT WAVEFORMS



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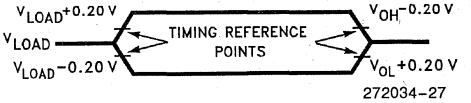
AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



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For Timing Purposes a Port Pin is no Longer Floating when a 200 mV change from Load Voltage Occurs and Begins to Float when a 200 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H - High
L - Low
V - Valid
X - No Longer Valid
Z - Floating

Signals:

A - Address
D - DATA IN
L - ALE/$\overline{\text{ADV}}$
Q - DATA OUT
R - $\overline{\text{RD}}$
W - $\overline{\text{WR}}$
X - XTAL1
Y - READY

10-BIT AID CHARACTERISTICS

At a clock speed of 6 MHz or less, the clock prescaler should be disabled. This is accomplished by setting IOC2.4 = 1.

At higher frequencies (greater than 6 MHz) the clock prescaler should be turned on (IOC2.4 = 0) to allow the comparator to settle.

The table below shows two different clock speeds and their corresponding A/D conversion and sample times.

State times are calculated as follows:

$$\text{state time} = \frac{2}{f_{XTAL1}}$$

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

See the MCS-96 A/D Converter Quick Reference for definition of A/D terms.

Example Sample and Conversion Times

AID Clock Prescaler	Clock Speed (MHz)	Sample Time (States)	Sample Time at Clock Speed (μs)	Conversion Time (States)	Conversion Time at Clock Speed (μs)
IOC2.4=0 → ON	16	15	1.875	156.5	19.6
IOC2.4=1 → OFF	6	8	2.667	89.5	29.8

A/D CONVERTER SPECIFICATIONS

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ±0.50			LSBs	
Zero Offset Error	−0.25 ±0.50			LSBs	
Non-Linearity Error	1.5 ±2.5	0	±3	LSBs	
Differential Non-Linearity Error		>−1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
DC Input Leakage		0	3.0	μA	
Sample Time: Prescaler On Prescaler Off	15 8			States States	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.

EPROM SPECIFICATIONS

EPROM PROGRAMMING OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}, V_{PD}, V_{REF}(1)	Supply Voltages during Programming	4.5	5.5	V
V_{EA}	Programming Mode Supply Voltage	12.50	13.0	V(2)
V_{PP}	EPROM Programming Supply Voltage	12.50	13.0	V(2)
V_{SS}, ANGND(3)	Digital and Analog Ground	0	0	V
F_{OSC}	Oscillator Frequency **16 MHz**	6.0	16.0	MHz

NOTES:
1. V_{CC}, V_{PD} and V_{REF} should nominally be at the same voltage during programming.
2. V_{EA} and V_{PP} must never exceed the maximum voltage for any amount of time or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same voltage (0V) during programming.

AC EPROM PROGRAMMING CHARACTERISTICS

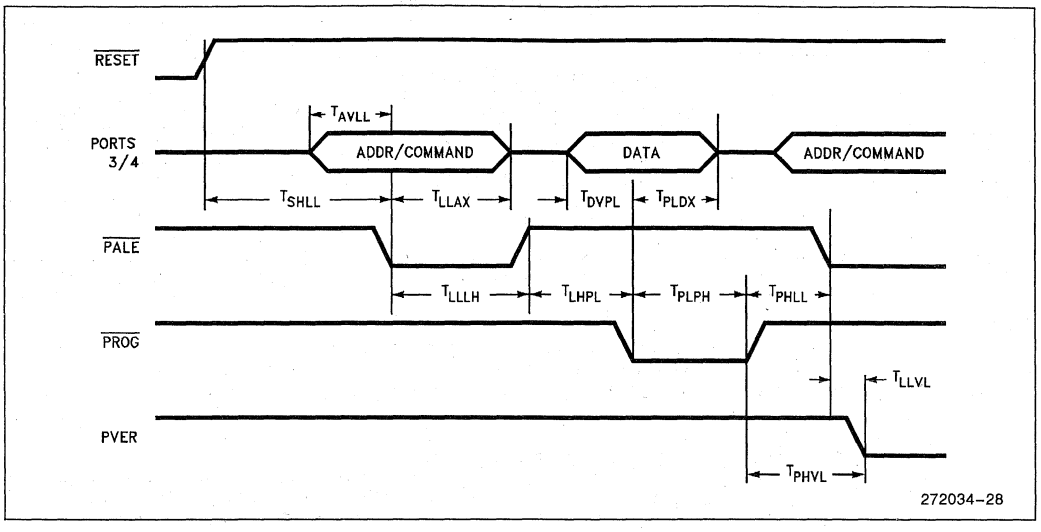
Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	40		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	50		T_{OSC}
T_{LLVL}	$\overline{PALE}$ Low to PVER Low		60	T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width	40		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	120		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	120		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	40		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to PVER Low		90	T_{OSC}

DC EPROM PROGRAMMING CHARACTERISTICS

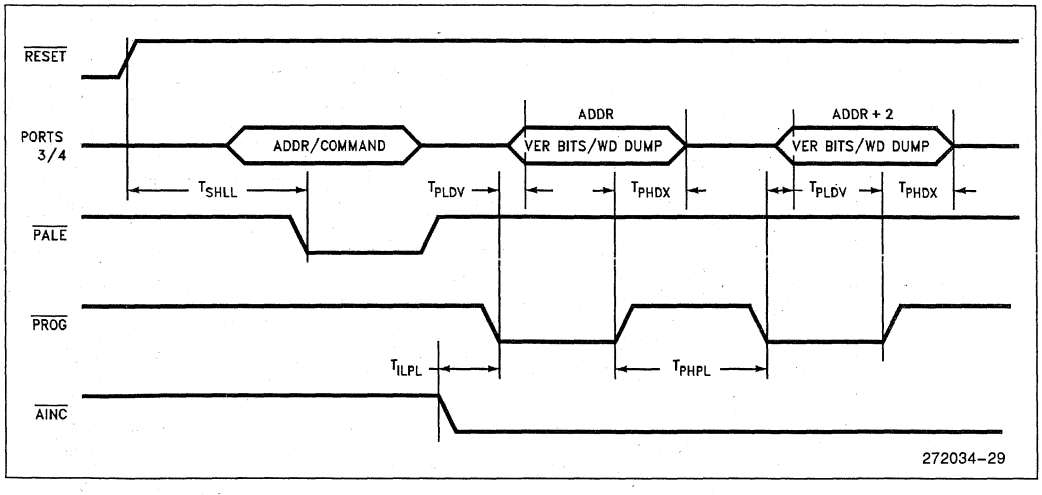
Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

EPROM PROGRAMMING WAVEFORMS

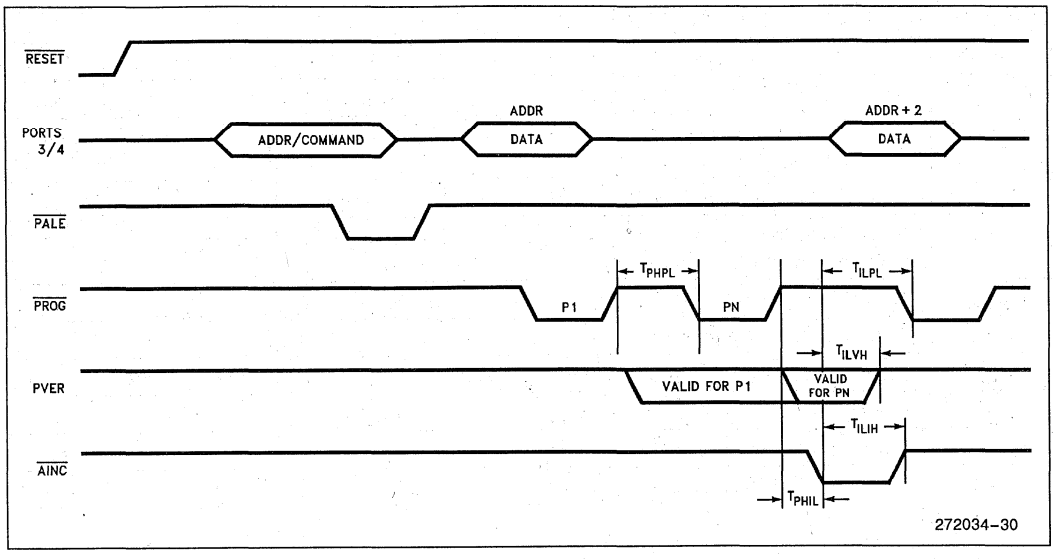
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



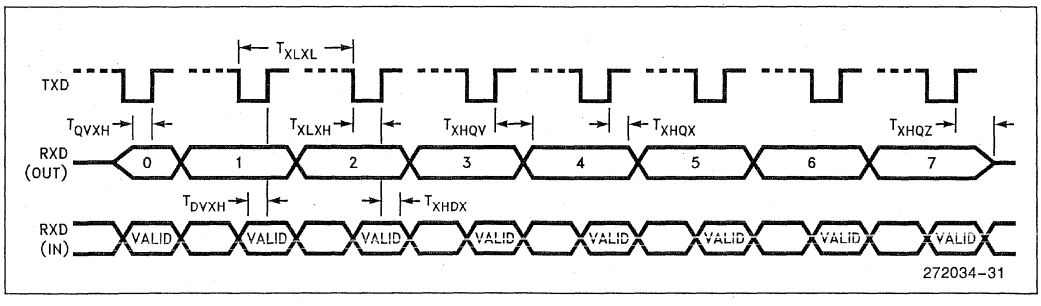
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} + 50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		2 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



FUNCTIONAL DEVIATIONS

Devices marked with an "E", "F", or "G" have the following errata.

1. HIGH SPEED INPUTS

The High Speed Input (HSI) has three deviations from the specifications.

NOTE:
"Events" are defined as one or more pin transitions. "Entries" are defined as the recording of one or more events.

A. The resolution is nine states instead of eight states. Events occurring on the same pin more frequently than once every nine states may be lost.

B. A mismatch between the nine state HSI resolution and the eight state hardware timer causes one time-tag value to be skipped every nine timer counts. Events may receive a time-tag one count later than expected.

C. If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register, leaving the FIFO empty again. The next event that occurs will be the first event loaded into the empty FIFO. If the first two events into an empty FIFO (not counting the Holding Register) occur coincident with each other, both are recorded as one entry with one time-tag. If the second event occurs within 9 states after the first, the events will be entered separately with time-tags at least one count apart. If the second event enters the FIFO coincident with the "skipped" time-tag situation (see B above) the time-tags will be at least two counts apart.

2. CMPL with R0

Using CMPL with register 0 can set incorrect flags. Don't use register 0 with the compare long instruction. Use another long word register and set it equal to zero. See Techbit MC0692.

REVISION HISTORY

This data sheet (272034-003) is valid for devices marked with an "E", "F", or "G" at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet and the previous version (-002).

1. This data sheet added the ROMless and ROM devices 80C198 and 83C198 respectively.
2. The description of the A/D converter prescalar bit was improved.

8XC196KC/8XC196KC20 COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

87C196KC—16 Kbytes of On-Chip OTPROM
83C196KC—16 Kbytes ROM
80C196KC—ROMless

- 16 and 20 MHz Available
- 488 Byte Register RAM
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- Peripheral Transaction Server
- 1.4 μs 16 x 16 Multiply (20 MHz)
- 2.4 μs 32/16 Divide (20 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Extended Temperature Available
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- 3 Pulse-Width-Modulated Outputs
- Four 16-Bit Software Timers
- 8- or 10-Bit A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol
- OTPROM One-Time Programmable Version

The 80C196KC 16-bit microcontroller is a high performance member of the MCS® 96 microcontroller family. The 80C196KC is an enhanced 80C196KB device with 488 bytes RAM, 16 and 20 MHz operation and an optional 16 Kbytes of ROM/OTPROM. Intel's CHMOS III process provides a high performance processor along with low power consumption.

The 87C196KC is an 80C196KC with 16 Kbytes on-chip OTPROM. The 83C196KC is an 80C196KC with 16 Kbytes factory programmed ROM. In this document, the 80C196KC will refer to all products unless otherwise stated.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended (Express) temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

See the Packaging information for extended temperature designators.

November 1994

Order Number: 270942-005

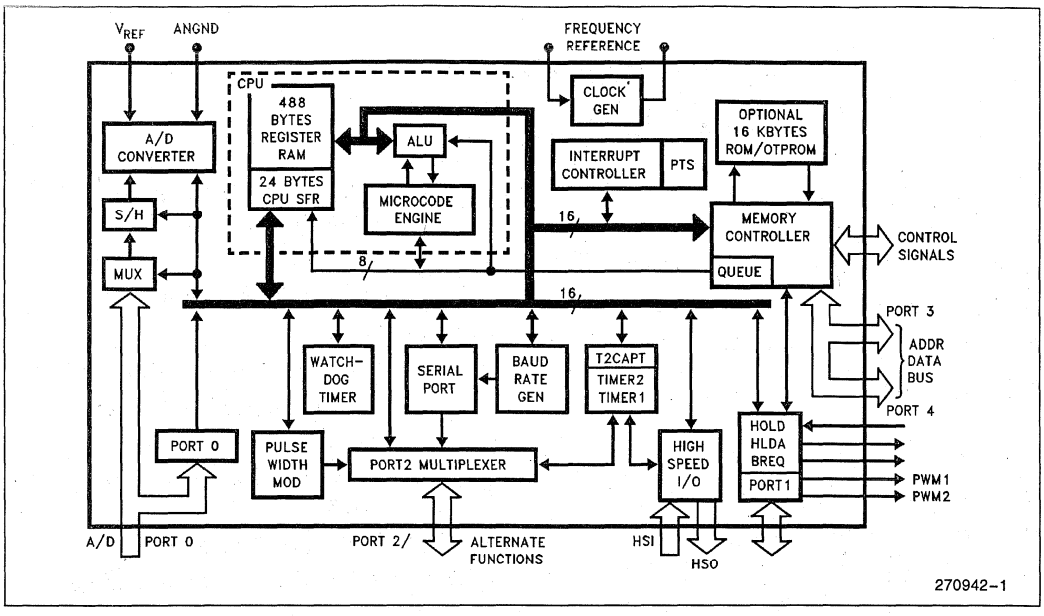
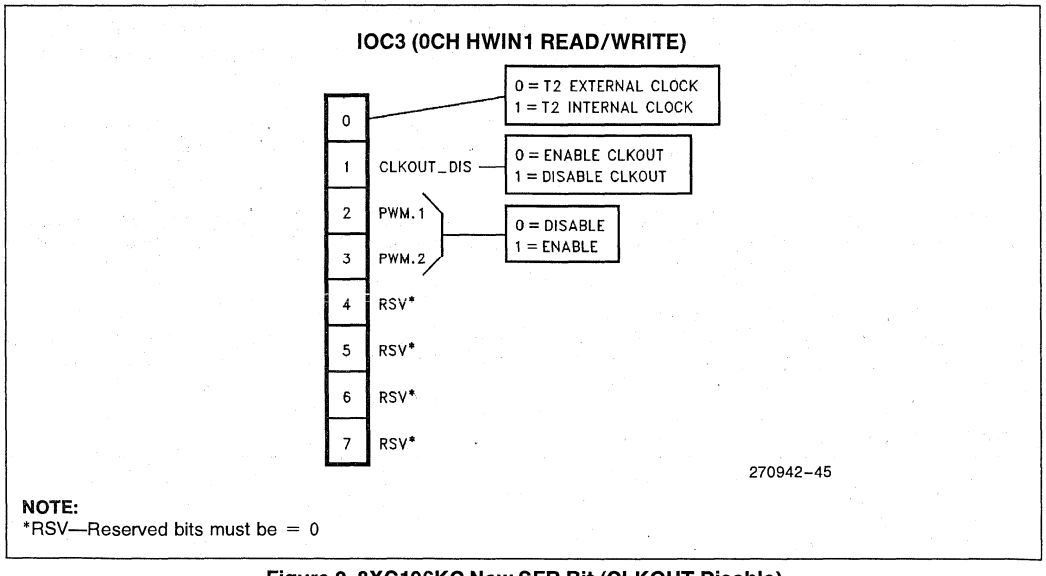


Figure 1. 8XC196KC Block Diagram

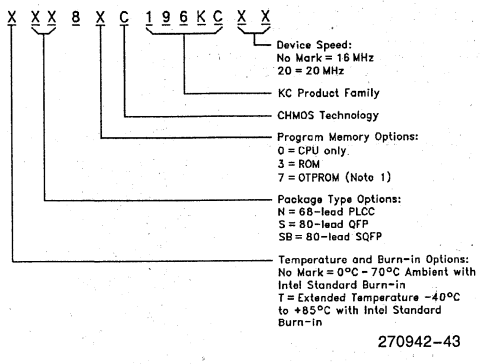


NOTE:
*RSV—Reserved bits must be = 0

Figure 2. 8XC196KC New SFR Bit (CLKOUT Disable)

PROCESS INFORMATION

This device is manufactured on PX29.5 or PX29.9, a CHMOS III process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196KC is 68-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC196KC Family Nomenclature

Table 1. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	55°C/W	16°C/W
SQFP	TBD	TBD

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 2. 8XC196KC Memory Map

Description	Address
External Memory or I/O	0FFFFH 06000H
Internal ROM/OTPROM or External Memory (Determined by $\overline{EA}$)	5FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/OTPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4	1FFFH 1FFEH
External Memory	1FFDH 0200H
488 Bytes Register RAM (Note 1)	01FFH 0018H
CPU SFR's (Notes 1, 3, 4)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 01FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC User's manual for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

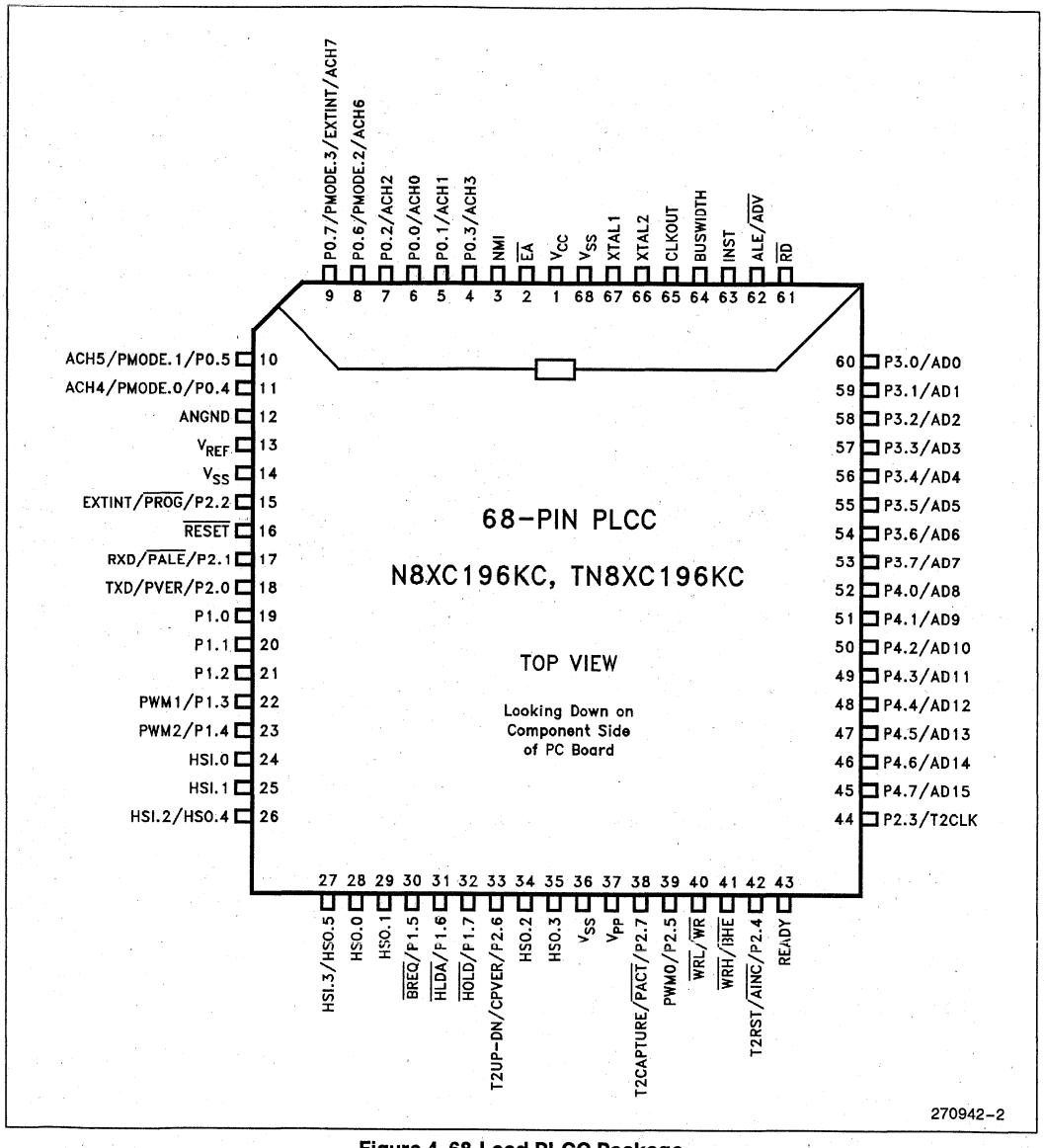


Figure 4. 68-Lead PLCC Package

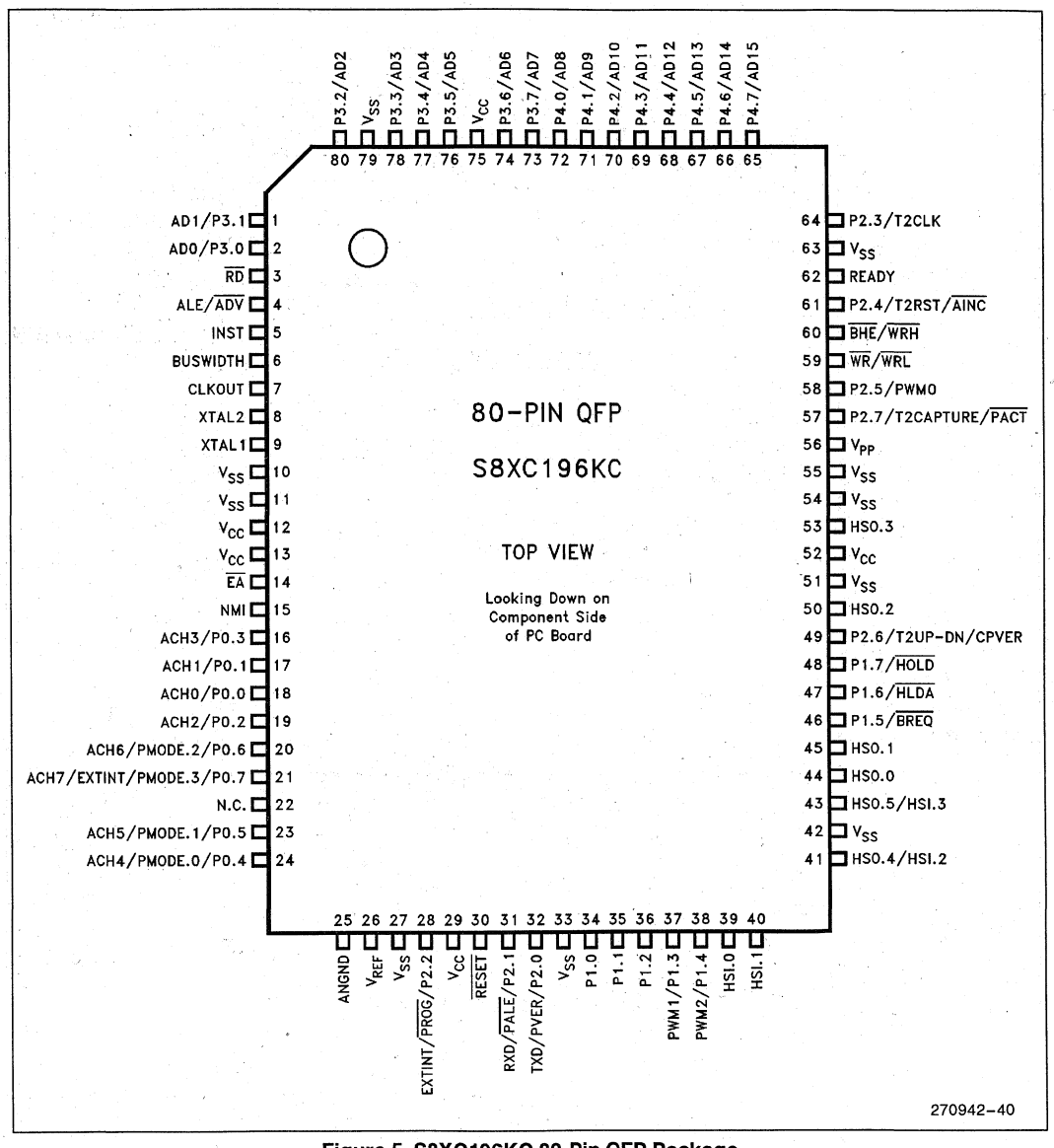


Figure 5. S8XC196KC 80-Pin QFP Package

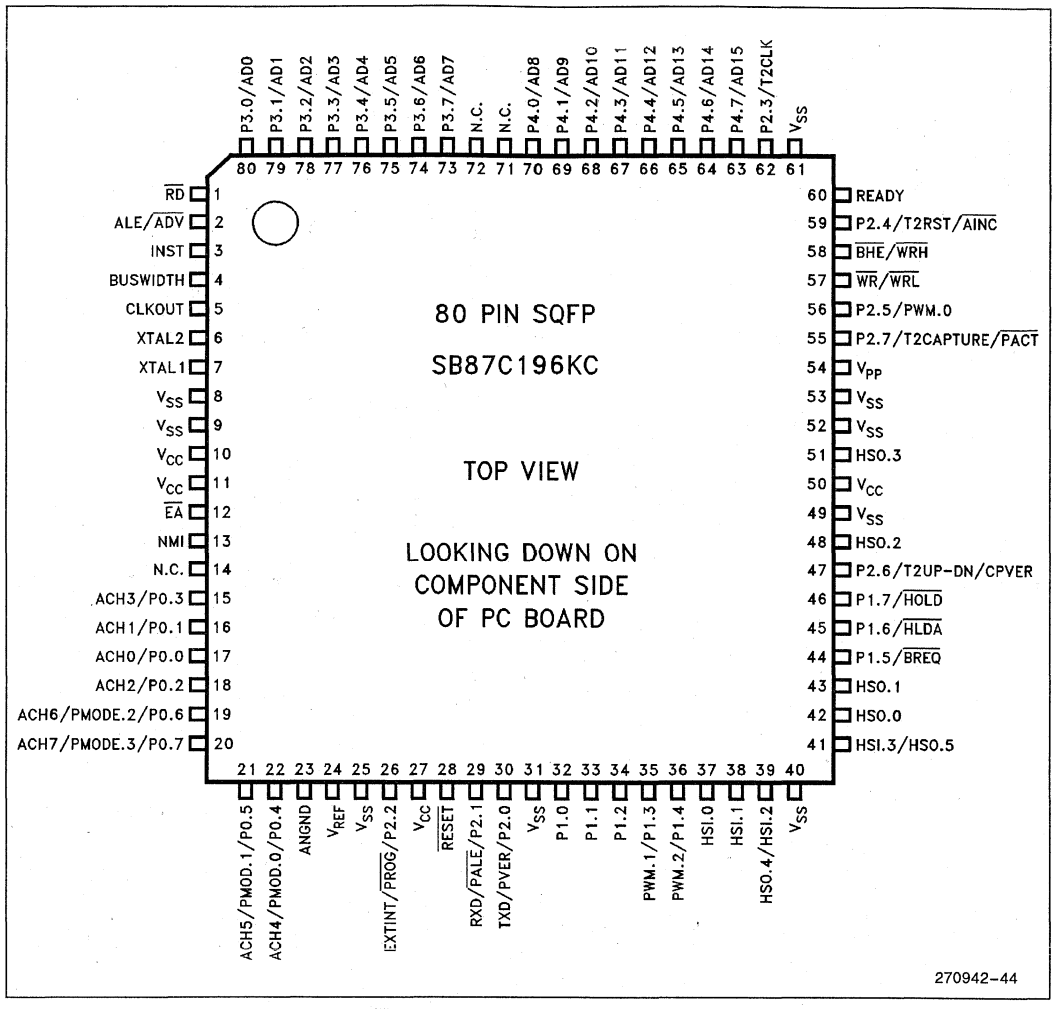


Figure 6. 80-Pin SQFP Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. This pin also supplies the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{\text{RESET}}$	Reset input and open drain output.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal high causes memory accesses to locations 2000H through 5FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal to low causes accesses to those locations to be directed to off-chip memory. Also used to enter programming mode.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being written. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KC. Pins 2.6 and 2.7 are quasi-bidirectional.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
CPVER	Cummulative Program Output Verification. Pin is high if all locations have programmed correctly since entering a programming mode.
$\overline{\text{PALE}}$	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programmig Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
$\overline{\text{AINC}}$	Auto Increment. Active low input signal indicates that the auto increment mode is enabled. Auto Increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V(1)
Voltage from $\overline{EA}$ or
V_{PP} to V_{SS} or ANGND ..... +13.00V
Power Dissipation ..... 1.5W(2)

NOTE:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This is a production data sheet. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature Under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} − 0.4	V_{SS} + 0.4	V(1)
F_{OSC}	Oscillator Frequency **(8XC196KC)**	8	16	MHz
F_{OSC}	Oscillator Frequency **(8XC196KC20)**	8	20	MHz

NOTE:
1. ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Over Specified Operating Conditions)

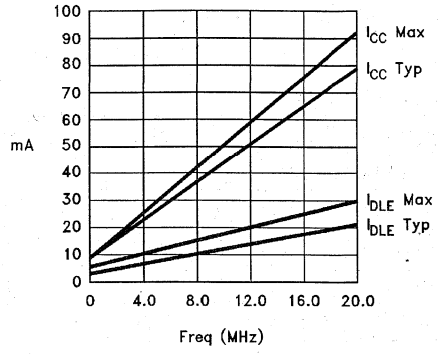
Symbol	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2		V_{CC} + 0.5	V	
V_{HYS}	Hysteresis on $\overline{RESET}$	300			mV	V_{CC} = 5.0V
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)			0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA

DC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10\ \mu A$ $I_{OH} = -30\ \mu A$ $I_{OH} = -60\ \mu A$
I_{OH1}	Logical 1 Output Current in Reset. on P2.0. Do not exceed this or device may enter test modes.	−0.8			mA	$V_{IH} = V_{CC} - 1.5V$
I_{IL2}	Logical 0 Input Current in Reset on P2.0. Maximum current that must be sunk by external device to ensure test mode entry.			TBD	mA	$V_{IN} = 0.45V$
I_{IH1}	Logical 1 Input Current. Maximum current that external device must source to initiate NMI.			+200	μA	$V_{IN} = V_{CC} = 2.4V$
I_{LI}	Input Leakage Current (Std. Inputs)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	$V_{IN} = 0.45V$
I_{IL1}	Ports 3 and 4 in Reset			−70	μA	$V_{IN} = 0.45V$
I_{CC}	Active Mode Current in Reset **(8XC196KC)**		65	75	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{CC}	Active Mode Current in Reset **(8XC196KC20)**		80	92	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current **(8XC196KC)**		17	25	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current **(8XC196KC20)**		21	30	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current		8	15	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	$V_{CC} = 5.5V, V_{IN} = 4.0V$
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
1. All pins except RESET and XTAL1.
2. Violating these specifications in Reset may cause the part to enter test modes.
3. Commercial specifications apply to express parts except where noted.
4. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
5. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
6. Standard Inputs include HSI pins, READY, BUSWIDTH, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
7. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below $V_{CC} - 0.7V$:
   - I_{OL} on Output pins: 10 mA
   - I_{OH} on quasi-bidirectional pins: self limiting
   - I_{OH} on Standard Output pins: 10 mA
8. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
9. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA



I_{CC} Max = 4.13 × Frequency + 9 mA
I_{CC} Typ = 3.50 × Frequency + 9 mA
I_{IDLE} Max = 1.25 × Frequency + 5 mA
I_{IDLE} Typ = 0.88 × Frequency + 3 mA

NOTE:
Frequencies below 8 MHz are shown for reference only; no testing is performed.

Figure 7. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The system must meet these specifications to work with the 80C196KC:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 68	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	T_{OSC} − 15	2 T_{OSC} − 40	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} − 68	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 22	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 45	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

AC CHARACTERISTICS (Continued)

For user over specified operating conditions.

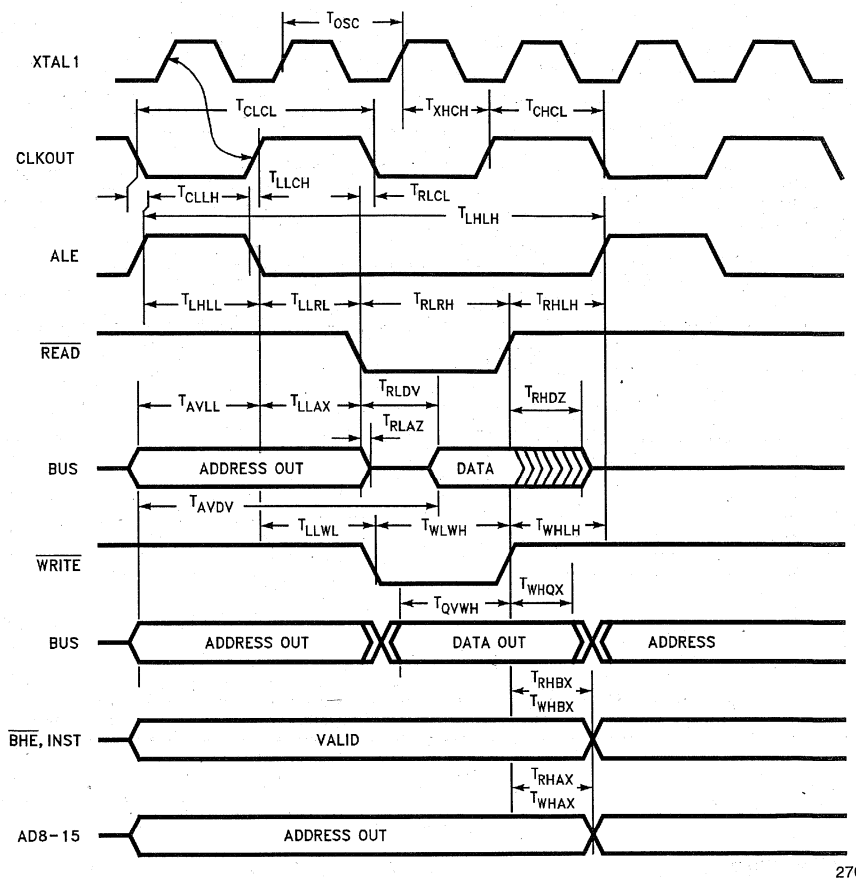
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

The 80C196KC will meet these specifications:

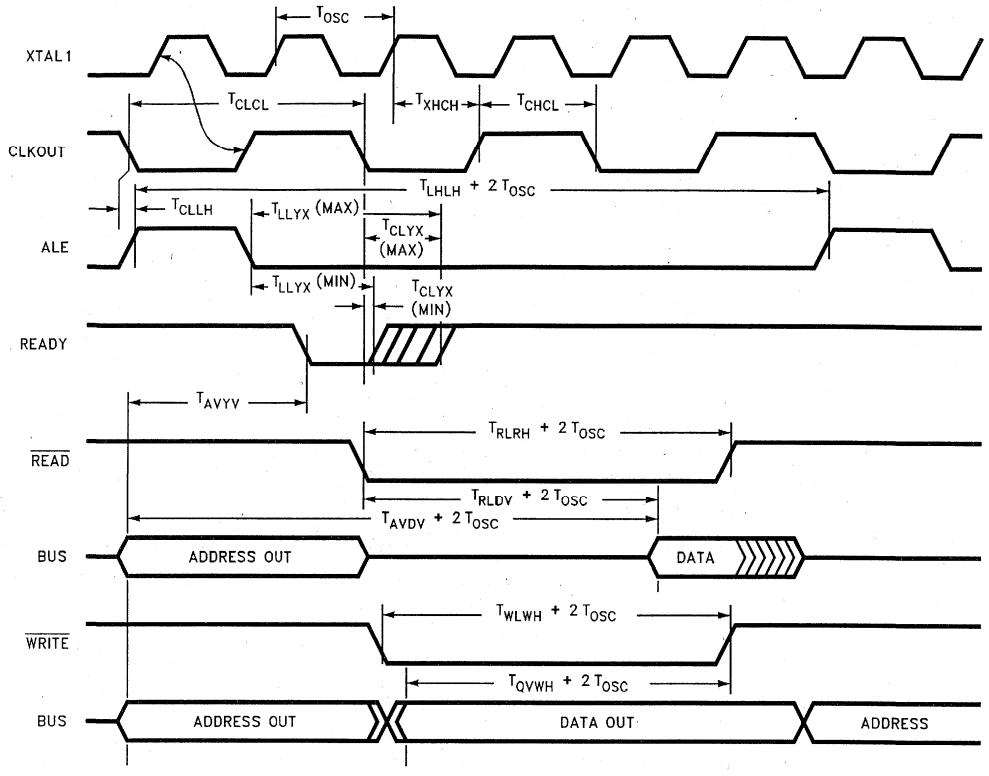
Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **(8XC196KC)**	8	16	MHz	(Note 1)
F_{XTAL}	Frequency on XTAL1 **(8XC196KC20)**	8	20	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$ **(8XC196KC)**	62.5	125	ns	
T_{OSC}	$1/F_{XTAL}$ **(8XC196KC20)**	50	125	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC}+15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	+15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 4)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC}+10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15			
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 35		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23			(Note 4)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 20		ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	T_{OSC} − 30		ns	(Note 3)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	T_{OSC} − 25		ns	(Note 3)

NOTES:
1. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

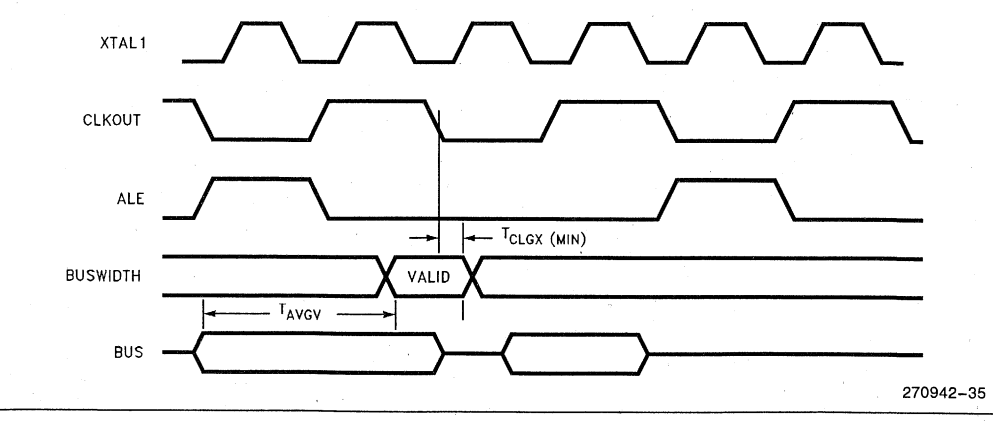
System Bus Timings



READY Timings (One Wait State)



Buswidth Timings



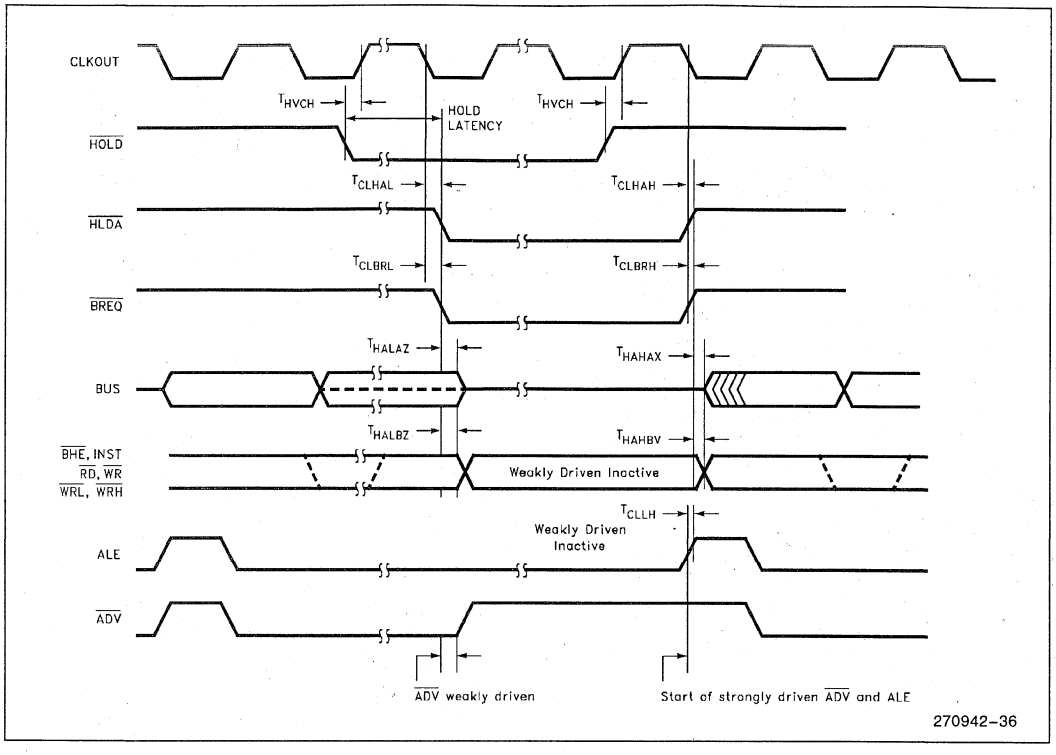
$\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	$\overline{\text{HOLD}}$ Setup	+55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to $\overline{\text{HLDA}}$ Low	−15	+15	ns	
T_{CLBRL}	CLKOUT Low to $\overline{\text{BREQ}}$ Low	−15	+15	ns	
T_{HALAZ}	$\overline{\text{HLDA}}$ Low to Address Float		+15	ns	
T_{HALBZ}	$\overline{\text{HLDA}}$ Low to $\overline{\text{BHE}}$, INST, $\overline{\text{RD}}$, $\overline{\text{WR}}$ Weakly Driven		+20	ns	
T_{CLHAH}	CLKOUT Low to $\overline{\text{HLDA}}$ High	−15	+15	ns	
T_{CLBRH}	CLKOUT Low to $\overline{\text{BREQ}}$ High	−15	+15	ns	
T_{HAHAX}	$\overline{\text{HLDA}}$ High to Address No Longer Float	−15		ns	
T_{HAHBV}	$\overline{\text{HLDA}}$ High to $\overline{\text{BHE}}$, INST, $\overline{\text{RD}}$, $\overline{\text{WR}}$ Valid	−10	+15	ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	+15	ns	

NOTE:
1. To guarantee recognition at next clock.

DC SPECIFICATIONS IN HOLD

Description	Min	Max	Units
Weak Pullups on $\overline{\text{ADV}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WRL}}$, $\overline{\text{BHE}}$	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4



Maximum Hold Latency

Bus Cycle Type	
Internal Execution	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

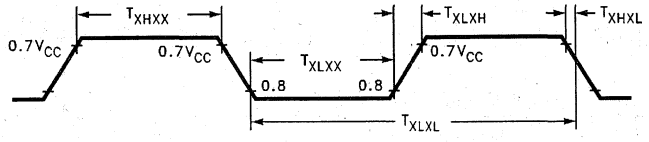
EXTERNAL CLOCK DRIVE (8XC196KC)

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	20		ns
T_{XLXX}	Low Time	20		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE (8XC196KC20)

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	20.0	MHz
T_{XLXL}	Oscillator Period	50	125	ns
T_{XHXX}	High Time	17		ns
T_{XLXX}	Low Time	17		ns
T_{XLXH}	Rise Time		8	ns
T_{XHXL}	Fall Time		8	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



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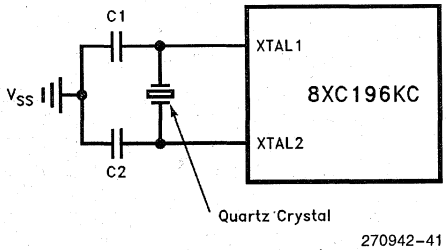
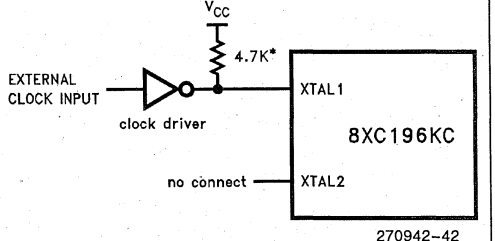
EXTERNAL CRYSTAL CONNECTIONS



270942-41

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = C2 ≈ 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

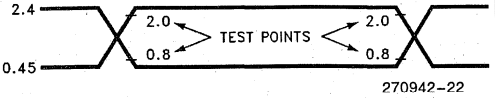
EXTERNAL CLOCK CONNECTIONS



270942-42

NOTE:
*Required if TTL driver used.
Not needed if CMOS driver is used.

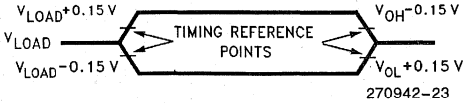
AC TESTING INPUT, OUTPUT WAVEFORMS



270942-22

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



270942-23

For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs; I_{OL}/I_{OH} = ±15 mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
BR— $\overline{BREQ}$
R— $\overline{RD}$
W— $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X— XTAL1
Y— READY
Q— Data Out

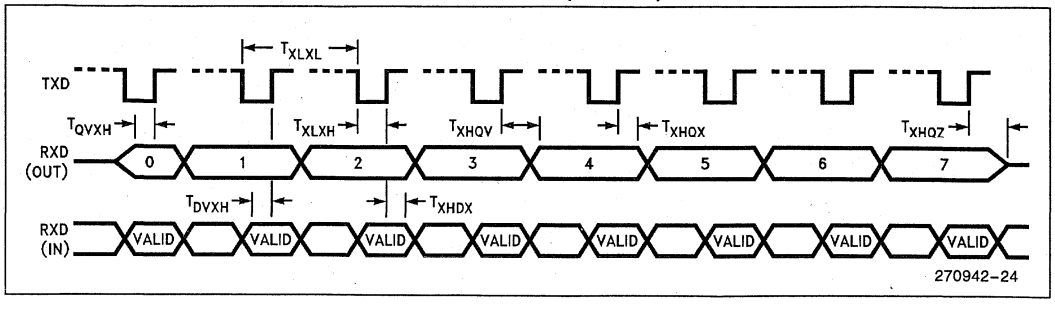
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} +50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} −50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)



A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	10	20	μs(1)
F_{OSC}	Oscillator Frequency **(8XC196KC)**	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency **(8XC196KC20)**	8.0	20.0	MHz

NOTE:
ANGND and V_{SS} should nominally be at the same potential, 0.00V.
1. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Non-Linearity	1.0 ± 2.0	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 2
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approxiimately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of all channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	7	20	μs(1)
F_{OSC}	Oscillator Frequency **(8XC196KC)**	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency **(8XC196KC20)**	8.0	20.0	MHz

NOTE:
ANGND and V_{SS} should nominally be at the same potential, 0.00V.
1. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±1	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±1	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ωs	4
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of all channels being converted.
7. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS DURING PROGRAMMING

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency During Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency During Run-Time Programming **(8XC196KC)**	6.0	16.0	MHz
F_{OSC}	Oscillator Frequency During Run-Time Programming **(8XC196KC20)**	6.0	20.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm. See user's manual for further information.

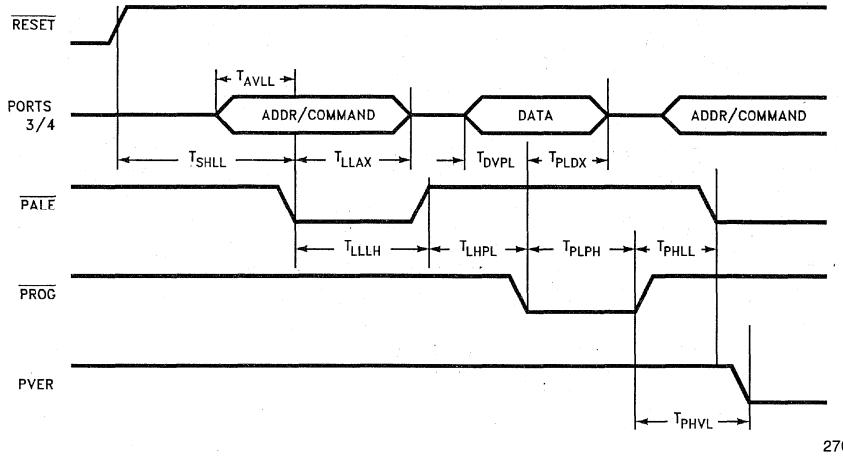
DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

EPROM PROGRAMMING WAVEFORMS

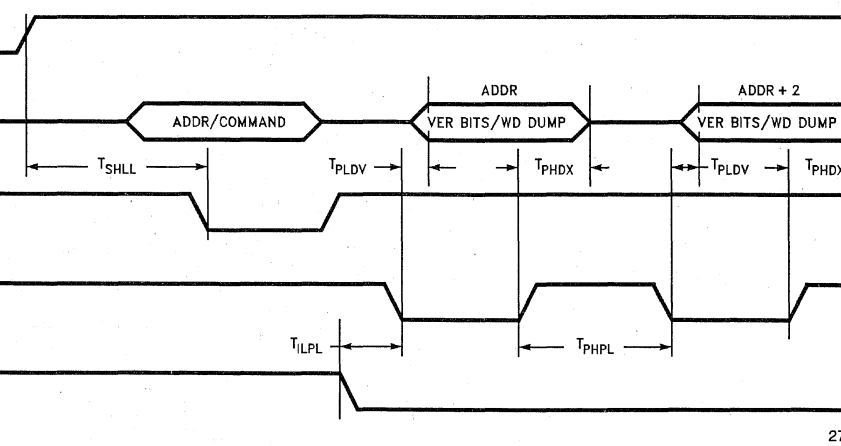
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



270942-27

NOTE:
P3.0 must be high ("1")

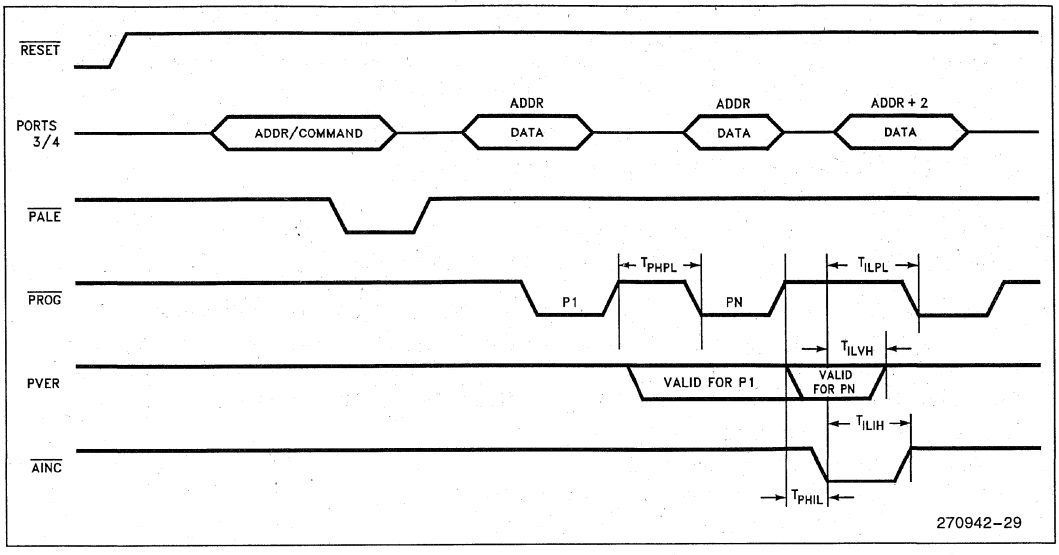
SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



270942-28

NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



8XC196KB TO 8XC196KC DESIGN CONSIDERATIONS

1. Memory Map. The 8XC196KC has 512 bytes of RAM/SFRs and an optional 16K of ROM/OTPROM. The extra 256 bytes of RAM will reside in locations 100H–1FFH and the extra 8K of ROM/OTPROM will reside in locations 4000H–5FFFH. These locations are external memory on the 8XC196KB.
2. The CDE pin on the KB has become a V_{SS} pin on the KC to support 16/20 MHz operation.
3. EPROM programming. The 8XC196KC has a different programming algorithm to support 16K of on-board memory. When performing Run-Time Programming, use the section of code in the 8XC196KC User's Guide.
4. ONCE Mode Entry. The ONCE mode is entered on the 8XC196KC by driving the TXD pin low on the rising edge of RESET. The TXD pin is held high by a pullup that is specified by I_{OH1}. This Pullup must not be overridden or the 8XC196KC will enter the ONCE mode.
5. During the bus HOLD state, the 8XC196KC weakly holds $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$ and INST in their inactive states. The 8XC196KB only holds ALE in its inactive state.
6. A RESET pulse from the 8XC196KC is 16 states rather than 4 states as on the 8XC196KB (i.e., a watchdog timer overflow). This provides a longer RESET pulse for other devices in the system.

8XC196KC ERRATA

1. **Missed EXTINT on P0.7.**

   The 80C196KC20 could possibly miss an EXTINT on P0.7. See techbit MC0893.

2. HSI_MODE divide-by-eight.

   See Faxback #2192.

3. IPD hump.

   See Faxback #2311.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a "H", "L" or "M" at the end of the topside tracking number. The topside tracking number consists of nine characters and is the second line on the top side of the device. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are differences between the 270942-004 and 270942-005 datasheets:

1. Removed "Word Addressable Only" from Port 3 and 4 in Table 2.
2. Renamed PVAL to CPVER.
3. Removed T_{LLYV} and T_{LLGV} from the waveform diagrams.
4. Added HSI_MODE divide-by-eight and IPD hump to 8XC196KC errata.

The following are important differences between the 270942-002 and 270942-004 data sheets:

1. NMI during PTS, QBD port glitch and Divide HOLD/READY erratas were fixed and have been removed from the data sheet. The HSI errata is also removed as this is now considered normal operation.
2. Combined 16 and 20 MHz data sheets. Data sheet 270924-001 (20 MHz) is now obsolete.
3. Added 80-lead SQFP package pinout.
4. Added documentation for CLKOUT disable bit.
5. θ_{JA} for QFP package was changed to 55°C/W from 42°C/W.
6. θ_{JC} for QFP package was changed to 16°C/W from TBD°C/W.
7. T_{SAM} (MIN) in 10-bit mode was changed to 1.0 μs from 3.0 μs.
8. T_{SAM} (MIN) in 8-bit mode was changed to 1.0 μs from 2.0 μs.
9. I_{IL1} specification for port 2.0 was renamed I_{IL2}.
10. I_{IL2} (MAX) is changed to TBD from − 6 mA.
11. I_{IH1} (MAX) is changed to +200 μA from +100 μA.
12. I_{IH1} test condition changes to V_{IN} = 2.4V from V_{IN} = 5.5V.
13. V_{HYS} is changed to 300 mV from 150 mV.
14. I_{CC} (TYP) at 16 MHz is changed to 65 mA from 50 mA.
15. I_{CC} (MAX) at 16 MHz is changed to 75 mA from 70 mA.
16. I_{CC} (TYP) at 20 MHz is changed to 80 mA from 60 mA.
17. I_{CC} (MAX) at 20 MHz is changed to 92 mA from 86 mA.
18. I_{IDLE} (TYP) at 16 MHz is changed to 17 mA from 15 mA.
19. I_{IDLE} (MAX) at 16 MHz is changed to 25 mA from 30 mA.
20. I_{IDLE} (TYP) at 20 MHz is changed to 21 mA from 15 mA.
21. I_{IDLE} (MAX) at 20 MHz is changed to 30 mA from 35 mA.
22. I_{PD} (TYP) at 16 MHz is changed to 8 μA from 15 μA.
23. I_{PD} (MAX) at 16 MHz is changed to 15 μA from TBD.
24. I_{PD} (TYP) at 20 MHz is changed to 8 μA from 18 μA.
25. I_{PD} (MAX) at 20 MHz is changed to 15 μA from TBD.
26. T_{CLDV} (MAX) is changed to T_{OSC} −45 ns from T_{OSC} − 50 ns.
27. T_{LLAX} (MIN) is changed to T_{OSC} −35 ns from T_{OSC} − 40 ns.
28. T_{CHWH} (MIN) is changed to −5 ns from −10 ns.
29. T_{RHAX} (MIN) is changed to T_{OSC} − 25 ns from T_{OSC} − 30 ns.
30. T_{HALAZ} (MAX) is changed to +15 ns from +10 ns.
31. T_{HALBZ} (MAX) is changed to +20 ns from +15 ns.

32. T_{HAHBV} (MAX) is now specified at +15 ns, was formerly unspecified.
33. The T_{LLYV} and T_{LLGV} specifications were removed. These specifications are not required in high-speed systems designs.
34. Added EXTINT, P0.7 errata to Errata section.

The following are the important differences between the -001 and -002 versions of data sheet 270942.

1. Express and Commercial devices are combined into one data sheet. The Express only data sheet 270794-001 is obsolete.
2. Removed KB/KC feature set differences, pin definition table, and SFR locations and bitmaps.
3. Added programming pin function to package drawings and pin descriptions.
4. Changed absolute maximum temperature under bias from 0°C to +70°C to −55°C to +125°C.
5. Replaced V_{OH2} specification with I_{OH1} and I_{IL1} specifications.
6. Added I_{IH1} specification for NMI pulldown resistors.
7. Added maximum hold latency table.
8. Added external oscillator and external clock circuit drawings.
9. Changed Clock Drive T_{XHXX} and T_{XLXX} Min spec to 20 ns.
10. Fixed Serial Port T_{XLXH} specification.
11. Added 8- and 10-bit mode A/D operating conditions tables.
12. Specified operating range for sample and convert times.
13. Added specification for voltage on analog input pin.
14. Put operating conditions for EPROM programming into tabular format.

8XC196KD/8XC196KD20
COMMERCIAL CHMOS MICROCONTROLLER

87C196KD—32 Kbytes of On-Chip OTPROM
83C196KD—32 Kbytes of ROM

- 16 MHz and 20 MHz Available
- 1000 Byte Register RAM
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- Peripheral Transaction Server
- 1.4 μs 16 x 16 Multiply (20 MHz)
- 2.4 μs 32/16 Divide (20 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- 3 Pulse-Width-Modulated Outputs
- Four 16-Bit Software Timers
- 8- or 10-Bit A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol
- OTP One-Time Programmable Version

The 8XC196KD 16-bit microcontroller is a high performance member of the MCS® 96 microcontroller family. The 8XC196KD is an enhanced 80C196KC device with 1000 bytes RAM, 16 MHz operation and an optional 32 Kbytes of ROM/EPROM. Intel's CHMOS III process provides a high performance processor along with low power consumption.

The 8XC196KD has a maximum guaranteed frequency of 16 MHz. The 8XC196KD20 has a maximum guaranteed frequency of 20 MHz. Unless otherwise noted, all references to the 8XC196KD also refer to the 8XC196KD20.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

November 1994

Order Number: 272145-003

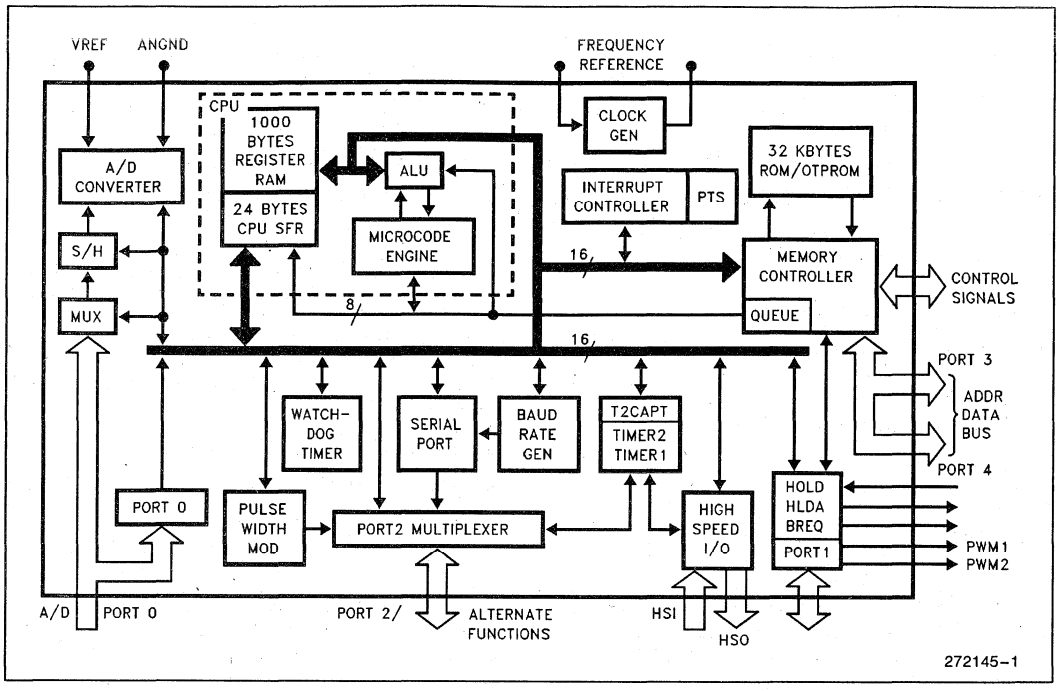
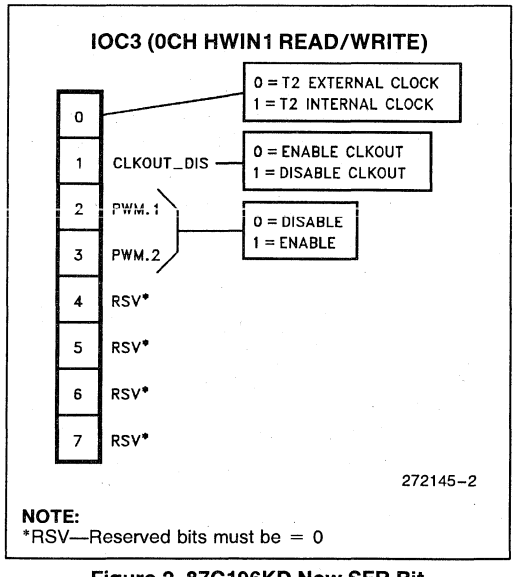


Figure 1. 8XC196KD Block Diagram

87C196KD ENHANCED FEATURE SET OVER THE 87C196KC

1. The 87C196KD has twice the RAM and twice the OTPROM space of the 87C196KC.
2. The vertical windowing scheme has been extended to allow all 1000 bytes of register RAM to be windowed into the lower register file.



NOTE:
*RSV—Reserved bits must be = 0

Figure 2. 87C196KD New SFR Bit (CLKOUT Disable)

8XC196KD VERTICAL WINDOWING MAP

Table 1. 128-Byte Windows

Address to Remap	Device Series	WSR Contents
0380H	KD	X001 0111B = 17H
0300H	KD	X001 0110B = 16H
0280H	KD	X001 0101B = 15H
0200H	KD	X001 0100B = 14H
0180H	KC, KD	X001 0011B = 13H
0100H	KC, KD	X001 0010B = 12H
0080H	KC, KD	X001 0001B = 11H
0000H	KC, KD	X001 0000B = 10H

Window in Lower Register File: 80H–FFH

Table 2. 64-Byte Windows

Address to Remap	Device Series	WSR Contents
03C0H	KD	X010 1111B = 2FH
0380H	KD	X010 1110B = 2EH
0340H	KD	X010 1101B = 2DH
0300H	KD	X010 1100B = 2CH
02C0H	KD	X010 1011B = 2BH
0280H	KD	X010 1010B = 2AH
0240H	KD	X010 1001B = 29H
0200H	KD	X010 1000B = 28H
01C0H	KC, KD	X010 0111B = 27H
0180H	KC, KD	X010 0110B = 26H
0140H	KC, KD	X010 0101B = 25H
0100H	KC, KD	X010 0100B = 24H
00C0H	KC, KD	X010 0011B = 23H
0080H	KC, KD	X010 0010B = 22H
0040H	KC, KD	X010 0001B = 21H
0000H	KC, KD	X010 0000B = 20H

Window in Lower Register File: C0H–FFH

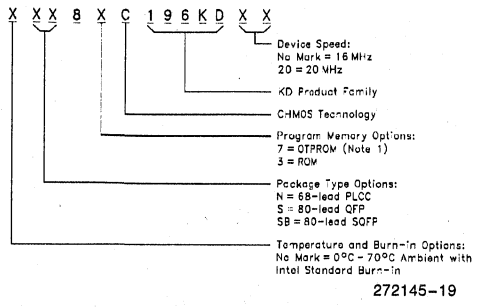
Table 3. 32-Byte Windows

Address to Remap	Device Series	WSR Contents
03E0H	KD	X101 1111B = 5FH
03C0H	KD	X101 1110B = 5EH
03A0H	KD	X101 1101B = 5DH
0380H	KD	X101 1100B = 5CH
0360H	KD	X101 1011B = 5BH
0340H	KD	X101 1010B = 5AH
0320H	KD	X101 1001B = 59H
0300H	KD	X101 1000B = 58H
02E0H	KD	X101 0111B = 57H
02C0H	KD	X101 0110B = 56H
02A0H	KD	X101 0101B = 55H
0280H	KD	X101 0100B = 54H
0260H	KD	X101 0011B = 53H
0240H	KD	X101 0010B = 52H
0220H	KD	X101 0001B = 51H
0200H	KD	X101 0000B = 50H
01E0H	KC, KD	X100 1111B = 4FH
01C0H	KC, KD	X100 1110B = 4EH
01A0H	KC, KD	X100 1101B = 4DH
0180H	KC, KD	X100 1100B = 4CH
0160H	KC, KD	X100 1011B = 4BH
0140H	KC, KD	X100 1010B = 4AH
0120H	KC, KD	X100 1001B = 49H
0100H	KC, KD	X100 1000B = 48H
00E0H	KC, KD	X100 0111B = 47H
00C0H	KC, KD	X100 0110B = 46H
00A0H	KC, KD	X100 0101B = 45H
0080H	KC, KD	X100 0100B = 44H
0060H	KC, KD	X100 0011B = 43H
0040H	KC, KD	X100 0010B = 42H
0020H	KC, KD	X100 0001B = 41H
0000H	KC, KD	X100 0000B = 40H

Window in Lower Register File: E0H–FFH

PROCESS INFORMATION

This device is manufactured on PX29.5 or PX29.9, a CHMOS III process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196KD20 is 68-Lead PLCC OTPROM, 20 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC196KD Family Nomenclature

Table 4. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W
SQFP	68°C/W	15.5°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 5. 8XC196KD Memory Map

Description	Address
External Memory or I/O	0FFFFH 0A000H
Internal ROM/OTPROM or External Memory (Determined by $\overline{EA}$)	9FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/OTPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4	1FFFH 1FFEH
External Memory	1FFDH 0400H
1000 Bytes Register RAM (Note 1)	03FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 03FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

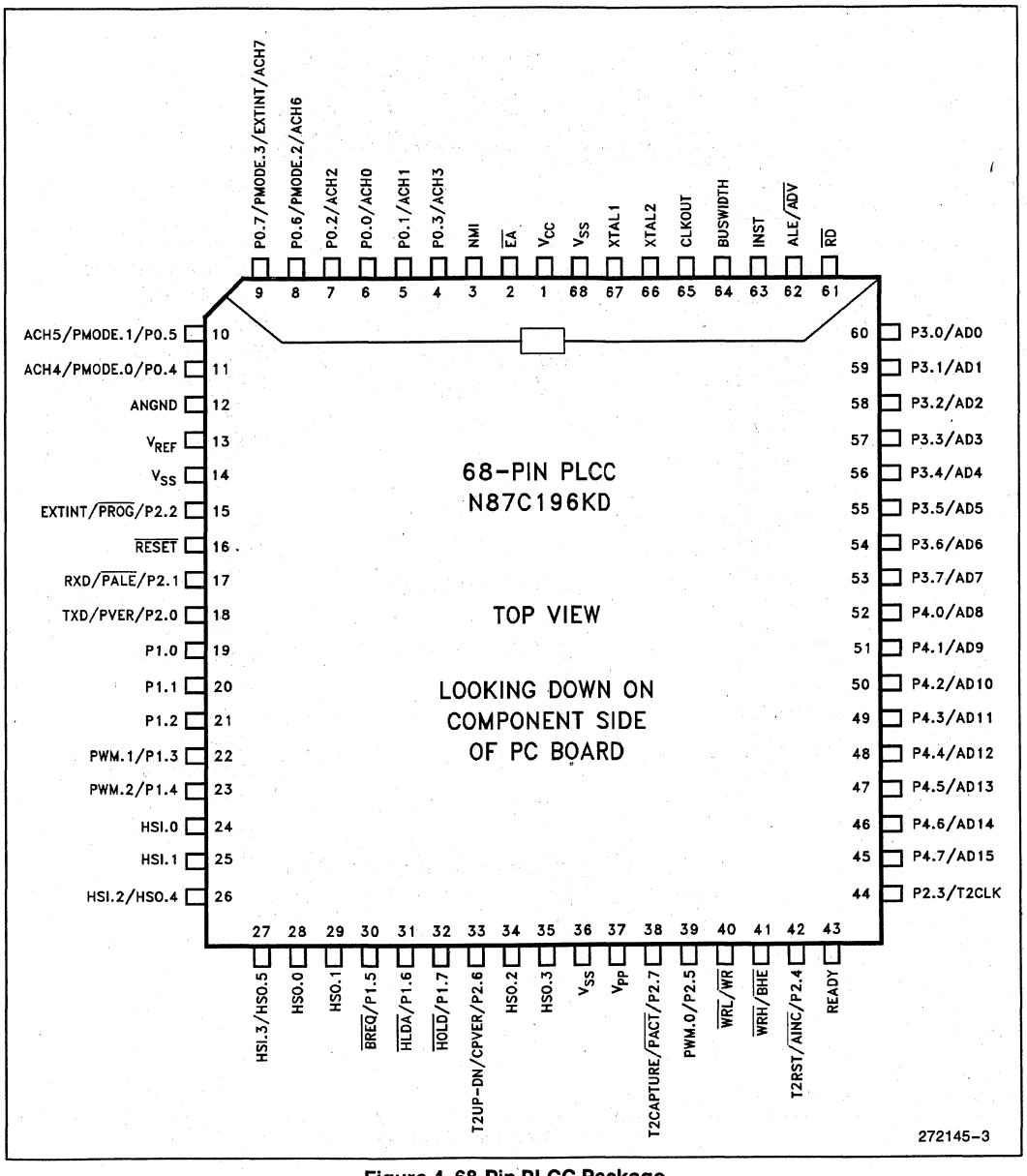
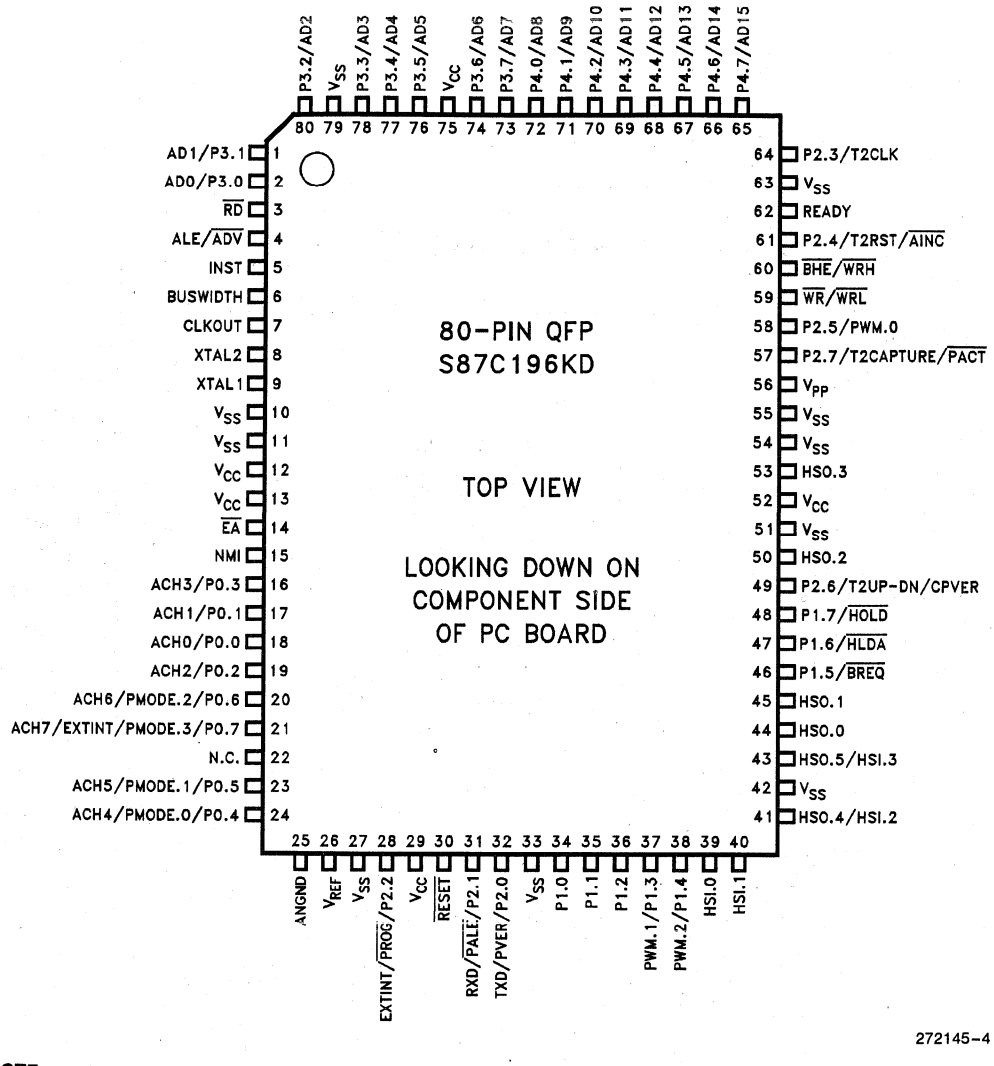
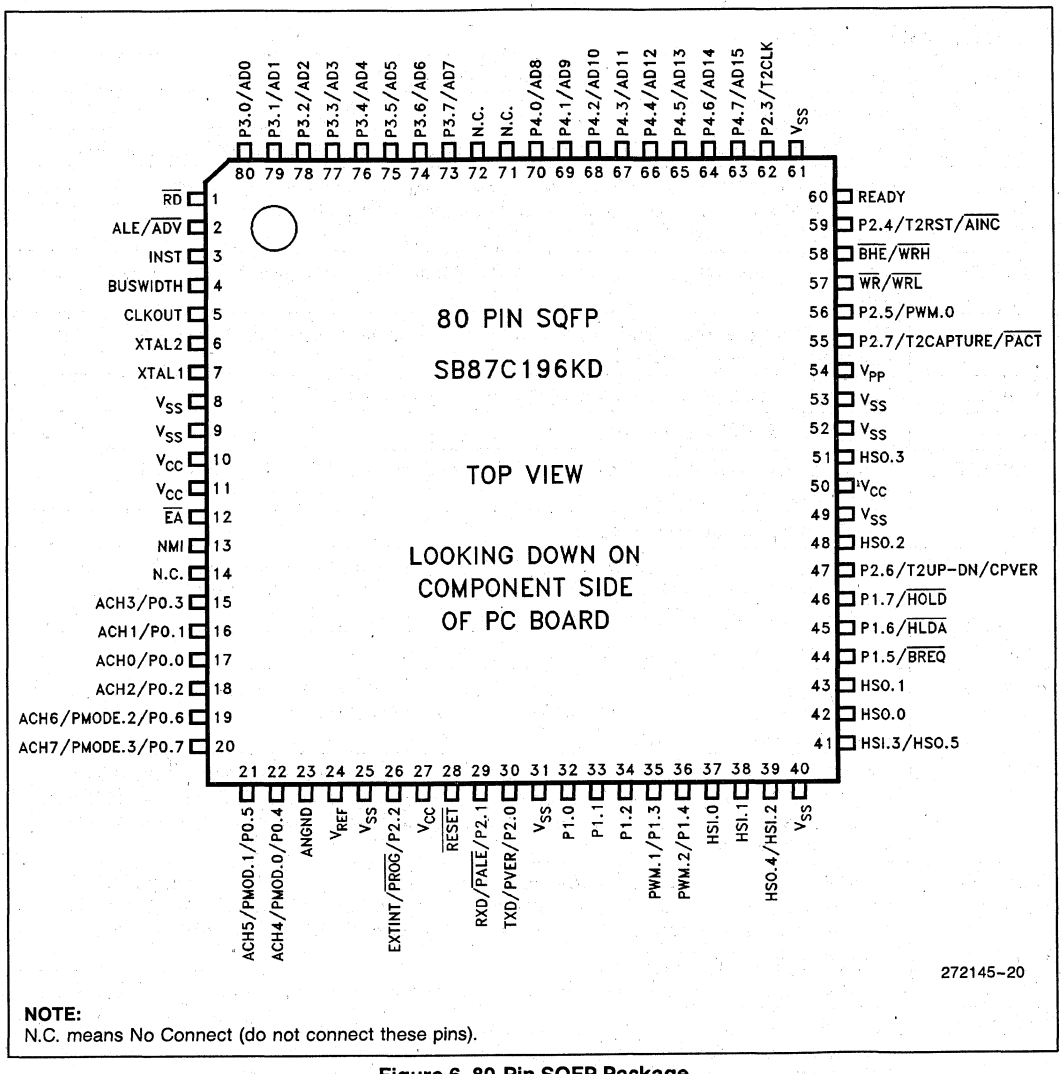


Figure 4. 68-Pin PLCC Package



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 5. 80-Pin QFP Package



NOTE:
N.C. means No Connect (do not connect these pins).

Figure 6. 80-Pin SQFP Package

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. This pin also supplies the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{\text{RESET}}$	Reset input and open drain output.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal high causes memory accesses to locations 2000H through 9FFFH to be directed to on-chip ROM/EPROM. $\overline{\text{EA}}$ equal low causes accesses to those locations to be directed to off-chip memory. Also used to enter programming mode.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ will go low for external writes to the high byte of the data bus. $\overline{\text{WRH}}$ will go low for external writes where an odd byte is being written. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 8XC196KD. Pins 2.6 and 2.7 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
$\overline{\text{PALE}}$	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER	Cummulative Program Output Verification. Pin is high if all locations have programmed correctly since entering a programming mode.
$\overline{\text{AINC}}$	Auto Increment. Active low input enables the auto increment mode. Auto increment allows reading or writing sequential EPROM locations without address transactions across the PBUS for each read or write.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS}
Except EA and V_{PP} ..... −0.5V to +7.0V(1)
Voltage from $\overline{EA}$ or
V_{PP} to V_{SS} or ANGND ..... −0.5V to +13.00V
Power Dissipation ..... 1.5W(2)

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} − 0.4	V_{SS} + 0.4	V(1)
F_{OSC}	Oscillator Frequency **(8XC196KD)**	8	16	MHz
F_{OSC}	Oscillator Frequency **(8XC196KD20)**	8	20	MHz

NOTE:
1. ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Over Specified Operating Conditions)

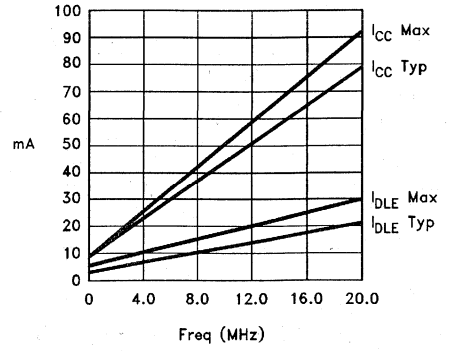
Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0	V_{CC} + 0.5	V	
V_{HYS}	Hysteresis on $\overline{RESET}$	300		mV	V_{CC} = 5.0V
V_{IH1}	Input High Voltage on XTAL 1	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.2	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I_{OL} = +0.4 mA
V_{OH}	Output High Voltage (Standard Outputs) (Note 4)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs) (Note 3)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −10 µA I_{OH} = −30 µA I_{OH} = −60 µA

DC CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
I_{OH1}	Logical 1 Output Current in Reset on P2.0. Do not exceed this or device may enter test modes.	−0.8			mA	$V_{IH} = V_{CC} - 1.5V$
I_{IL2}	Logical 0 Input Current in Reset on P2.0. Maximum current that must be sunk by external device to ensure test mode entry.			−12.0	mA	$V_{IN} = 0.45V$
I_{IH1}	Logical 1 Input Current. Maximum current that external device must source to initiate NMI.			+200	μA	$V_{IN} = 2.4V$
I_{LI}	Input Leakage Current (Std. Inputs) (Note 5)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)			−650	μA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)			−70	μA	$V_{IN} = 0.45V$
I_{IL1}	AD Bus in Reset			−70	μA	$V_{IN} = 0.45V$
I_{CC}	Active Mode Current in Reset **(8XC196KD)**		65	75	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{CC}	Active Mode Current in Reset **(8XC196KD20)**		80	92	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current **(8XC196KD)**		17	25	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current **(8XC196KD20)**		21	30	mA	XTAL1 = 20 MHz $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current		8	15	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Converter Reference Current		2	5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	$V_{CC} = 5.5V, V_{IN} = 4.0V$
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	

NOTES:
1. All pins except RESET and XTAL1.
2. Violating these specifications in Reset may cause the part to enter test modes.
3. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
4. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
5. Standard Inputs include HSI pins, READY, BUSWIDTH, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
6. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below $V_{CC} - 0.7V$:
   - I_{OL} on Output pins: 10 mA
   - I_{OH} on quasi-bidirectional pins: self limiting
   - I_{OH} on Standard Output pins: 10 mA
7. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
8. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA



I_{CC} Max = 4.13 × Frequency + 9 mA
I_{CC} Typ = 3.50 × Frequency + 9 mA
I_{IDLE} Max = 1.25 × Frequency + 5 mA
I_{IDLE} Typ = 0.88 × Frequency + 3 mA

NOTE:
Frequencies below 8 MHz are shown for reference only; no testing is performed.

Figure 7. I_{CC} and I_{IDLE} vs Frequency

AC CHARACTERISTICS

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16/20 MHz

The system must meet these specifications to work with the 80C196KD:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} − 68	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} − 30	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	T_{OSC} − 15	2 T_{OSC} − 40	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} − 68	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} − 55	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		T_{OSC} − 22	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} − 45	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

AC CHARACTERISTICS (Continued)

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16/20 MHz

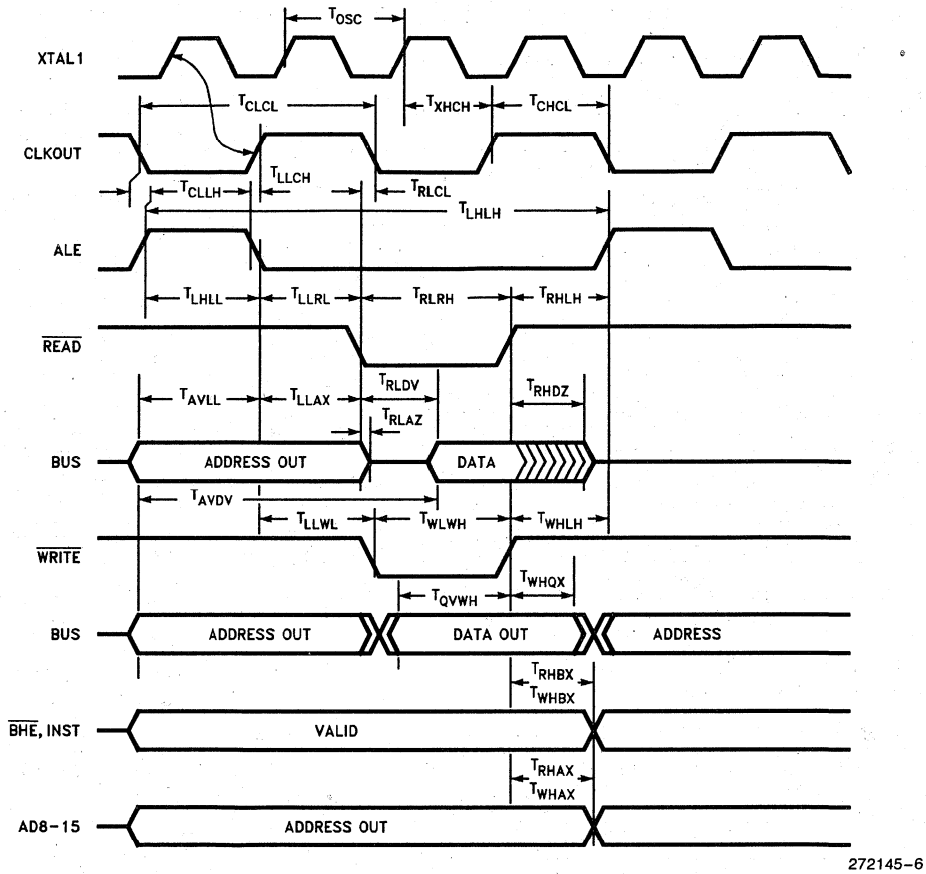
The 80C196KD will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1 **(8XC196KD)**	8	16	MHz	(Note 1)
F_{XTAL}	Frequency on XTAL1 **(8XC196KD20)**	8	20	MHz	(Note 1)
T_{OSC}	$1/F_{XTAL}$ **(8XC196KD)**	62.5	125	ns	
T_{OSC}	$1/F_{XTAL}$ **(8XC196KD20)**	50	125	ns	
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	+15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 4)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15			
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 35		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	+4	+30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns	(Note 4)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23			(Note 4)
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	+15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 20		ns	(Note 4)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	T_{OSC} − 30		ns	(Note 3)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	T_{OSC} − 25		ns	(Note 3)

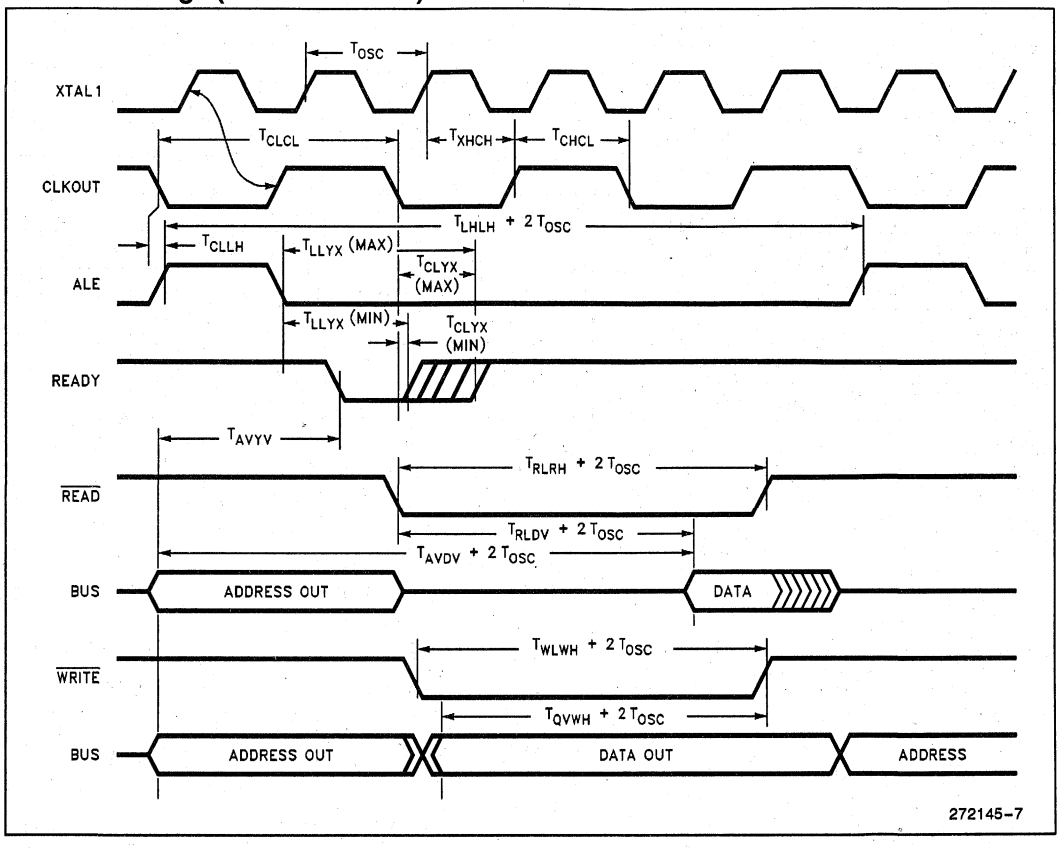
NOTES:

1. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.

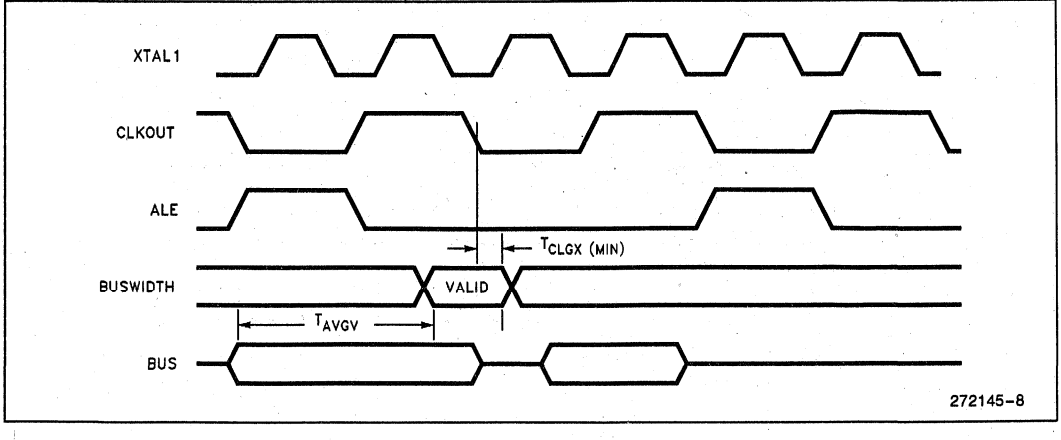
System Bus Timings



READY Timings (One Wait State)



Buswidth Timings



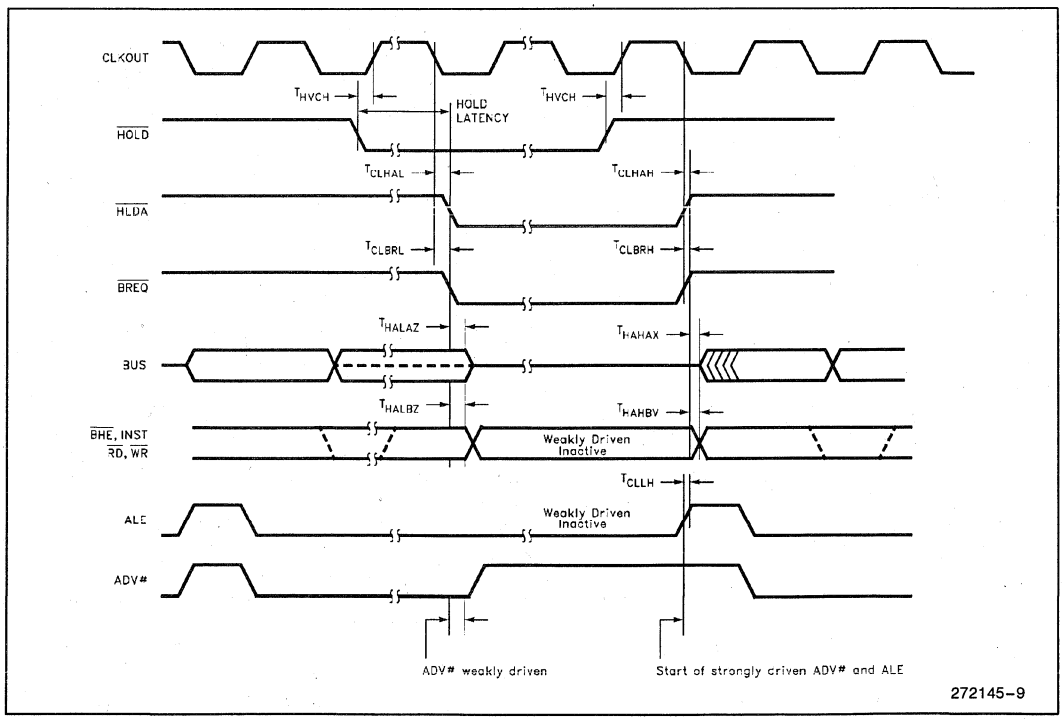
$\overline{HOLD}/\overline{HLDA}$ TIMINGS

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	$\overline{HOLD}$ Setup	+55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to $\overline{HLDA}$ Low	−15	+15	ns	
T_{CLBRL}	CLKOUT Low to $\overline{BREQ}$ Low	−15	+15	ns	
T_{HALAZ}	$\overline{HLDA}$ Low to Address Float		+15	ns	
T_{HALBZ}	$\overline{HLDA}$ Low to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Weakly Driven		+20	ns	
T_{CLHAH}	CLKOUT Low to $\overline{HLDA}$ High	−15	+15	ns	
T_{CLBRH}	CLKOUT Low to $\overline{BREQ}$ High	−15	+15	ns	
T_{HAHAX}	$\overline{HLDA}$ High to Address No Longer Float	−15		ns	
T_{HAHBV}	$\overline{HLDA}$ High to $\overline{BHE}$, INST, $\overline{RD}$, $\overline{WR}$ Valid	−10	+15	ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	+15	ns	

NOTE:
1. To guarantee recognition at next clock.

DC SPECIFICATIONS IN HOLD

Description	Min	Max	Units
Weak Pullups on $\overline{ADV}$, $\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{BHE}$	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4



MAXIMUM HOLD LATENCY

Bus Cycle Type	
Internal Execution	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

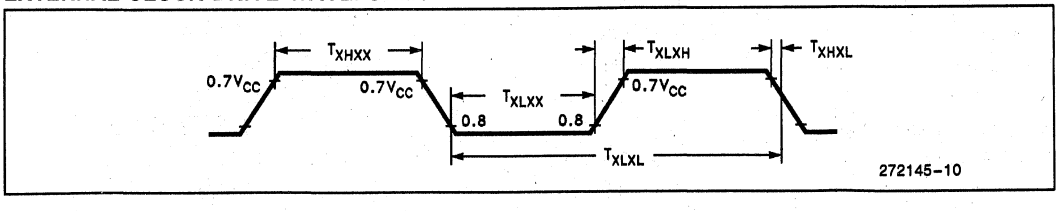
EXTERNAL CLOCK DRIVE (8XC196KD)

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	20		ns
T_{XLXX}	Low Time	20		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

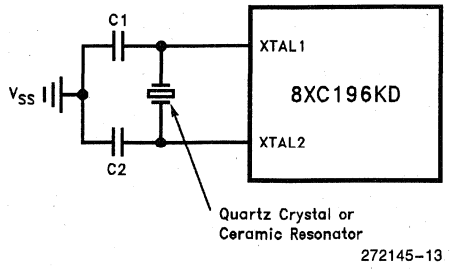
EXTERNAL CLOCK DRIVE (8XC196KD20)

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	20.0	MHz
T_{XLXL}	Oscillator Period	50	125	ns
T_{XHXX}	High Time	17		ns
T_{XLXX}	Low Time	17		ns
T_{XLXH}	Rise Time		8	ns
T_{XHXL}	Fall Time		8	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



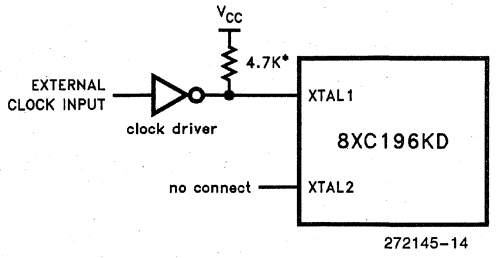
EXTERNAL CRYSTAL CONNECTIONS



272145-13

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using ceramic crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators consult manufacturer for recommended capacitor values.

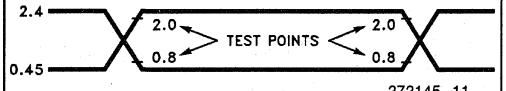
EXTERNAL CLOCK CONNECTIONS



272145-14

NOTE:
*Required if TTL driver used.
Not needed if CMOS driver is used.

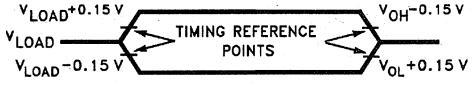
AC TESTING INPUT, OUTPUT WAVEFORMS



272145-11

AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



272145-12

For Timing Purposes a Port Pin is no Longer Floating when a 150 mV change from Load Voltage Occurs, and Begins to Float when a 150 mV change from the Loaded V_{OH}/V_{OL} Level occurs; $I_{OL}/I_{OH} = \pm 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
BR— $\overline{BREQ}$
R— $\overline{RD}$
W— $\overline{WR}/\overline{WRH}/\overline{WRL}$
X— XTAL1
Y— READY
Q— Data Out

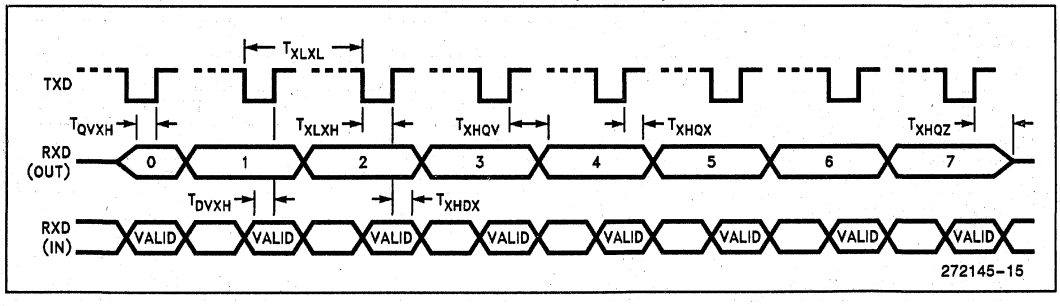
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} −50	4 T_{OSC} +50	ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} −50	2 T_{OSC} +50	ns
T_{QVXH}	Output Data Valid to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)



A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} − 0.40	V_{CC} + 0.40	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	10	20	μs(1)
F_{OSC}	Oscillator Frequency **(8XC196KD)**	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency **(8XC196KD20)**	8.0	20.0	MHz

NOTE:
1. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±3	LSBs	
Full Scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Non-Linearity	1.0 ± 2.0	0	±3	LSBs	
Differential Non-Linearity Error		> −1	+2	LSBs	
Channel-to-Channel Matching	±0.1	0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approxiimately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms.)
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V_{SS} −0.40	V_{SS} + 0.40	V
T_{SAM}	Sample Time	1.0		μs(1)
T_{CONV}	Conversion Time	7	20	μs(1)
F_{OSC}	Oscillator Frequency **(8XC196KD)**	8.0	16.0	MHz
F_{OSC}	Oscillator Frequency **(8XC196KD20)**	8.0	20.0	MHz

NOTE:
1. The value of AD__TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±1	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±1	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	2, 3
Feedthrough	−60			dB	2
V_{CC} Power Supply Rejection	−60			dB	2
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

NOTES:
*An "LSB" as used here has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

OTPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming **(8XC196KD)**	6.0	16.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming **(8XC196KD20)**	6.0	20.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC OTPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

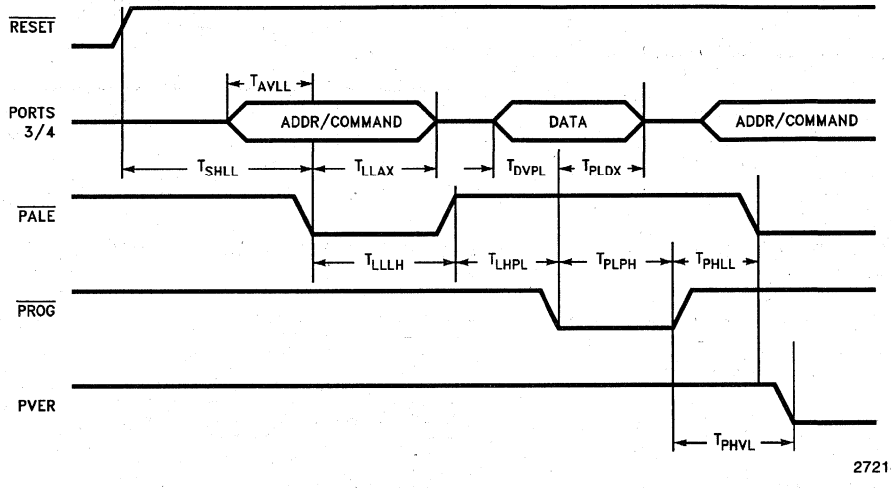
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

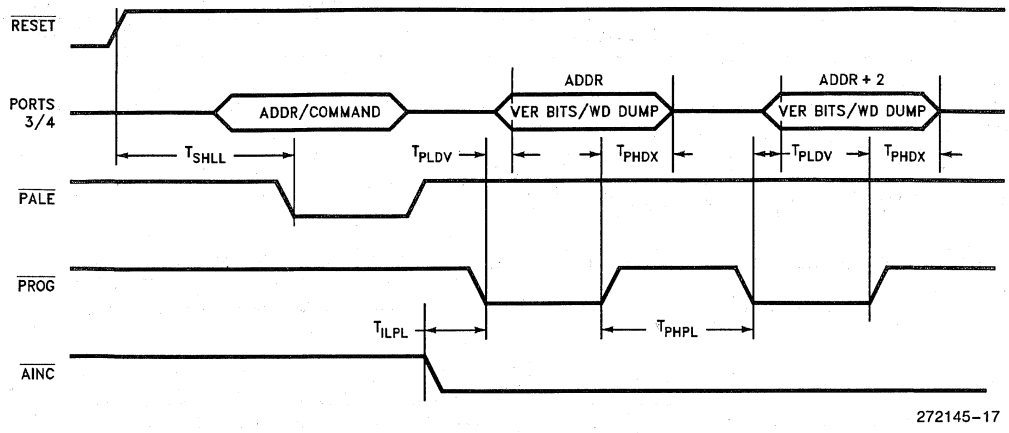
OTPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



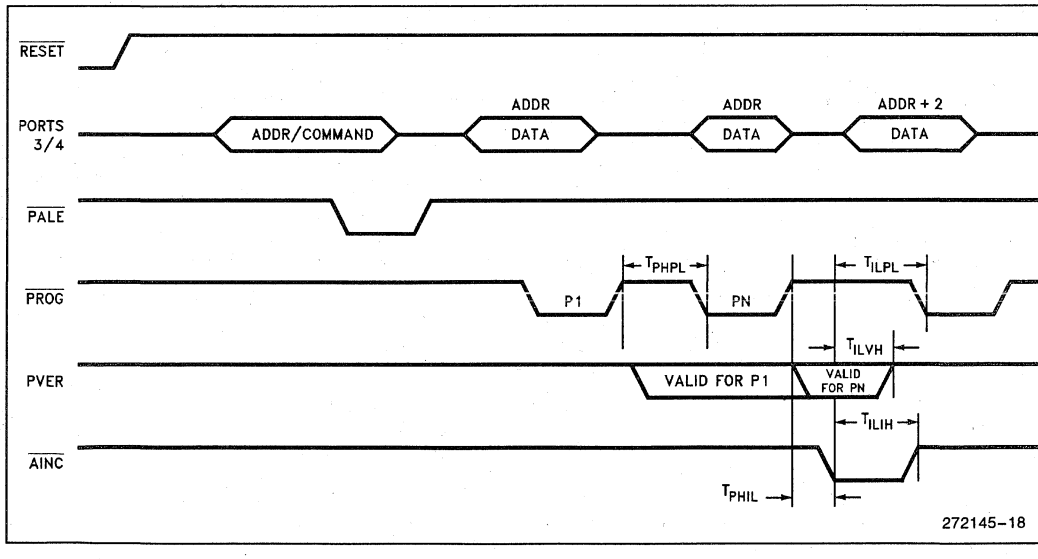
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



8XC196KC TO 8XC196KD DESIGN CONSIDERATIONS

1. Memory Map. The 8XC196KD has 1024 bytes of RAM/SFRs and 32K of OTPROM. The extra 512 bytes of RAM reside in locations 0200H to 03FFH, and the extra 16 Kbytes of OTPROM reside in locations 6000H to 9FFFH. On the 87C196KC these locations are always external, so KC code may have to be modified to run on the KD.
2. The vertical window scheme has been extended to include all on-chip RAM.
3. IOC3.1 controls the CLKOUT signal. This bit must be 0 to enable CLKOUT.
4. The 87C196KD has a different autoprogramming algorithm to support 32K of on-chip OTPROM.

8XC196KD ERRATA

1. 83C196KD can possibly miss interrupts on P0.7. See techbit MC0893.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a "D" and "E" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are important differences between the 272145-002 and 272145-003 data sheets:

1. I_{IL1} specification (logic 0 input current in reset) was misnamed. It is renamed I_{IL2}.
2. T_{LLYV} and T_{LLGV} were removed. These specifications are not necessary for high-speed system designs.
3. An errata with 83C196KD P0.7 EXTINT was added to the errata section.

The following are important differences between the 272145-001 and 272145-002 data sheets:

1. Added 20 MHz specifications.
2. Added 80-lead SQFP package pinout.
3. Changed QFP Package θ_{JA} to 56°C/W from 42°C/W.
4. Changed V_{HYS} to 300 mV from 150 mV.
5. Changed I_{CC} Typical specification at 16 MHz to 65 mA from 50 mA.
6. Changed I_{CC} Maximum specification at 16 MHz to 75 mA from 70 mA.
7. Changed I_{IDLE} Typical specification to 17 mA from 15 mA.
8. Changed I_{IDLE} Maximum specification to 25 mA from 30 mA.
9. Changed I_{PD} Typical specification to 8 μA from 15 μA.
10. Added I_{PD} Maximum specification.
11. Changed T_{CLDV} Maximum specification to $T_{OSC} - 45$ from $T_{OSC} - 50$.
12. Changed T_{LLAX} Minimum specification to $T_{OSC} - 35$ from $T_{OSC} - 40$.
13. Changed T_{CHWH} Minimum specification to -5 from -10.
14. Changed T_{RHAX} Minimum specification to $T_{OSC} - 25$ from $T_{OSC} - 30$.
15. Changed T_{HALAZ} Maximum specification to $+15$ from $+10$.
16. Changed T_{HALBZ} Maximum specification to $+20$ from $+15$.
17. Added T_{HAHBV} Maximum specification.
18. Changed T_{SAM} for 10-bit mode to 1 μs from 3 μs.
19. Changed T_{SAM} for 8-bit mode to 1 μs from 2 μs.
20. Changed I_{IH1} test condition to $V_{IN} = 2.4V$ from 5.5V.
21. Changed I_{IH1} maximum specification to $+200$ μA from $+100$ μA.
22. Removed NMI from list of standard inputs.
23. Updated I_{CC} and I_{IDLE} vs frequency graph.
24. Updated note under DC EPROM Programming Characteristics.
25. Changed I_{LI1} maximum specification to -12 mA from -6 mA.

8XC196KR/KQ/JR/JQ
COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER

87C196KR/KQ/JR/JQ—16 Kbytes of On-Chip OTPROM
80C196KR/KQ/JR/JQ—ROMless

- High Performance CHMOS 16-Bit CPU
- 16 MHz Operating Frequency
- Up to 488 Bytes of On-Chip Register RAM
- 256 Bytes of Additional RAM (Code or Data RAM)
- Register-Register Architecture
- 8 Channel/10-Bit A/D with Sample/Hold
- 37 Prioritized Interrupt Sources
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port (SIO) and Full Duplex Synchronous Serial I/O Port (SSIO) with Dedicated Baud Rate Generators
- Interprocessor Communication Slave Port
- Watchdog Timer
- High-Speed Peripheral Transaction Server (PTS)
- Two Programmable 16-Bit Timer/Counters with Prescale, Cascading, Standard and Quadrature Counting Inputs
- 10 High-Speed Capture/Compare (EPA)
- Two Dedicated High Speed Compare Registers
- Two Flexible 16-Bit Timer/Counters
- Quadrature Counting Inputs
- Flexible 8-/16-Bit External Bus
- Programmable Bus (HOLD/HLDA)
- 1.75 μs 16 x 16 Multiply
- 3 μs 32/16 Divide
- Extended Temperature Available
- 68-Pin and 52-Pin PLCC Packages

Device	Pins/Package	OTPROM	Reg RAM	Internal RAM	I/O	EPA	SIO	SSIO	A/D
87C196KR	68 p PLCC	16K	512	256	56	10	Y	Y	8
87C196KQ	68 p PLCC	12K	384	128	56	10	Y	Y	8
87C196JR	52 p PLCC	16K	512	256	41	6	Y	Y	6
87C196JQ	52 p PLCC	12K	384	128	41	6	Y	Y	6
80C196KR	68 p PLCC	0	512	256	56	10	Y	Y	8
80C196KQ	68 p PLCC	0	384	128	56	10	Y	Y	8
80C196JR	52 p PLCC	0	512	256	41	6	Y	Y	6
80C196JQ	52 p PLCC	0	384	128	41	6	Y	Y	6

The 87C196KR/KQ/JR/JQ devices represent the 4th generation of MCS® 96 products implemented on Intel's advanced 1 micron process technology. These products are members of the 80C196 family of devices and the instruction set is the same as that of the 80C196KC. The 87C196JR is a 52-lead version of the 87C196KR device, while the 87C196KQ/JQ are memory scalars of the 87C196KR/JR.

The MCS 96 microcontroller family members are all high-performance microcontrollers with a 16-bit CPU. The 87C196KR is composed of the high-speed (16 MHz) core as well as the following peripherals: up to 16 Kbytes of on-chip EPROM, up to 512 bytes of Register RAM, 256 bytes of Code RAM, an eight-channel 10-bit analog to digital converter, an (8096 compatible) asynchronous/synchronous serial I/O port, an additional synchronous serial I/O port, 10 modularized multiplexed capture and compare channels (called the Event Processor Array), a sophisticated prioritized interrupt structure with the programmable Peripheral Transaction Server (PTS).

November 1994

Order Number: 270912-004

Additional register space is allocated for the EPA and can be windowed into the lower Register RAM area.

With the commercial (standard) temperature option, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended (**Express**) temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C. Unless otherwise noted, the specifications are the same for both options.

See the prefix identification for extended temperature designators.

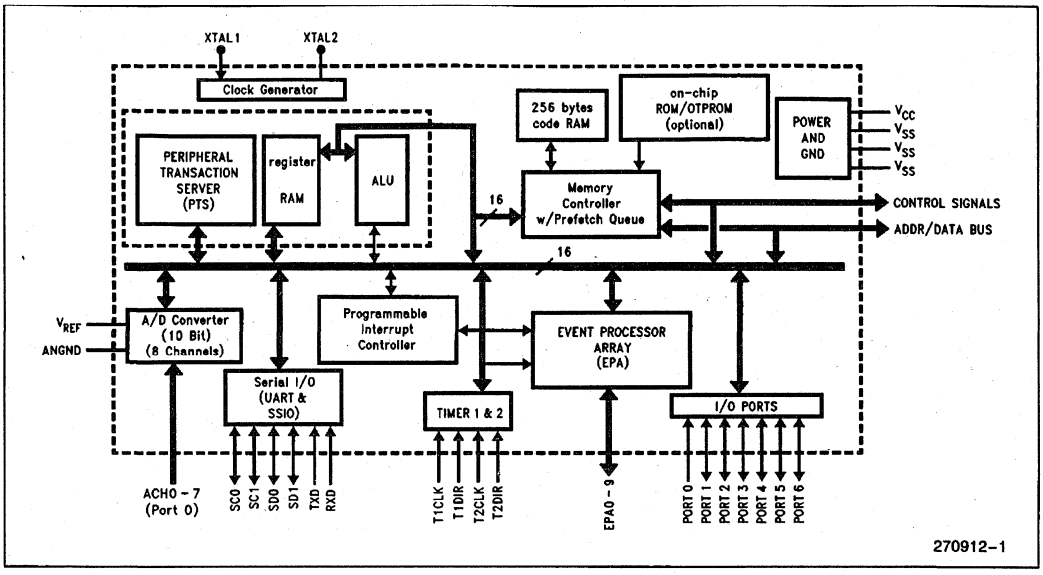


Figure 1. Block Diagram

0FFFFH 06000H	External Memory
05FFFH 02080H	Internal ROM/EPROM or External Memory
0207FH 0205EH	Reserved
0205DH 02040H	PTS Vectors
0203FH 02030H	Interrupt Vectors (upper)
0202FH 02020H	ROM/EPROM Security Key
0201FH	Reserved
0201BH	Reserved (must contain 20H)
0201AH	CCB1
02019H	Reserved (must contain 20H)

02018H	CCB0
02017H 02014H	Reserved
02013H 02000H	Interrupt Vectors (lower)
01FFFH 01F00H	Internal SFRs
01EFFH 00500H	External Memory
004FFH 00400H	Internal RAM
003FFH 00200H	External Memory
001FFH 18H	Register File
17H 00H	CPU SFR's

NOTES:
1. Reserved memory locations must contain 0FFH unless noted.
2. Reserved SFR bit locations must contain 0H unless noted.
3. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

Process Information

The 8XC196KR/JR/KQ/JQ is manufactured on PX29.5, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

Table 1. Prefix Identification

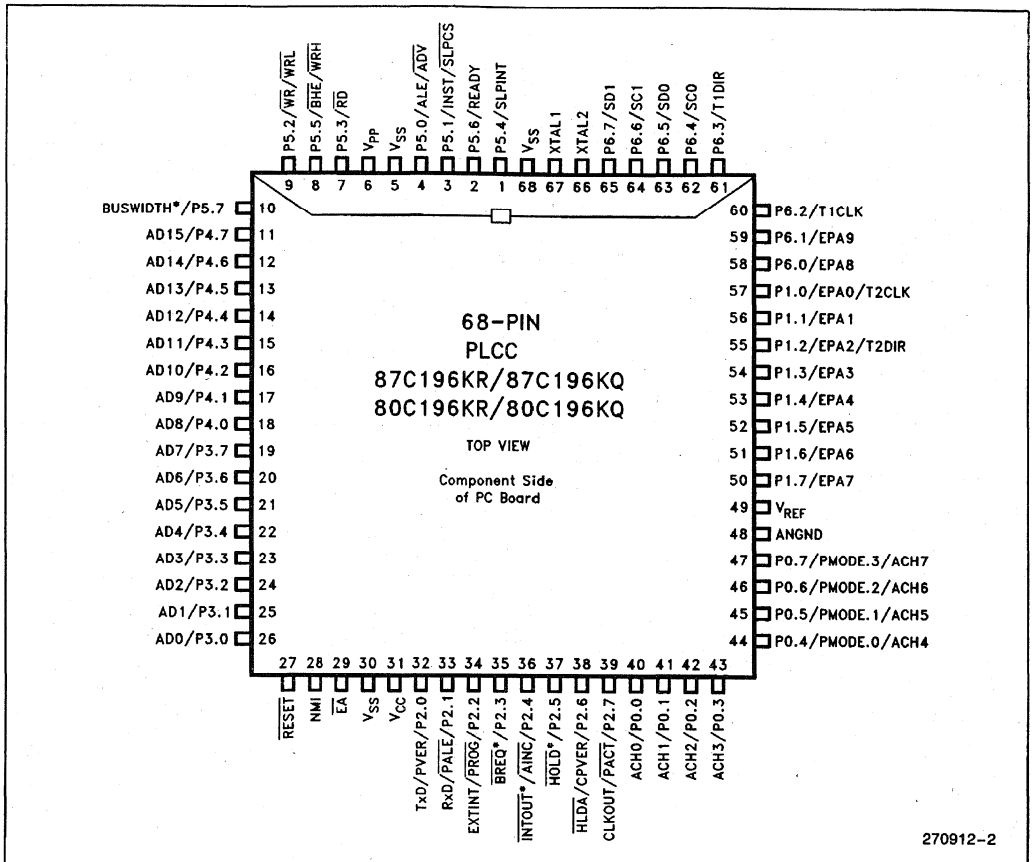
Device	Commercial PLCC	Express PLCC
80C196KR	N80C196KR	*TN80C196KR
80C196JR	N80C196JR	*TN80C196JR
80C196KQ	N80C196KQ	*TN80C196KQ
80C196JQ	N80C196JQ	*TN80C196JQ
87C196KR	N87C196KR	*TN87C196KR
87C196JR	N87C196JR	*TN87C196JR
87C196KQ	N87C196KQ	*TN87C196KQ
87C196JQ	N87C196JQ	*TN87C196JQ

*T = Extended Temperature, no burn-in.

Table 2. Thermal Characteristics

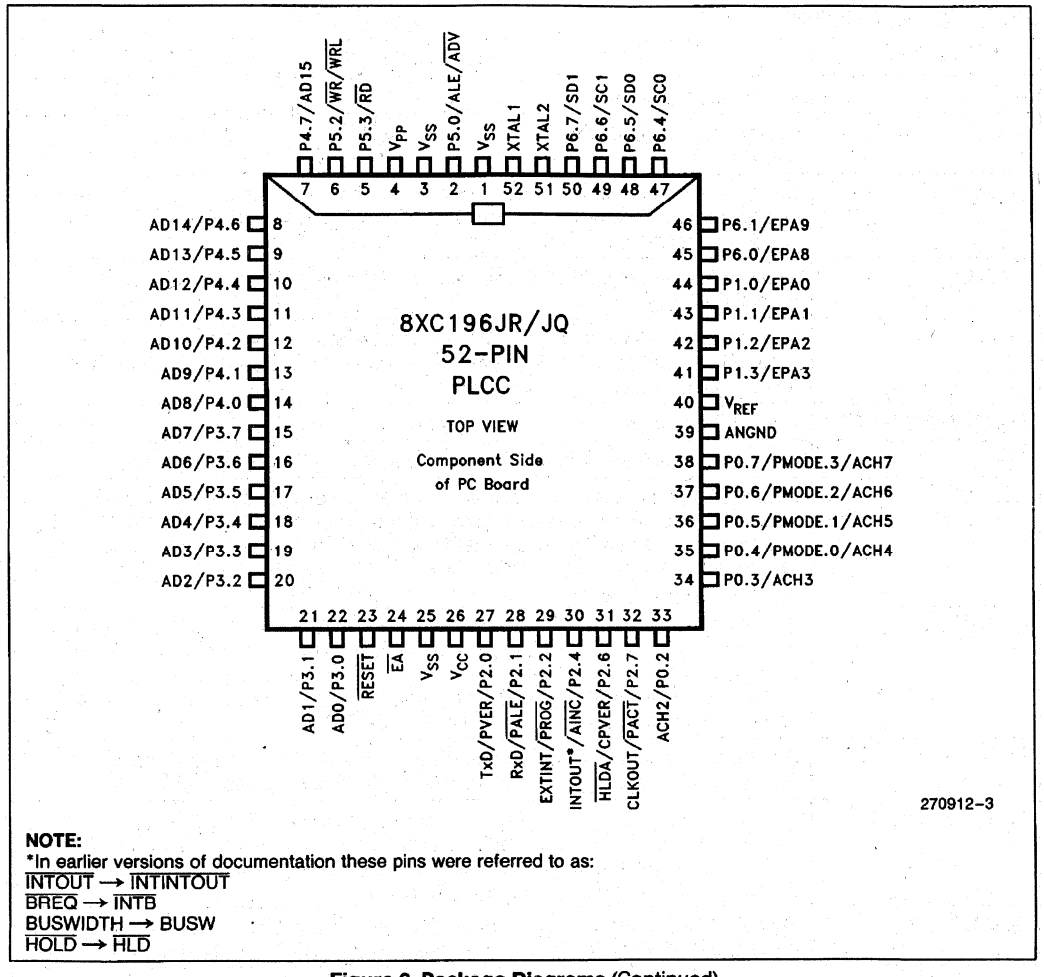
Package	θ_{ja}	θ_{jc}
52-Lead PLCC	35°C/W	12°C/W
68-Lead PLCC	35°C/W	13°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See Intel *Packaging Handbook,* (Order Number 240800) for a description of Intel's thermal impedance test methodology.



NOTE:
*In earlier versions of documentation these pins were referred to as:
INTOUT → INTINTOUT
BREQ → INTB
BUSWIDTH → BUSW
HOLD → HLD

Figure 2. Package Diagrams



NOTE:
*In earlier versions of documentation these pins were referred to as:
INTOUT → INTINTOUT
BREQ → INTB
BUSWIDTH → BUSW
HOLD → HLD

Figure 2. Package Diagrams (Continued)

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Programming voltage for the OTPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. If this function is not used, V_{PP} must be tied to V_{CC}.
ACH0–ACH7/PORT0	Analog inputs to the on-chip A/D converter.
$\overline{AINC}$	Input to automatically increment the address when in Programming mode.
ALE/$\overline{ADV}$/P5.0	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options allow a latch to demultiplex the address/data bus. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. When the pin is ALE, the address can be latched on the falling edge. ALE/$\overline{ADV}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE.
$\overline{BHE}$/$\overline{WRH}$/P5.5	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is only valid during 16-bit external memory cycles. Can be used as standard I/O when not used as $\overline{BHE}$/$\overline{WRH}$.
$\overline{BREQ}$/P2.3	Bus Request output activated when the bus controller has a pending external memory cycle. Can be used as standard I/O when not used as $\overline{BREQ}$.
BUSWIDTH/P5.7	Input for bus width selection. If CCR bit 1 = 1 and CCR1 bit 2 = 1, this pin dynamically controls the Bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. Can be used as standard I/O when not used as BUSWIDTH.
CLKOUT/P2.7	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Can be used as standard I/O when not used as CLKOUT.
CPVER	Cumulative Program Verify output. Indicates when all EPROM locations program correctly.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ = 1 causes memory accesses from locations 2000H to 5FFFH to be directed to on-chip EPROM/ROM. $\overline{EA}$ = 0 causes all memory accesses to be directed to off-chip memory. $\overline{EA}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{EA}$ is latched at reset.
EPA0–7/PORT1 EPA8-9/P6.0–6.1	Event Processor Array pin for High Speed capture and compare. EPA0 and EPA2 also function as T2CLK and T2DIR. Can be used as standard I/O when not used as EPA or T2 clock functions.
EXTINT/P2.2	A positive transition on this pin causes a maskable interrupt vector through memory location 203CH. May be used as standard I/O if not used as EXTINT.
$\overline{HLDA}$/P2.6	Bus Hold Acknowledge output indicating release of the bus. Can be used as standard I/O when not used as $\overline{HLDA}$.
$\overline{HOLD}$/P2.5	Bus Hold input requesting control of the bus. Can be used as standard I/O when not used as $\overline{HOLD}$.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
INST/P5.1	Output high during an external memory instruction fetch. INST is valid throughout the bus cycle. INST is low otherwise. Can be used as standard I/O when not used as INST.
$\overline{\text{INTOUT}}$/P2.4	Interrupt output indicating that a pending interrupt requires use of the external bus. Can be used as standard I/O if not used as $\overline{\text{INTOUT}}$.
NMI	A positive transition causes a non-maskable interrupt vector through memory location 203EH. If not used, this pin should be tied to V_{SS}. May be used by Intel Evaluation boards.
$\overline{\text{PACT}}$	Output that indicates when the device is currently programming itself. Not active during slave programming.
$\overline{\text{PALE}}$	Input to latch the address during programming modes.
PMODE.0–PMODE.3	Programming mode select inputs.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port 0 pins should not be left floating. These pins are also used as inputs by EPROM parts to select the Programming Mode.
PORT1	8-bit bidirectional standard I/O port. All of its pins are shared with the EPA.
PORT2	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (TxD, RxD, EXTINT, $\overline{\text{BREQ}}$, $\overline{\text{INTOUT}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$, CLKOUT).
PORT3 PORT4	8-bit bidirectional standard I/O with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (ALE/$\overline{\text{ADV}}$, INST, $\overline{\text{WR}}$/$\overline{\text{WRL}}$, $\overline{\text{RD}}$, SLPINT, $\overline{\text{BHE}}$/$\overline{\text{WRH}}$, READY, BUSWIDTH).
PORT6	8-bit bidirectional standard I/O port. All of its pins are shared with other functions (EPA8, EPA9, T1CLK, T1DIR, SC0, SD0, SC1, SD1).
$\overline{\text{PROG}}$	Programming mode enable input.
PVER	Program Verify output. Goes high after a byte/word is programmed to indicate a successful operation.
$\overline{\text{RD}}$/P5.3	Read signal output to external memory. $\overline{\text{RD}}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{\text{RD}}$.
READY/P5.6	Ready input to lengthen external memory cycles. If READY = 1, CPU operation continues in a normal manner. If READY = 0 with the appropriate timings, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{\text{RESET}}$	Reset input to and output from the chip. Held low for at least 16 state times to reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence. Input high for normal operation. $\overline{\text{RESET}}$ has an internal pullup.
RXD/P2.1	Receive data input pin for the Serial I/O port. Can be used as standard I/O if not used as RXD.
$\overline{\text{SLPCS}}$	Slave port chip select input pin. Can be used as standard I/O if not used as $\overline{\text{SLPCS}}$.
SLPINT/P5.4	Slave Port Interrupt Output pin. Can be used as standard I/O when not used as SLPINT.
SSIO/P6.4–6.7 (SC0, SD0, SC1, SD1)	Synchronous Serial I/O pins. SC0/SC1 serve as clock pins and SD0/SD1 are data pins. Can be used as standard I/O if not used for serial I/O.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
T1CLK/P6.2	TIMER1 Clock input. The timer increments or decrements on both positive and negative edges. Can be used as standard I/O when not used as T1CLK.
T1DIR/P6.3	TIMER1 Direction input. The timer increments when this pin is high and decrements when this pin is low. Can be used as standard I/O when not used as T1DIR.
T2CLK/P1.0	TIMER2 Clock input. The timer increments or decrements on both positive and negative edges. Can be used as standard I/O when not used as T2CLK.
T2DIR/P1.2	TIMER2 Direction input. The timer increments when this pin is high and decrements when this pin is low. Can be used as standard I/O when not used as T2DIR.
TXD/P2.0	Transmit data output pins for the Serial I/O port. Can be used as standard I/O if not used as TXD.
$\overline{WR}$/$\overline{WRL}$/P5.2	Write and Write Low output to external memory. $\overline{WR}$ will go low for every external write. $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is active only during external memory writes. Can be used as standard I/O when not used as $\overline{WR}$/$\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... −60°C to +150°C

Ambient Temperature under Bias ..... −55°C to +125°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND ..... −0.5V to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation 1.0W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature under Bias **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature under Bias **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	16	MHz(4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

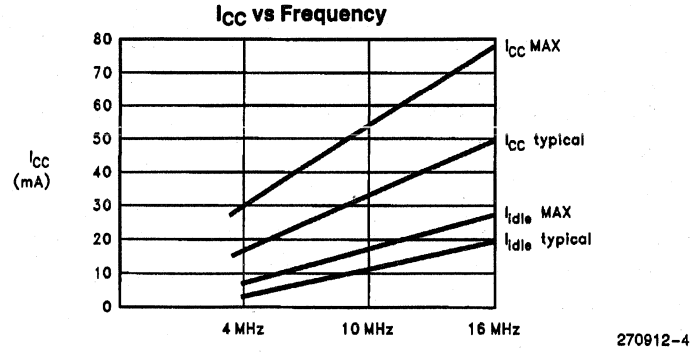
DC CHARACTERISTICS (Over Specified Operating Conditions)(9)

Symbol	Parameter	Min	Typ(6)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (All Pins)	−0.5V		0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Outputs Configured as Push/Pull)			0.3 0.45 1.5	V V V	I_{OL} = 200 μA(3, 5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Push/Pull)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA(3, 5, 8) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
V_{OH2}	Output High Voltage in RESET	V_{CC} − 1V			V	I_{OH} = −15 μA(1, 7)
I_{LI}	Input Leakage Current (Std. Inputs)			±10	μA	$V_{SS} < V_{IN} < V_{CC}$ − 0.3V(2)
I_{LI1}	Input Leakage Current (Port 0—A/D Inputs)		±1	±3	μA	$V_{SS} < V_{IN} < V_{REF}$
I_{IH}	Input High Current (NMI)			+175	μA	$V_{SS} < V_{IN} < V_{CC}$ − 0.3V(10)

DC CHARACTERISTICS (Over Specified Operating Conditions)(9) (Continued)

Symbol	Parameter	Min	Typ(6)	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		60	75	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While Device in Reset)
I_{REF}	A/D Reference Supply Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current(6)		50	TBD	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K		65K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz
R_{WPU}	Weak Pullup Resistance (Approx)		150K		Ω	(6)

NOTES:
1. All BD (Bidirectional) pins except INST and CLKOUT. BD pins include Port1, Port2, Port3, Port4, Port5 (as a port), and Port6.
2. Standard Input pins include XTAL1, $\overline{EA}$, $\overline{RESET}$, and Port 1/2/3/4/5/6 when setup as inputs.
3. All Bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is Static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{OL}/I_{OH} currents per pin will be characterized and published at a later date.
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. This specification applies to P3/4 only when used as an address bus supplying the address.
9. All voltages are referenced relative to V_{SS}. When used, V_{SS} refers to the device pin.
10. Worst case is at upper limit of test conditions.



NOTES:
I_{CC} Max = 3.88 × FREQ + 13.43
I_{idle} Max = 1.65 × FREQ + 2.2

AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 87C196KR/KQ/JR/JQ:

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC}-75$	ns(2)
T_{LLYV}	ALE Low to READY Setup		$T_{OSC}-70$	ns(2)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC}-30$	ns(1, 2)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC}-15$	$2T_{OSC}-40$	ns(1, 2)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC}-75$	ns(2)
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC}-60$	ns(2)
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns(2)
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC}-55$	ns
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC}-22$	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC}-50$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns

NOTE:
1. If max is exceeded, additional wait states will occur.
2. Does not apply to JR/JQ.

AC CHARACTERISTICS (Over Specified Operating Conditions)

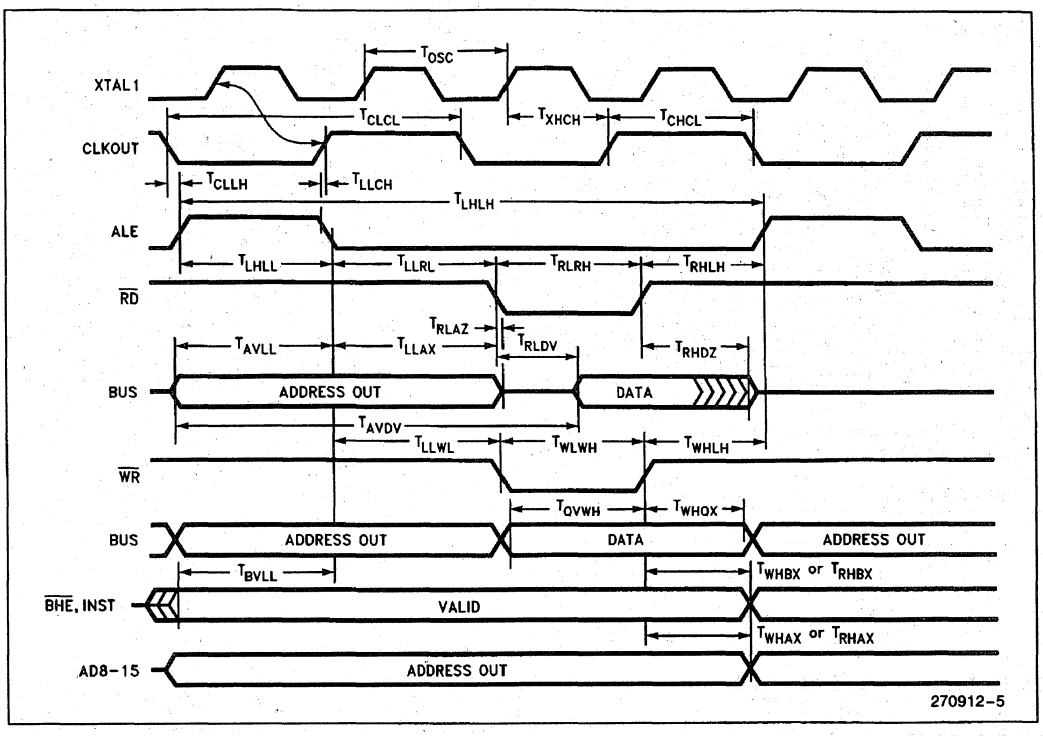
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 87C196KR/KQ/JR/JQ will meet these specifications.

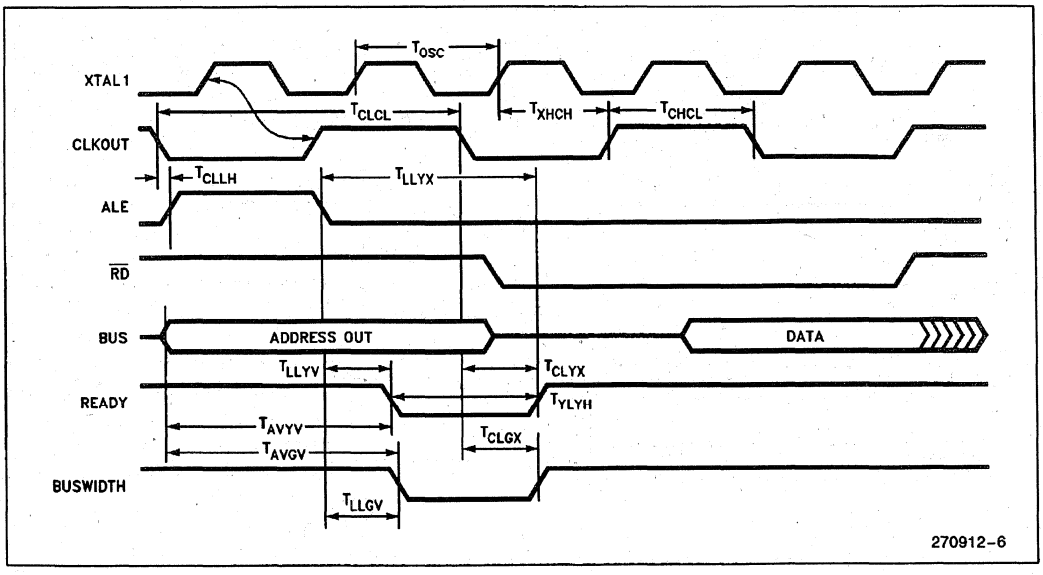
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Oscillator Frequency	4.0	16.0	MHz(1)
T_{OSC}	Oscillator Period (1/Fxtal)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns(2)
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	$T_{OSC}-10$	$T_{OSC}+15$	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Falling Edge to CLKOUT Rising	−20	15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Period	$T_{OSC}-10$	$T_{OSC}+10$	ns
T_{AVLL}	Address Setup to ALE/$\overline{ADV}$ Falling Edge	$T_{OSC}-15$		ns
T_{LLAX}	Address Hold after ALE/$\overline{ADV}$ Falling Edge	$T_{OSC}-40$		ns
T_{LLRL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{RD}$ Falling Edge	$T_{OSC}-30$		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns
T_{RLRH}	$\overline{RD}$ Low Period	$T_{OSC}-5$		ns(5)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	T_{OSC}	$T_{OSC}+25$	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Falling Edge to $\overline{WR}$ Falling Edge	$T_{OSC}-10$		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	−5	25	ns
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	$T_{OSC}-23$		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns
T_{WLWH}	$\overline{WR}$ Low Period	$T_{OSC}-30$		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-25$		ns
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE/$\overline{ADV}$ Rising Edge	$T_{OSC}-10$	$T_{OSC}+15$	ns(3)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-10$		ns(6)
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	$T_{OSC}-30$(4)		ns
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising Edge	$T_{OSC}-10$		ns(6)
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	$T_{OSC}-30$(4)		ns
T_{BVLL}	BHE Valid to ALE Falling Edge	$T_{OSC}-15$		ns(6)

NOTES:
1. Testing performed at 4.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 $T_{OSC} \times n$, where n = number of wait states.
6. Does not apply to JR/JQ.

System Bus Timing



Buswidth Timings



HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	65		ns	(1, 2)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	15	ns	(2)
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	15	ns	(2)
T_{AZHAL}	HLDA Low to Address Float		25	ns	(2)
T_{BZHAL}	HLDA Low to BHE, INST, RD, WR Weakly Driven		25	ns	(2)
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	(2)
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	(2)
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	(2)
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−10		ns	(2)
T_{CLLH}	CLKOUT Low to ALE High	−10	15	ns	

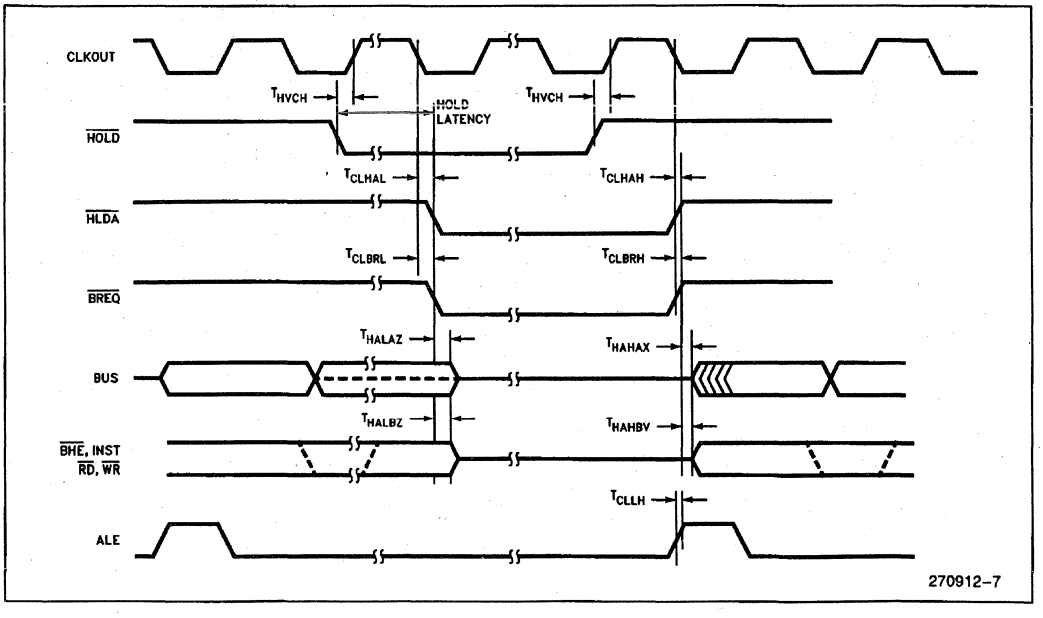
NOTE:
1. To guarantee recognition at next clock.
2. Does not apply to JR/JQ.

HOLD LATENCY

	Max
Internal Access	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

DC SPECIFICATIONS IN HOLD

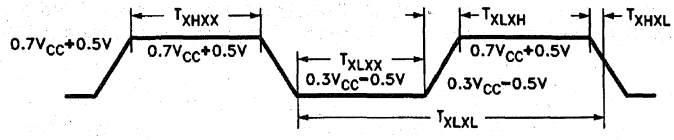
Parameter	Min	Max	Units
Weak Pullups on ADV, RD, WR, WRL, BHE	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4V



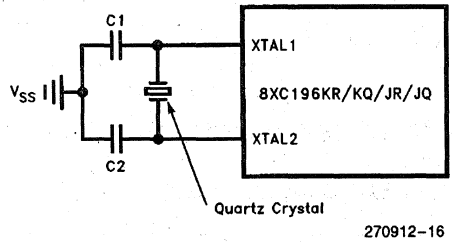
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4.0	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	250	ns
T_{XHXX}	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS

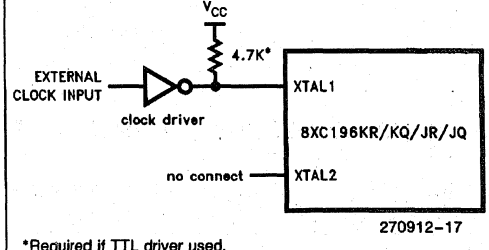


EXTERNAL CRYSTAL CONNECTIONS



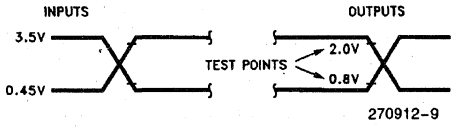
NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using quartz crystals, typically C1 ≈ 22 pF and C2 ≈ 22 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

EXTERNAL CLOCK CONNECTIONS



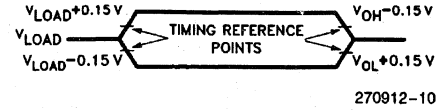
*Required if TTL driver used.
Not needed if CMOS driver is used.

AC TESTING INPUT, OUTPUT WAVEFORMS



NOTE:
AC Testing Inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS



NOTE:
For Timing Purposes a Port Pin is no longer floating when a 150 mV change from Load Voltage Occurs and Begins to Float when a 150 mV change from the Loading V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} \leq 15$ mA.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
BR— $\overline{BREQ}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
Q— Data Out
R— $\overline{RD}$
W— $\overline{WR}/\overline{WRH}/\overline{WRI}$
X— XTAL1
Y— READY

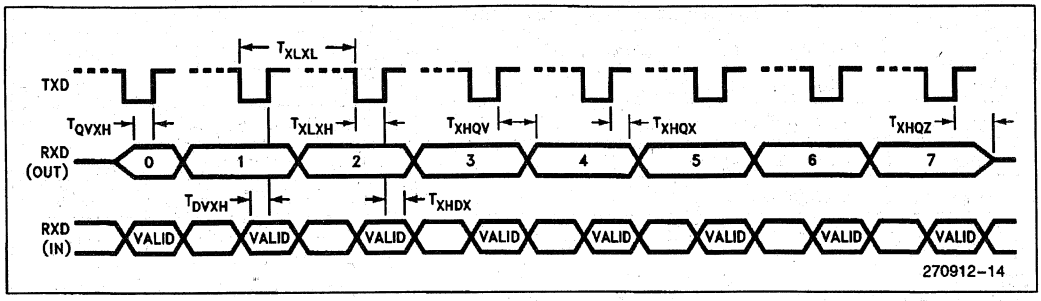
AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE (MODE 0)

SERIAL PORT TIMING—SHIFT REGISTER MODE (Over Specified Operating Conditions)
Test Conditions: Load Capacitance = 100 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 $T_{OSC}-50$	4 $T_{OSC}+50$	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 $T_{OSC}-50$		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 $T_{OSC}+50$	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 $T_{OSC}+200$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE (MODE 0)

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



A TO D

The speed of the A/D converter in the 10-bit or 8-bit modes can be adjusted by setting the AD_TIME special function register to the appropriate value. The AD_TIME register only programs the speed at which the conversions are performed, not the speed it can convert correctly.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

A/D CONVERTER SPECIFICATION

After a conversion is started, the device is placed in the IDLE mode until the conversion is complete. Testing is performed at V_{REF} = 5.12V.

There is an AD_TEST register that allows for conversion on ANGND and V_{REF} as well as zero offset adjustment. The Absolute Error listed is WITHOUT doing any adjustments.

10-BIT A/D OPERATING CONDITIONS(1)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50(2)	V
T_{SAM}	Sample Time	2.0		µs(3)
T_{CONV}	Conversion Time	16.5	19.5	µs(3)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5V.
3. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical (1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3	LSBs
Differential Non-Linearity		> −0.5	+0.5	LSBs
Channel-to-Channel Matching	±0.1	0	±1	LSBs
Repeatability	±0.25	0		LSBs
Temperature Coefficients: Offset Fullscale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	1.2K	Ω(4)
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V
Sampling Capacitor	2			pF
DC Input Leakage		0	±3	µA

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal multiplexer, to sample capacitor.

8-BIT A/D OPERATING CONDITIONS(1)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature **Commercial** Temp.	0	+70	°C
T_A	Ambient Temperature **Extended** Temp.	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50(2)	V
T_{SAM}	Sample Time	2.0		µs(3)
T_{CONV}	Conversion Time	16.5	19.5	µs(3)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5V.
3. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

The 8-bit mode trades off resolution for a faster conversion time. The AD_TIME register must be used when performing an 8-bit conversion.

Parameter	Typ(1)	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±2	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±2	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB(2, 3)	
Feedthrough	−60			dB(2)	
V_{CC} Power Supply Rejection	−60			dB(2)	
Input Series Resistance		750	1.2K	Ω	
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V	
Sampling Capacitor	2			pF	
DC Input Leakage		0	±3	µA	

NOTES:
*An "LSB", as used here, has a value of approximately 20 mV.
1. Typical values are expected for most devices at 25°C.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. Resistance from device pin, through internal multiplexer, to sample capacitor.

OTPROM PROGRAMMING

OPERATING CONDITIONS DURING PROGRAMMING(3)

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	$\overline{EA}$ Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).

AC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Description	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(1)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTE:
1. This specification is for the word dump mode. For programming pulses use 100 µs.

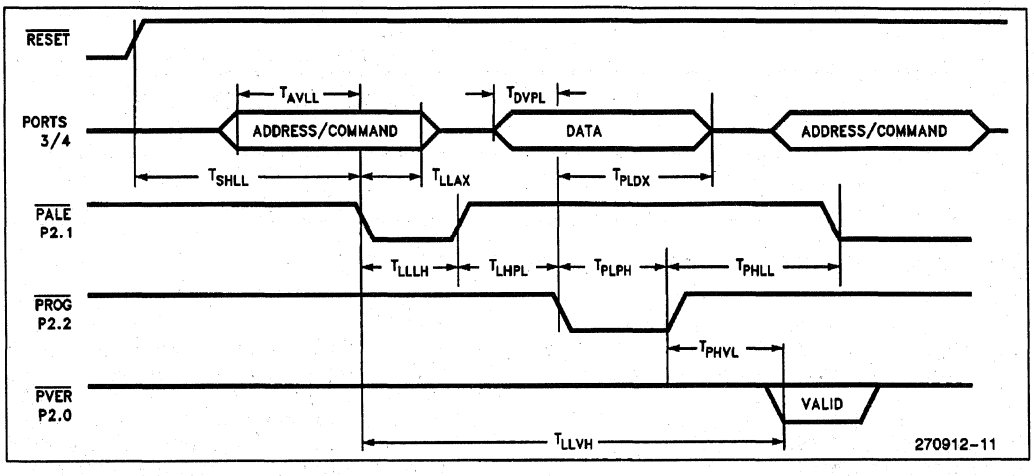
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		100	mA

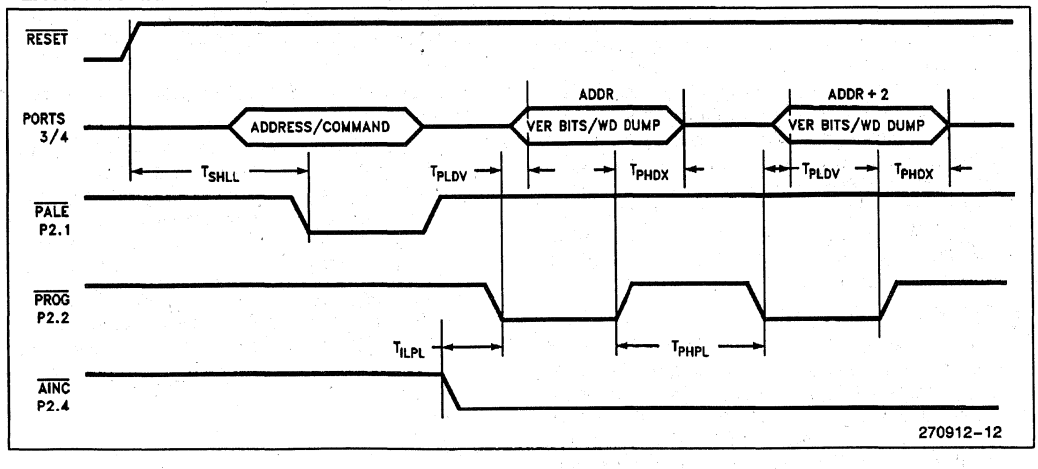
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

OTPROM PROGRAMMING WAVEFORMS

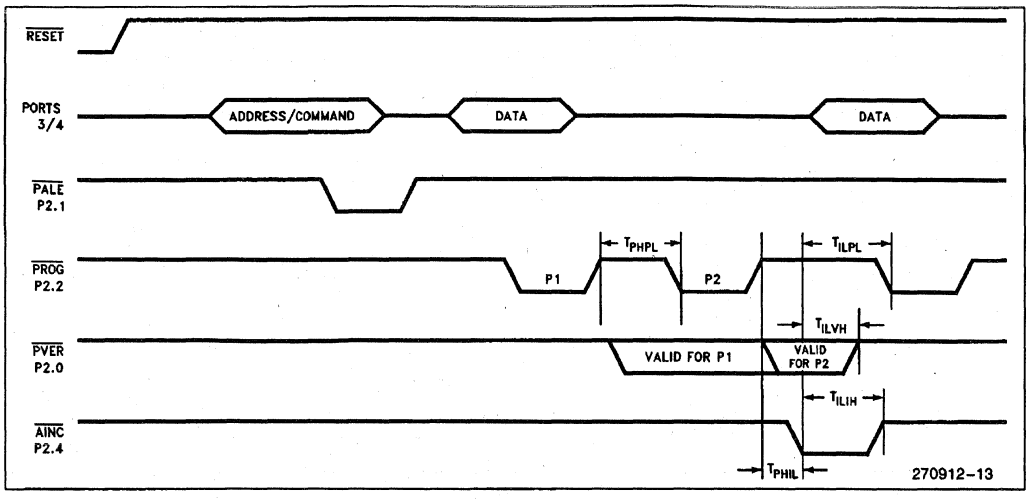
SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



SLAVE PROGRAMMING MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT



SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



87C196KR/87C196JR ERRATA

1. **I_{0H2}**

   Current devices do not meet the test condition for V_{OH2} of -15 μA. Instead the devices are guaranteed to source a minimum of -6 μA.

87C196KR/87C196JR DESIGN CONSIDERATIONS

1. **EPA Timers**

   Special care must be taken when resetting/writing the EPA timers. This is more of a software technique than a device errata. For example: The EPA timers do not generate a "time valid" signal when the counter is either reset or written. This means that if a compare event is programmed in the EPA/Compare channel for a value of "0000H" (when reset) or equal to a written value, the compared event will NOT happen. However, if the timers are allowed to increment/decrement to that value, that compare event WILL occur.

2. **Port 6.4, 6.5, 6.6, 6.7**

   The user is not allowed to modify the P6__REG register when these pins are configured as Special Function P6__MODE.x = 1). During software manipulation of these registers, it is a good practice to first change the P6__MODE register, then modify the P6__REG register when switching from SF to LSIO.

3. **P2.7 (CLKOUT)**

   Port 2.7 (CLKOUT) does not operate in open drain mode.

4. Current versions of the 8XC196KQ/JQ are fabricated with 16K of internal OTPROM, 512 bytes of register RAM, and 256 bytes of internal RAM. The memory map of the 8XC196KQ/JQ is identical to the 8XC196KR/JR. However, the extra memory locations are not tested and should not be used. Intel may disable this extra memory on future versions of the 8XC196KQ/JQ. Any software that relies on reading or writing these locations may not function correctly on future devices.

   Two steps the user should always incorporate to insure future compatibility are:

   A) The program must contain a jump to a location greater than 16K before the 12K boundary is reached. This is necessary only if greater than 12K of program memory is required and portions of the program executes from internal OTPROM.

   B) Use program memory from 12K to 16K only if $\overline{EA}$ is tied to ground. Never use data memory from 180H to 1FFH or from 480H to 4FFH.

52-LEAD DEVICES

Intel offers a 52-lead version of the 87C196KR device: the 87C196JR and 87C196JQ devices.

It is important to point out some functionality differences because of future devices or to remain software consistent with the 68-lead device. Because of the absence of pins on the 52-lead device some functions are not supported.

52-Lead Unsupported Functions:
- Analog Channels 0 and 1
- INST Pin Functionality
- SLPINT Pin Support
- HLD/HLDA Functionality
- External Clocking/Direction of Timer1
- WRH or BHE Functions
- Dynamic Buswidth
- Dynamic Wait State Control

The following is a list of recommended practices when using the 52-lead device:

(1) **External Memory.** Use an 8-bit bus mode only. There is neither a WRH or BUSWIDTH pin. The bus cannot dynamically switch from 8- to 16-bit or vice versa. Set the CCB bytes to an 8-bit only mode, using WR function only.

(2) **Wait State Control.** Use the CCB bytes to configure the maximum number of wait states. If the READY pin is selected to be a system function, the device will lockup waiting for READY. If the READY pin is configured as LSIO (default after RESET), the internal logic will receive a logic "0" level and insert the CCB defined number of wait states in the bus cycle. DON'T USE IRC = "111".

(3) **NMI Support.** The NMI is not bonded out. Make the NMI vector at location 203Eh vector to a Return instruction. This is for glitch safety protection only.

(4) **Auto-Programming Mode.** The 52-lead device will ONLY support the 16-bit zero wait state bus during auto-programming.

(5) **EPA4 through EPA7.** Since the JR and JQ devices use the KR silicon, these functions are in the device, just not bonded out. A programmer can use these as compare only channels or for other functions like software timer, start and A/D, or reset timers.

(6) **Slave Port Support.** The Slave port can still be used on the 52-lead devices. The only function removed is the SLPINT output function.

(7) **Port Functions.** Some port pins have been removed. P5.7, P5.6, P5.5, P5.1, P6.2, P6.3, P1.4 through P1.7, P2.3, P2.5, P0.0 and P0.1. The Px_REG, Px_MODE, and Px_DIR registers can still be updated and read. The programmer should not use the corresponding bits associated with the removed port pins to conditionally branch in software. Treat these bits as RESERVED.

Additionally, these port pins should be setup internally by software as follows:

1. Written to Px_REG as "1" or "0".
2. Configured as Push/Pull, Px_DIR as "0".
3. Configured as LSIO.

This configuration will effectively strap the pin either high or low. *DO NOT Configure as Open Drain output "1", or as an Input pin. This device is CMOS.*

REVISION HISTORY

This data sheet (270912-003) supercedes 270912-002 and is valid for devices with a "C" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify that you have the latest version before finalizing a design or ordering devices.

1. Removed the following errata:
   - Slave Programming Mode
   - EPA__MASK1/EPA__PEND1
   - BMOVI
   - PTS and Other Interrupts
   - Serial Port Framing Error
   - Remap Mode on EPA3
   - A/D Abort
   - PTS/NMI Conflict
   - Data Output Register Cleared
   - Divide Error during HOLD/READY
   - SIO Mode 0
   - EPAIPV Multiplied by Two
   - (These were fixed on the C-step)
2. Moved the following from Errata to Design Considerations:
   - EPA Timers
   - Port 6.4, 6.5, 6.6, 6.7 (and reworded)
   - P2.7 (CLKOUT)
   - Oscillator Noise Sensitivity
3. Added New Errata:
   - I_{OH2} (also existed on A-step)
4. Added SLPCS to Package Diagrams and Pin Descriptions
5. Added T_{BVLL}
6. Added I_{IH} for NMI
7. Added notes to AC Characteristics identifying specifications that do not apply to JR/JQ
8. Changed T_{CLLH} from −5 ns to −10 ns under HOLD/HLDA Timings
9. Changed T_{HVCH} from 55 ns to 65 ns
10. Changed T_{AZHAL} from 10 ns to 25 ns
11. Changed T_{BZHAL} from 10 ns to 25 ns
12. Changed I_{CC} (max) from 70 mA to 75 mA
13. Changed I_{CC} formula from (3.88 × Freq + 8.43) to (3.88X Freq + 13.43)
14. Changed V_{OH2} test point from −50 µA to −15 µA
15. Changed Note 1 in DC parameters
16. Changed External Clock min/max, high/low times from percentage to ratio of T_{OSC}
17. Removed NMI from standard inputs (Note 2 under DC Characteristics)
18. Removed V_{OL1} spec
19. Removed T_{CLBV}
20. Added JQ/KQ design consideration

Data sheet 270912-002 supercedes 270912-001 and is valid for devices with an "A" at the end of the topside tracking number.

1. Removed:
   - CPU features descriptions
   - Peripheral features descriptions
   - SFR Operation (placed in Quick Reference)
   - SFR Maps (placed in Quick Reference)
   - SFR Bit Maps (placed in Quick Reference)
   - I_{IL} in DC Characteristics
   - T_{CLHAL} Max and T_{CLBRH} Max
   - Incorrect Sample and Convert time table from 8-bit A/D
2. Added:
   - Express options
   - Bullets on front page
   - Memory Map
   - Process Information
   - Prefix Identification
   - Thermal Characteristics
   - Programming functions to pin-out and pin descriptions
   - Ambient Temperature under Bias to Absolute Maximum Ratings
   - Note relating to Power Dissipation in Absolute Maximum Rating
   - Notes 8 and 9 to DC Characteristics
   - T_{CLBV} to AC Characteristics
   - Title to Buswidth timing diagram
   - T_{YLYH} to Buswidth timing diagram
   - Hold latency spec
   - External Crystal Connection diagram
   - External Clock Connection diagram
   - 10-bit A/D Operating Conditions Table
   - Title to 10-bit and 8-bit mode A/D Characteristics
   - Voltage on Analog Input Pin specification
   - Sampling Capacitor typical value
   - Note 4 to 10-bit and 8-bit A/D Specifications
   - 8-bit A/D Operating Conditions Table

Off Isolation, Feedthrough, V_{CC} Power Supply Rejection, Input Series Resistance, Voltage on Analog Input Pin, Sampling Capacitor and DC Input Leakage to 8-bit A/D specifications

Notes 1, 2 and 3 to EPROM Programming Conditions

New Errata (Items 10 to 16)

3. Changed:

Title of data sheet from "8XC196KR/KQ/JR/JQ 16-BIT HIGH PERFORMANCE CHMOS MICROCONTROLLER" to "8XC196KR/KQ/JR/JQ COMMERCIAL/EXPRESS CHMOS MICROCONTROLLER"

Several bullets on cover sheet

Register RAM numbers in table on front page to match device

Operating conditions to tabular format

Note 1 in DC Characteristics to include Ports 3 and 4

0 to V_{SS} for I_{LI} and I_{LI1} in DC Characteristics

Format of symbols in AC Characteristics

T_{CLCH} to T_{CLLH} in System Bus Timing diagram

T_{XLXL} Max from 286 ns to 250 ns

T_{XHXX} from T_{OSC} − 44 ns to 35%/65%

T_{XLXX} from T_{OSC} − 44 ns to 35%/65%

T_{XLXH} from T_{OSC} − 50 ns to 10 ns

T_{XHXL} from T_{OSC} − 50 ns to 10 ns

AC Testing Input, Output Waveform

Introductory text on A to D Characteristics and Converter Specification

DC Input Leakage from ±1 μA to ±3 μA in A/D Specifications.

Power Dissipation from 0.5W to 1.0W.

Wording in Float Waveform from 100 mV to 150 mV.

EPROM Programming Characteristics to Operating Conditions table.

Data sheet (270912-001) is valid for devices with an "A" at the end of the topside tracking number. This is the first version of the data sheet.

8XC196NT
CHMOS MICROCONTROLLER WITH 1 MBYTE LINEAR ADDRESS SPACE

- 20 MHz Operation
- High Performance CHMOS 16-Bit CPU
- Up to 32 Kbytes of On-Chip OTPROM
- Up to 1 Kbyte of On-Chip Register RAM
- Up to 512 Bytes of Internal RAM
- Register-Register Architecture
- 4 Channel/10-Bit A/D with Sample/Hold
- 37 Prioritized Interrupt Sources
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port
- Dedicated Baud Rate Generator
- Interprocessor Communication Slave Port
- Selectable Bus Timing Modes for Flexible External Memory Interfacing
- Oscillator Fail Detection Circuitry
- High Speed Peripheral Transaction Server (PTS)
- Two Dedicated 16-Bit High-Speed Compare Registers
- 10 High Speed Capture/Compare (EPA)
- Full Duplex Synchronous Serial I/O Port (SSIO)
- Two Flexible 16-Bit Timer/Counters
- Quadrature Counting Inputs
- Flexible 8-/16-Bit External Bus (Programmable)
- Programmable Bus (HOLD/HLDA)
- 1.4 μs 16 x 16 Multiply
- 2.4 μs 32/16 Divide
- 68-Pin Package

Device	Pins/Package	OTPROM	Reg RAM	Code RAM	Address Space	I/O	EPA	A/D
8XC196NT	68P PLCC	32K	1K	512	1 Mbyte	56	10	4

X = 7 OTPROM Device
X = 0 ROMLESS

The 8XC196NT 16-bit microcontroller is a high performance member of the MCS® 96 microcontroller family. The 8XC196NT is an enhanced 8XC196KR device with 1 Mbyte of linear address space, 1000 bytes of register RAM, 512 bytes of internal RAM, 20 MHz operation and an optional 32 Kbytes of OTPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

Ten high-speed capture/compare modules are provided. As capture modules event times with 200 ns resolution can be recorded and generate interrupts. As compare modules events such as toggling of a port pin, starting an A/D conversion, pulse width modulation, and software timers can be generated. Events can be based on the timer or up/down counter.

December 1996

Order Number: 272267-005

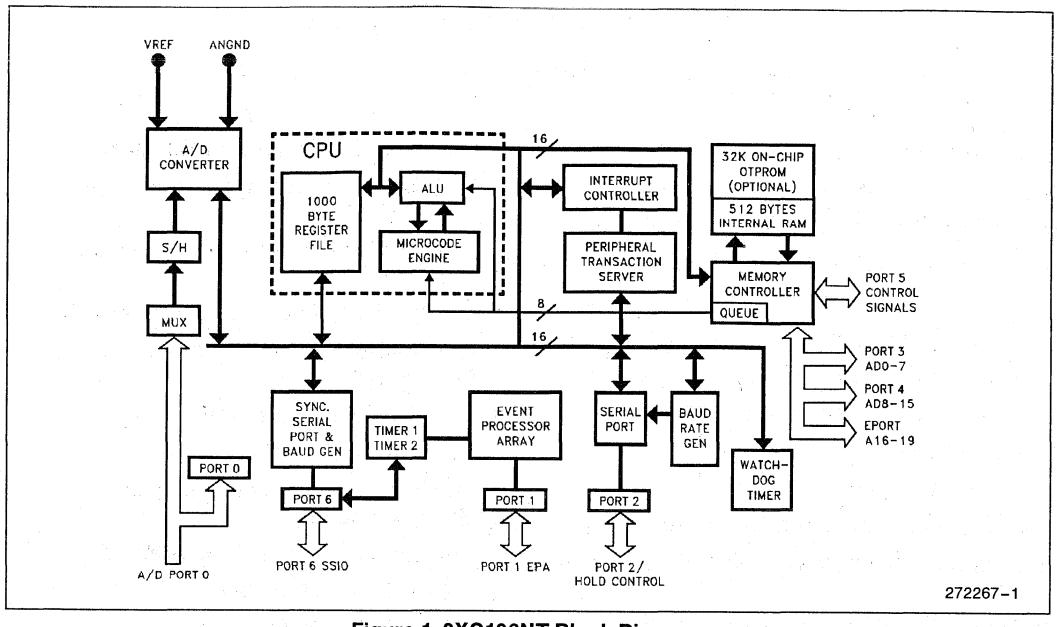


Figure 1. 8XC196NT Block Diagram

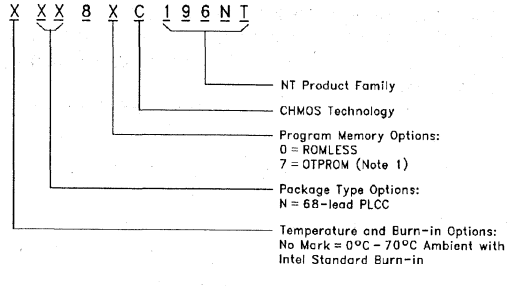
PROCESS INFORMATION

This device is manufactured on P629.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
PLCC	36.5°C/W	13°C/W



EXAMPLE: N87C196NT is 68-Lead PLCC OTPROM.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

Figure 2. The 8XC186NT Familiy Nomenclature

8XC196NT Memory Map

Address (Note 7)	Description
FFFFFFH FFA000H	External Memory
FF9FFFH FF2080H	Internal OTPROM or External Memory (Determined by $\overline{EA}$ Pin) RESET at FF2080H
FF207FH FF2000H	Reserved Memory (Internal OTPROM or External Memory) (Determined by $\overline{EA}$ Pin)
FF1FFFH FF0600H	External Memory
FF05FFH FF0400H	Internal RAM (Identically Mapped into 00400H–005FFH)
FF03FFH FF0100H	External Memory
FF00FFH FF0000H	Reserved for ICE
FEFFFFH 100000H	External Memory for future devices
FFFFFH 00A000H	984 Kbytes External Memory
009FFFH 002080H	Internal OTPROM or External Memory (Note 1)
00207FH 002000H	Reserved Memory (Internal OTPROM or External Memory) (Notes 1, 3, and 6)
001FFFH 001FE0H	Memory Mapped Special Function Registers (SFR's)
001FDFH 001F00H	Internal Special Function Registers (SFR's) (Note 5)
001EFFH 000600H	External Memory
0005FFH 000400H	Internal RAM (Address with Indirect or Indexed Modes)
0003FFH 000100H	Register RAM — Upper Register File (Address with Indirect or Indexed Modes or through Windows.) (Note 2)
0000FFH 000018H	Register RAM — Lower Register File (Address with Direct, Indirect, or Indexed Modes.) (Notes 2, 4)
000017H 000000H	CPU SFR's — Lower Register File (Address with Direct, Indirect, or Indexed Modes.) (Notes 2, 4)

NOTES:
1. These areas are mapped internal OTPROM if the REMAP bit (CCB2.2) is set and $\overline{EA}$ = 5V. Otherwise they are external memory.
2. Code executed in locations 00000H to 003FFH will be forced external.
3. Reserved memory locations must contain 0FFH unless noted.
4. Reserved SFR bit locations must be written with 0.
5. Refer to 8XC196NT User's Guide and Quick Reference for SFR descriptions.
6. **WARNING:** The contents or functions of reserved memory locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.
7. The 8XC196NT internally uses 24 bit address, but only 20 address lines are bonded out allowing 1 Mbyte external address space.

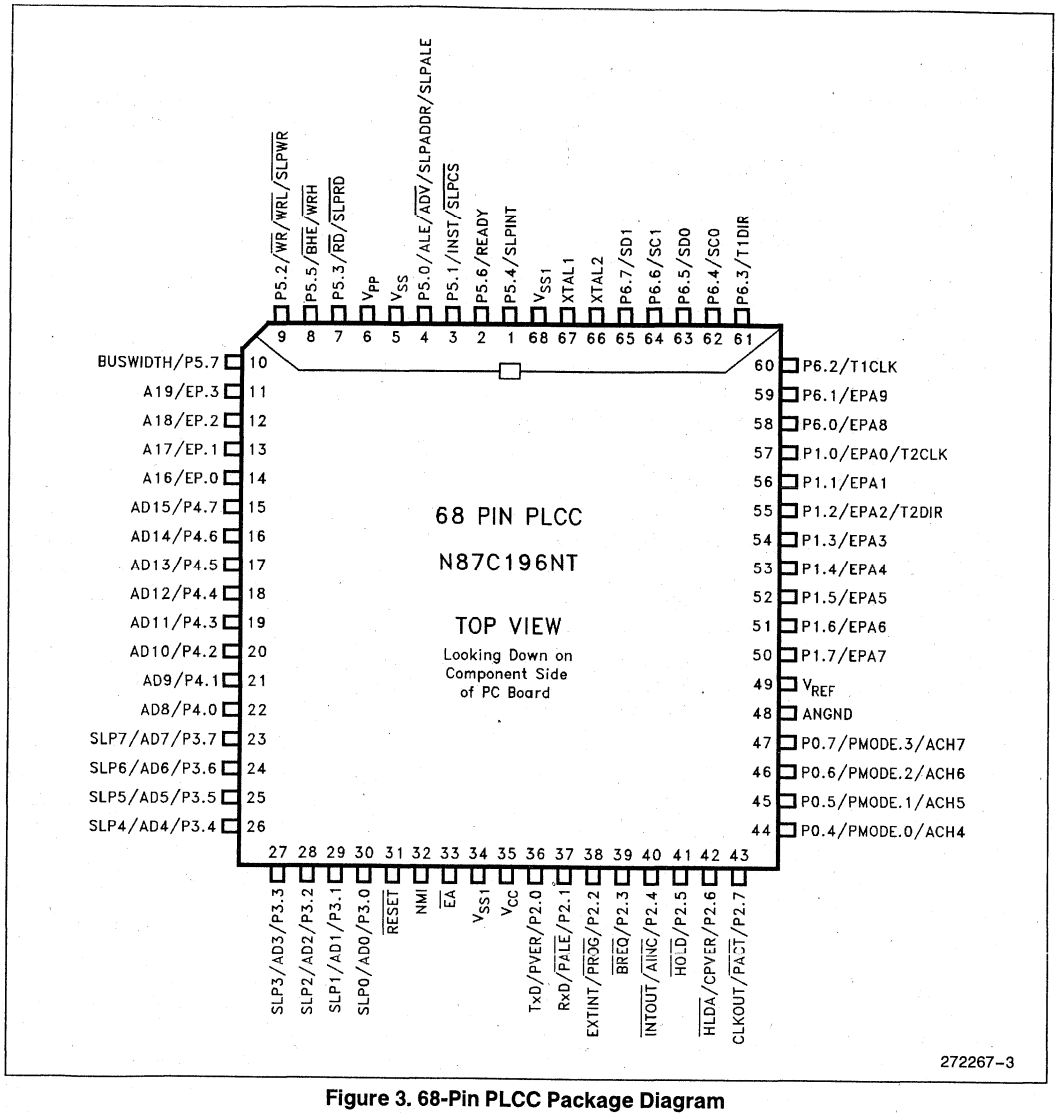


Figure 3. 68-Pin PLCC Package Diagram

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (+5V).
V_{SS}, V_{SS1}, V_{SS1}	Digital circuit ground (0V). There are multiple V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the OTPROM parts. It should be +12.5V for programming. It is also the timing pin for the return from powerdown circuit. Connect to V_{CC} if powerdown not being used.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P2.7/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin.
$\overline{\text{RESET}}$	Reset input to and open-drain output from the chip. $\overline{\text{RESET}}$ has an internal pullup.
P5.7/BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dyamically controls the Buswidth of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs, if BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is "0" and CCR1 bit 2 is "1", all bus cycles are 8-bit, if CCR bit 1 is "1" and CCR1 bit 2 is "0", all bus cycles are 16-bit. CCR bit 1 = "0" and CCR1 bit 2 = "0" is illegal. Also an LSIO pin when not used as BUSWIDTH.
NMI	A positive transition causes a non maskable interrupt vector through memory location 203EH.
P5.1/INST/$\overline{\text{SLPCS}}$	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal OTPROM fetches INST is held low. Also LSIO when not INST. $\overline{\text{SLPCS}}$ is the Slave Port Chip Select.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a high causes memory accesses to locations 0FF2000H through 0FF9FFFH to be directed to on-chip OTPROM. $\overline{\text{EA}}$ equal to a low causes accesses to these locations to be directed to off-chip memory. $\overline{\text{EA}}$ = +12.5V causes execution to begin in the Programming Mode. $\overline{\text{EA}}$ is latched at reset.
$\overline{\text{HOLD}}$	Bus Hold Input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
P5.0/ALE/$\overline{\text{ADV}}$/ SLPADDR/ SLPALE	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive (high) at the end of the bus cycle. $\overline{\text{ADV}}$ can be used as a chip select for external memory. ALE/$\overline{\text{ADV}}$ is active only during external memory accesses. Also LSIO when not used as ALE. SLPADDR is the Slave Port Address Control Input and SLPALE is the Slave Port Address Latch Enable Input.
P5.3/$\overline{\text{RD}}$/$\overline{\text{SLPRD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is active only during external memory reads or LSIO when not used as $\overline{\text{RD}}$. $\overline{\text{SLPRD}}$ is the Slave Port Read Control Input.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
P5.2/WR/WRL/SLPWR	Write and Write Low output to external memory, as selected by the CCR, WR will go low for every external write, while WRL will go low only for external writes where an even byte is being written. WR/WRL is active during external memory writes. Also an LSIO pin when not used as WR/WRL. SLPWR is the Slave Port Write Control Input
P5.5/BHE/WRH	Byte High Enable or Write High output, as selected by the CCR. BHE = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, BHE = 1), to the high byte only (A0 = 1, BHE = 0) or both bytes (A0 = 0, BHE = 0). If the WRH function is selected, the pin will go low if the bus cycle is writing to an odd memory location. BHE/WRH is only valid during 16-bit external memory read/write cycles. Also an LSIO pin when not BHE/WRH.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/CCR1. Also an LSIO pin when READY is not selected.
P5.4/SLPINT	Dual function I/O pin. As a bidirectional port pin or as a system function. The system function is a Slave Port Interrupt Output Pin.
P6.2/T1CLK	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Clock input. The TIMER1 will increment or decrement on both positive and negative edges of this pin.
P6.3/T1DIR	Dual function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Direction input. The TIMER1 will increment when this pin is high and decrements when this pin is low.
PORT1/EPA0–7 P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have yet another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH4–7	4-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to OTPROM parts to select the Programming Mode.
P6.3–6.7/SSIO	Dual function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
EPORT	8-bit bidirectional standard and I/O port. These bits are shared with the extended address bus, A16–A19. Pin function is selected on a per pin basis.
INTOUT	Interrupt Output. This active-low output indicates that a pending interrupt requires use of the external bus.
SLP0–SLP7	Slave Port Address/Data Bus

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −60°C to +150°C

Voltage from V_{PP} or $\overline{EA}$ to V_{SS} or ANGND ..... −0.5V to +13.0V

Voltage from Any Other Pin to V_{SS} or ANGND ..... −0.5 to +7.0V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation..... 0.5W

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	4	20	MHz (Note 4)

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC CHARACTERISTICS (Under Listed Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current			90	mA	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$ (While device in Reset)
I_{REF}	A/D Reference Supply Current			5	mA	
I_{IDLE}	Idle Mode Current			40	mA	XTAL1 = 20 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{PD}	Powerdown Mode Current(6)		50	75	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$(11)
V_{IL}	Input Low Voltage (all pins)	−0.5V		0.3 V_{CC}	V	For PORT0(10)
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	For PORT0(10)
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	XTAL1 Input Pin Only(1)
V_{IH2}	Input High Voltage on RESET	0.7 V_{CC}		V_{CC} + 0.5	V	RESET input pin only
V_{OL}	Output Low Voltage (Outputs Configured as Complementary)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA(3,5) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Outputs Configured as Complementary)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200µA(3,5) I_{OH} = −3.2 mA I_{OH} = −7.0 mA
I_{LI}	Input Leakage Current (Std. Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
I_{LI1}	Input Leakage Current (Port 0)			±3	µA	$V_{CC} < V_{IN} < V_{REF}$
I_{IL}	Logical 0 Input Current			−70	µA	V_{IN} = 0.45V(1)

DC CHARACTERISTICS (Under Listed Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OL1}	Output Low Voltage in RESET			0.8	V	(Note 7)
V_{OH1}	SLPINT (P5.4) and HLDA (P2.6) Output High Voltage in RESET	2.0			V	I_{OH} = 0.8 mA(7)
V_{OH2}	Output High Voltage in RESET	$V_{CC}-1V$			V	I_{OH} = −6 μA(1)
C_S	Pin Capacitance (Any pin to V_{SS})			10	pF	f_{test} = 1.0 MHz
R_{WPU}	Weak Pullup Resistance		150K		Ω	(Note 6)
R_{RST}	Reset Pullup	65K		180K	Ω	

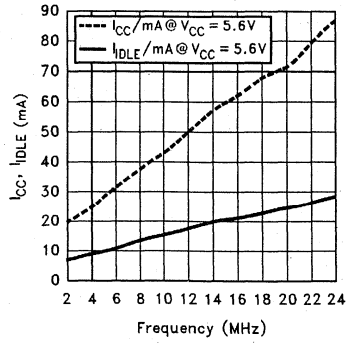
NOTES:
1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5, Port6 and EPORT except SPLINT (P5.4) and HLDA (P2.6).
2. Standard input pins include XTAL1, $\overline{EA}$, RESET, and Port 1/2/5/6 and EPORT when setup as inputs.
3. All bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Maximum I_{DL}/I_{DH} currents per pin are as follows:

   a.) Test Condition: $V_{OH} = V_{CC} - 0.7V$ $V_{OL} = 0.45V$

   Part 1: I_{OL} = 0.65 mA I_{OH} = 7.5 mA
   Part 2: I_{OL} = 8.0 mA I_{OH} = 12.0 mA
   Part 3: I_{OL} = 7.5 mA I_{OH} = 7.5 mA
   Part 4: I_{OL} = 7.5 mA I_{OH} = 7.5 mA
   Part 5: I_{OL} = 9.0 mA I_{OH} = 9.0 mA
   Part 6: I_{OL} = 8.0 mA I_{OH} = 9.0 mA

   b.) Test Condition: $V_{OH} = V_{CC} - 1.5V$ $V_{OL} = 1.5V$

   Part 1: I_{OL} = 21.0 mA I_{OH} = 26.0 mA
   Part 2: I_{OL} = 26.0 mA I_{OH} = 29.0 mA
   Part 3: I_{OL} = 17.0 mA I_{OH} = 25.0 mA
   Part 4: I_{OL} = 16.0 mA I_{OH} = 25.0 mA
   Part 5: I_{OL} = 21.0 mA I_{OH} = 28.0 mA
   Part 6: I_{OL} = 19.0 mA I_{OH} = 26.0 mA
6. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.5V$.
7. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).
8. TBD = To Be Determined.
9. Pullup present during return from powerdown condition.
10. When P0 is used as analog inputs, refer to A/D specifications.
11. For temperatures <100°C typical is 10 μA.



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8XC196NT ADDITIONAL BUS TIMING MODES

The 8XC196NT device has 3 additional bus timing modes for external memory interfacing.

MODE 3:

Mode 3 is the standard timing mode. Use this mode for systems that emulate the 8XC196KR bus timings.

MODE 0:

Mode 0 is the standard timing mode, but 1 (minimum) wait state is always inserted in external bus cycles.

MODE 1:

Mode 1 is the long R/W mode. This mode advances $\overline{RD}$ and $\overline{WR}$ signals by 1 T_{OSC} creating a 2 T_{OSC} $\overline{RD}/\overline{WR}$ low time. ALE is also advanced by 0.5 T_{OSC} but ALE high time remains 1 T_{OSC}.

MODE 2:

Mode 2 is the long R/W mode with Early Address. Mode 2 is similar to Mode 1 with respect to $\overline{RD}$, $\overline{WR}$, and ALE signals. Additionally, the address is output on the bus 0.5 T_{OSC} earlier in the bus cycle.

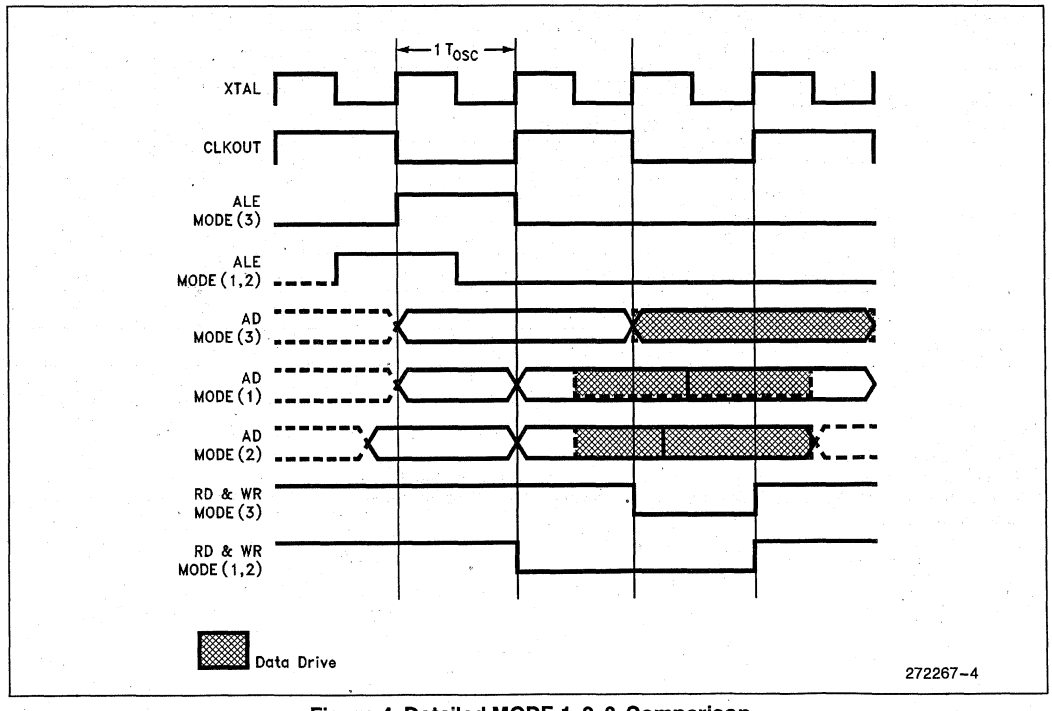


Figure 4. Detailed MODE 1, 2, 3, Comparison

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:
H—High
L—Low
V—Valid
X—No Longer Valid
Z—Floating

Signals:
A—Address
B—$\overline{BHE}$
BR—$\overline{BREQ}$
C—CLKOUT
D—DATA
G—Buswidth
H—$\overline{HOLD}$
HA—$\overline{HLDA}$
L—ALE/$\overline{ADV}$
Q—Data Out
RD—$\overline{RD}$
W—$\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X—XTAL1
Y—READY

BUS MODE 0 and 3—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2T_{OSC} - 75$	ns(3)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2T_{OSC} - 75$	ns(2, 3)
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns(2, 3)
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid		$T_{OSC} - 30$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2T_{OSC} \times n$, where n = number of wait states.
3. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add $2T_{OSC}$ to the specification.

BUS MODE 0 and 3—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

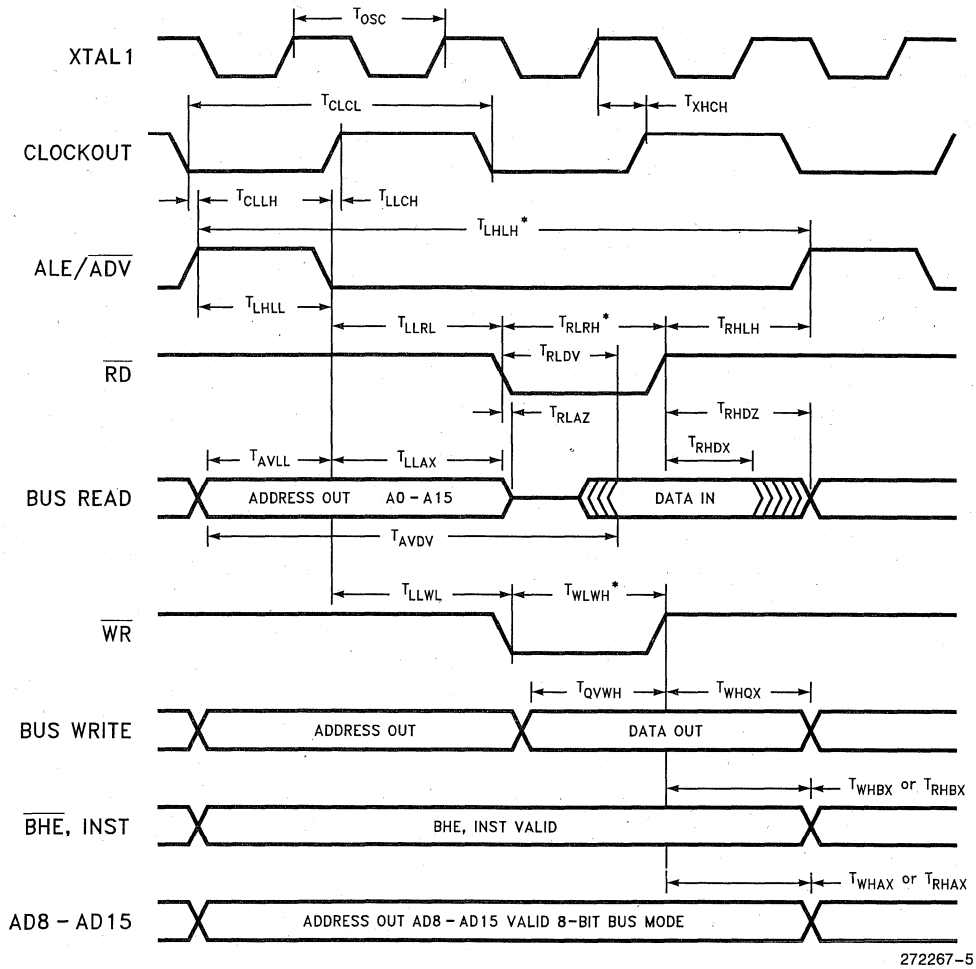
The 8XC196NT will meet these specifications

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{OFD}	Clock Failure to Reset Pulled Low(6)	4	40	μs
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 30	ns
T_{CLLH}	CLKOUT Low to ALE/$\overline{ADV}$ High	−10	+15	ns
T_{LLCH}	ALE/$\overline{ADV}$ Low to CLKOUT High	−25	+15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	T_{OSC} − 40		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	T_{OSC} − 40		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	−5	+35	ns
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	T_{OSC}	T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	−10	+25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{OSC} − 35		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	T_{OSC} − 10	T_{OSC} + 15	ns(3)
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ High	T_{OSC} − 10		ns
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ High	T_{OSC} − 10		ns
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	T_{OSC} − 30		ns(4)

NOTES:

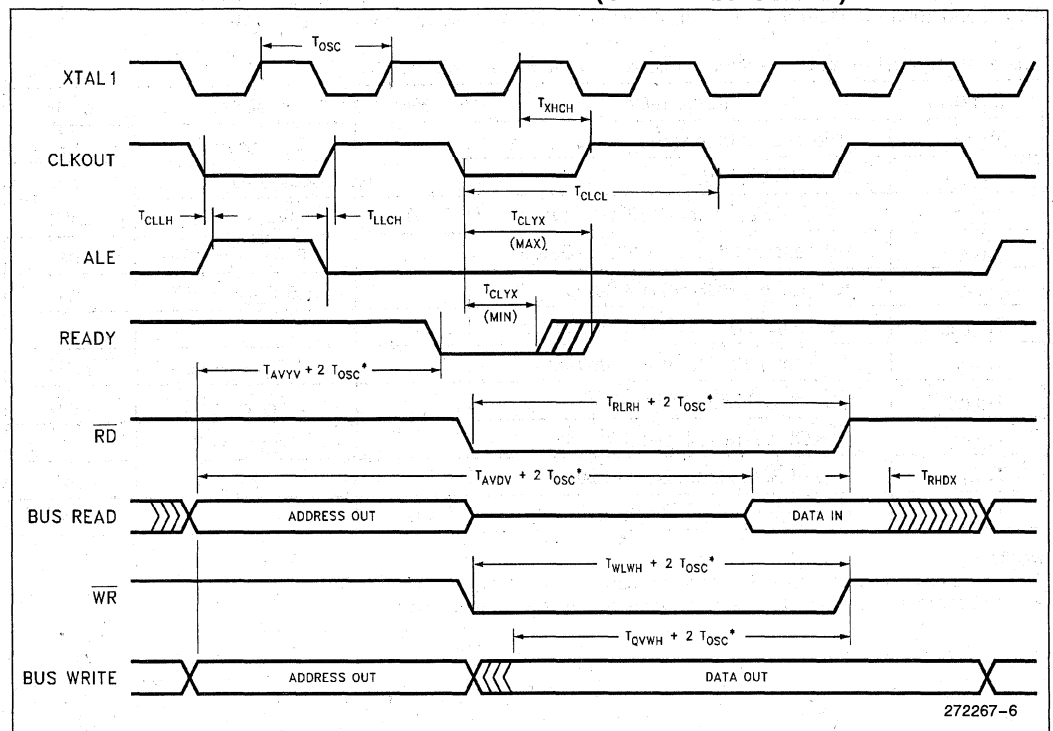
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. NT/NQ customer QROM codes need to equate location 2016H to the value 0CDEH if the oscillator fail detect (OFD) function is desired. Intel manufacturing uses location 2016H as a flag to determine whether or not to program the Clock Detect Enable (CDE) bit. Programming the CDE bit enables oscillator fail detection.

BUS MODE 0 and 3—8XC196NT SYSTEM BUS TIMING



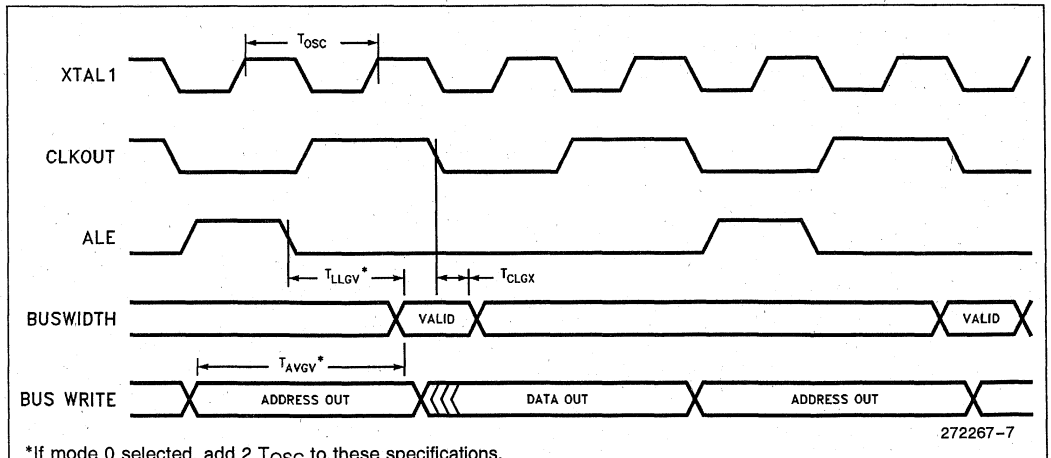
*If mode 0 operation is selected, add 2 T_{OSC} to this time.

8XC196NT MODE 0 and 3—READY TIMINGS (ONE WAIT STATE)



*If mode 0 selected, one wait state is always added. If additional wait states are required, add 2 T_{OSC} to these specifications.

MODE 0 and 3—8XC196NT BUSWIDTH TIMINGS



*If mode 0 selected, add 2 T_{OSC} to these specifications.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2\,T_{OSC} - 75$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2\,T_{OSC} - 75$	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		$1.5\,T_{OSC} - 60$	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3\,T_{OSC} - 60$	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid		$2\,T_{OSC} - 44$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2\,T_{OSC} \times n$, where n = number of wait states.

BUS MODE 1—AC CHARACTERISTICS (Over Specified Operating Conditions)

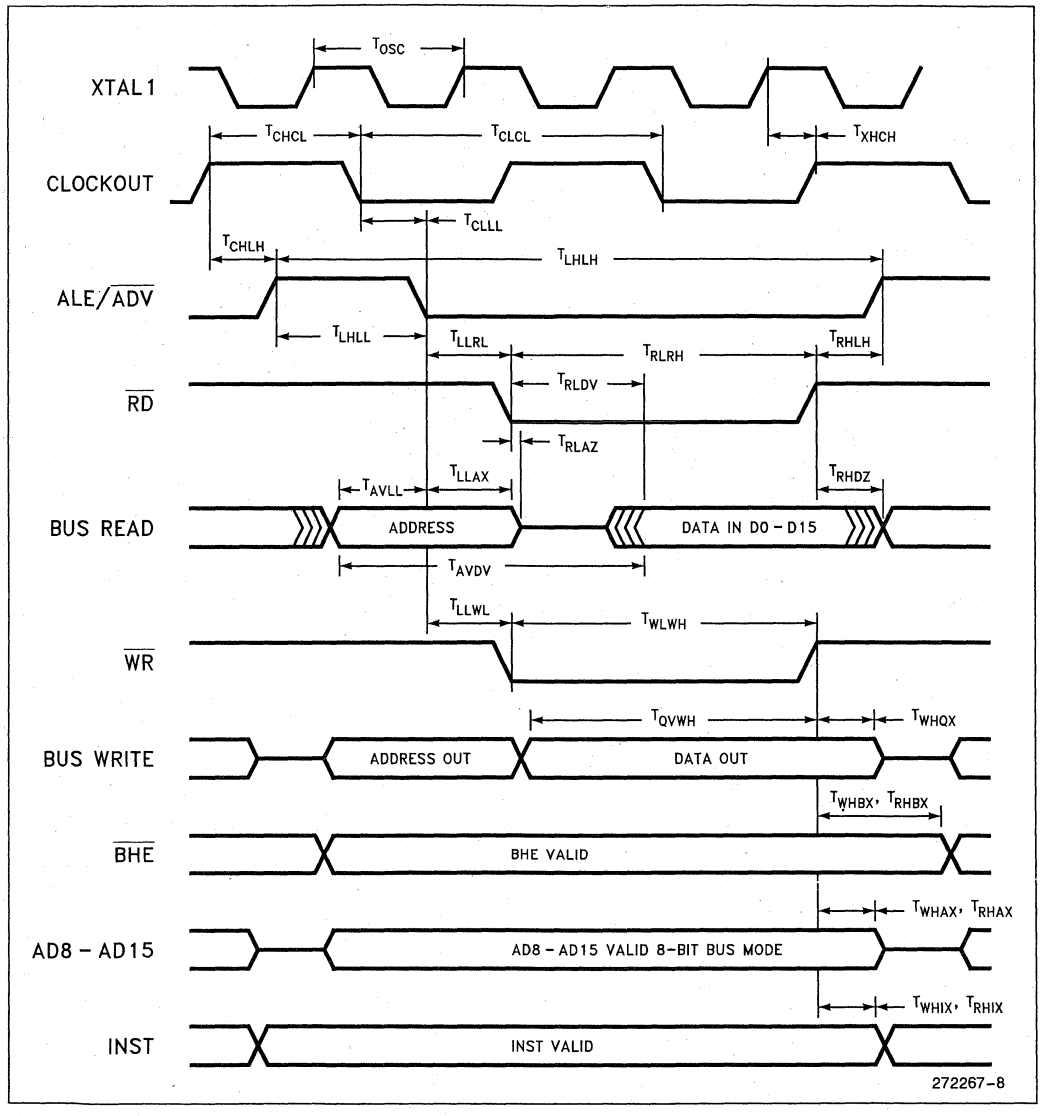
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196NT will meet these specifications

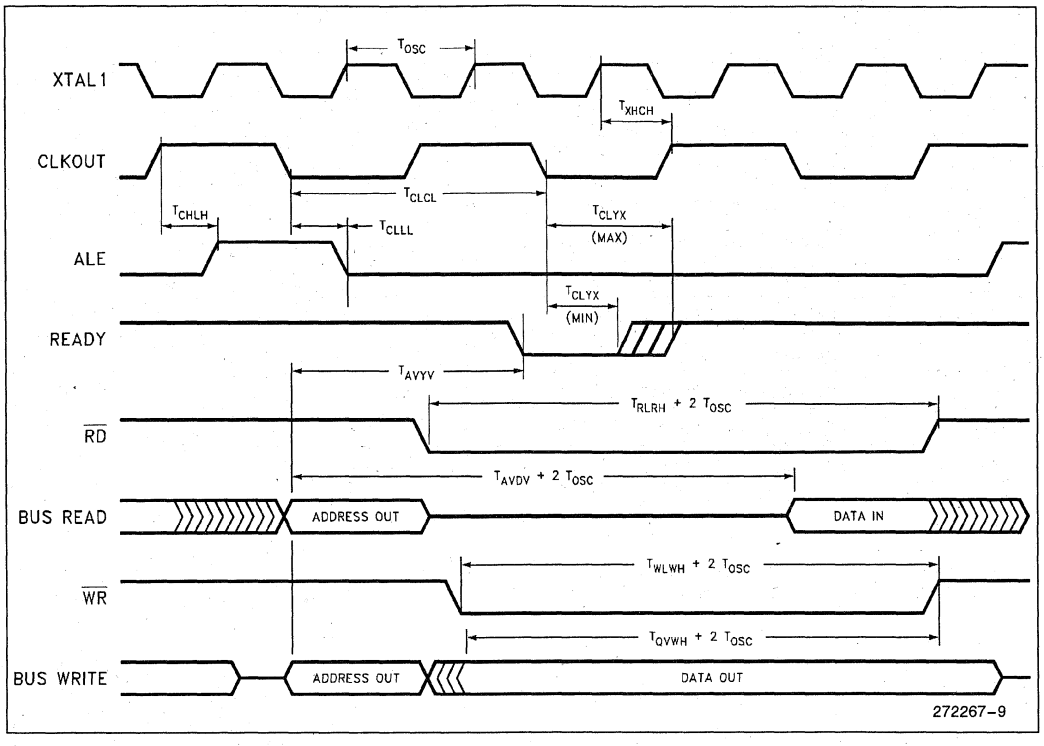
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 15	0.5 T_{OSC} + 15	ns
T_{CLLL}	CLKOUT LOW to ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 20	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	0.5 T_{OSC} − 20		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	0.5 T_{OSC} − 15		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	$\overline{RD}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC}	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	T_{OSC} − 15	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	2 T_{OSC} − 23		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	2 T_{OSC} − 15		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	0.5 T_{OSC} − 12		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 15	ns(3)
T_{WHBX}	$\overline{BHE}$ Hold after $\overline{WR}$ High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after $\overline{WR}$ High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$ Hold after $\overline{RD}$ High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after $\overline{RD}$ High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

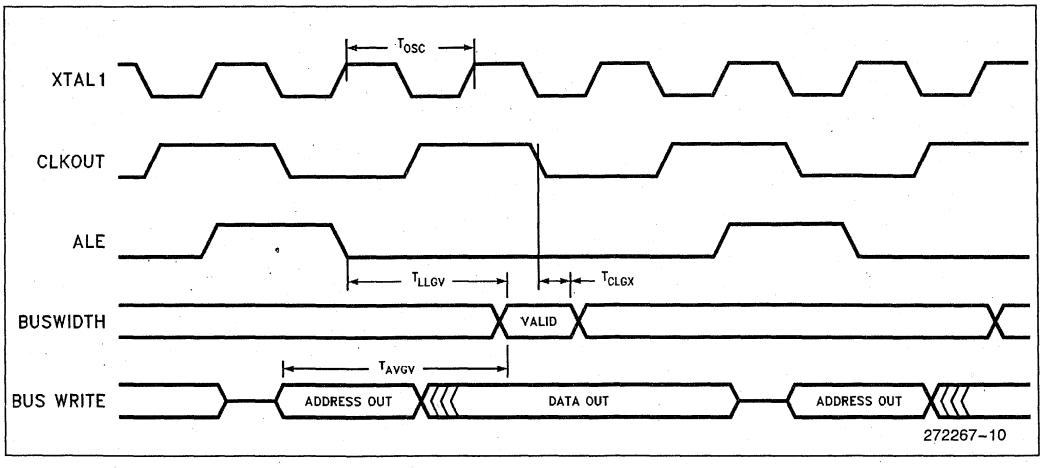
MODE 1—8XC196NT SYSTEM BUS TIMING



MODE 1—8XC196NT READY TIMINGS (ONE WAIT STATE)



MODE 1—8XC196NT BUSWIDTH TIMINGS



BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The system must meet these specifications to work with the 8XC196NT.

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		$2.5\,T_{OSC} - 75$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns(1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2.5\,T_{OSC} - 75$	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		$1.5\,T_{OSC} - 60$	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		$3.5\,T_{OSC} - 55$	ns(2)
T_{RLDV}	$\overline{RD}$ active to input Data Valid		$2\,T_{OSC} - 44$	ns(2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 60$	ns
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$0.5\,T_{OSC}$	ns
T_{RHDX}	Data Hold after $\overline{RD}$ High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2\,T_{OSC} \times n$, where n = number of wait states.

BUS MODE 2—AC CHARACTERISTICS (Over Specified Operating Conditions)

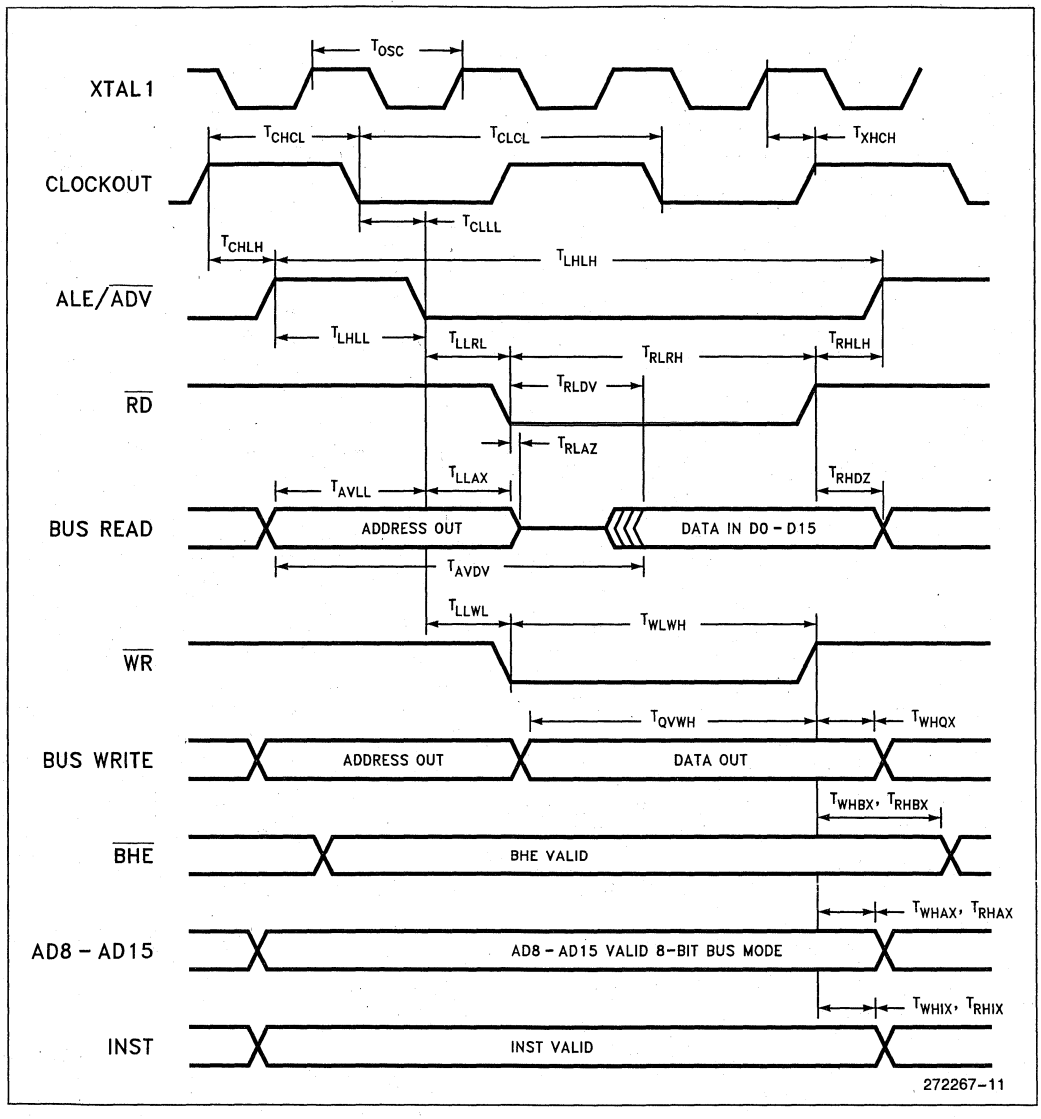
Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

The 8XC196NT will meet these specifications

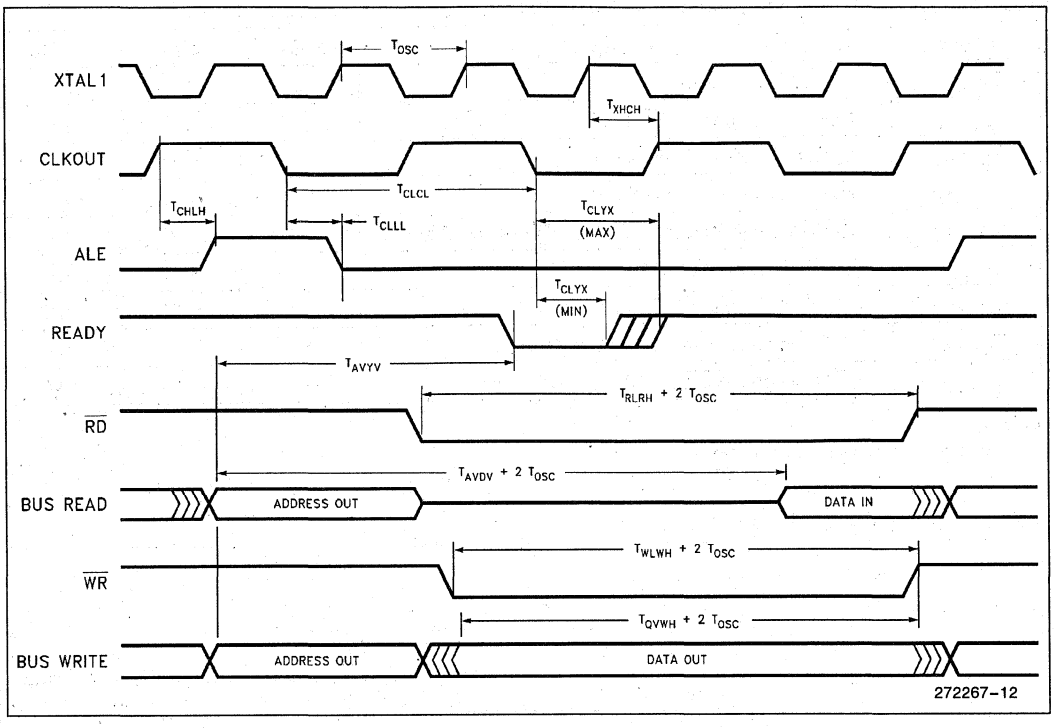
Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8.0	20	MHz(1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	50	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	+85	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 15	0.5 T_{OSC} + 15	ns
T_{CLLL}	CLKOUT LOW to ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/$\overline{ADV}$ Cycle Time	4 T_{OSC}		ns(5)
T_{LHLL}	ALE/$\overline{ADV}$ High Time	T_{OSC} − 20	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} − 15		ns
T_{LLAX}	Address Hold After ALE/$\overline{ADV}$ Low	0.5 T_{OSC} − 20		ns
T_{LLRL}	ALE/$\overline{ADV}$ Low to $\overline{RD}$ Low	0.5 T_{OSC} − 15		ns
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Low	T_{OSC} − 10	T_{OSC} + 30	ns
T_{RLRH}	$\overline{RD}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{RHLH}	$\overline{RD}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 5	0.5 T_{OSC} + 25	ns(3)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		+5	ns
T_{LLWL}	ALE/$\overline{ADV}$ Low to $\overline{WR}$ Low	0.5 T_{OSC} − 10		ns
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Low	T_{OSC} − 22	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before $\overline{WR}$ High	2 T_{OSC} − 25		ns
T_{CHWH}	CLKOUT High to $\overline{WR}$ High	−10	+15	ns
T_{WLWH}	$\overline{WR}$ Low Period	2 T_{OSC} − 20		ns(5)
T_{WHQX}	Data Hold after $\overline{WR}$ High	0.5 T_{OSC} − 12		ns
T_{WHLH}	$\overline{WR}$ High to ALE/$\overline{ADV}$ High	0.5 T_{OSC} − 10	0.5 T_{OSC} + 10	ns(3)
T_{WHBX}	$\overline{BHE}$ Hold after $\overline{WR}$ High	T_{OSC} − 15		ns
T_{WHIX}	INST Hold after $\overline{WR}$ High	0.5 T_{OSC} − 15		
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ High	0.5 T_{OSC} − 30		ns(4)
T_{RHBX}	$\overline{BHE}$ Hold after $\overline{RD}$ High	T_{OSC} − 32		ns
T_{RHIX}	INST Hold after $\overline{RD}$ High	0.5 T_{OSC} − 32		
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ High	0.5 T_{OSC} − 30		ns(4)

NOTES:
1. Testing performed at 8.0 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} × n, where n = number of wait states.

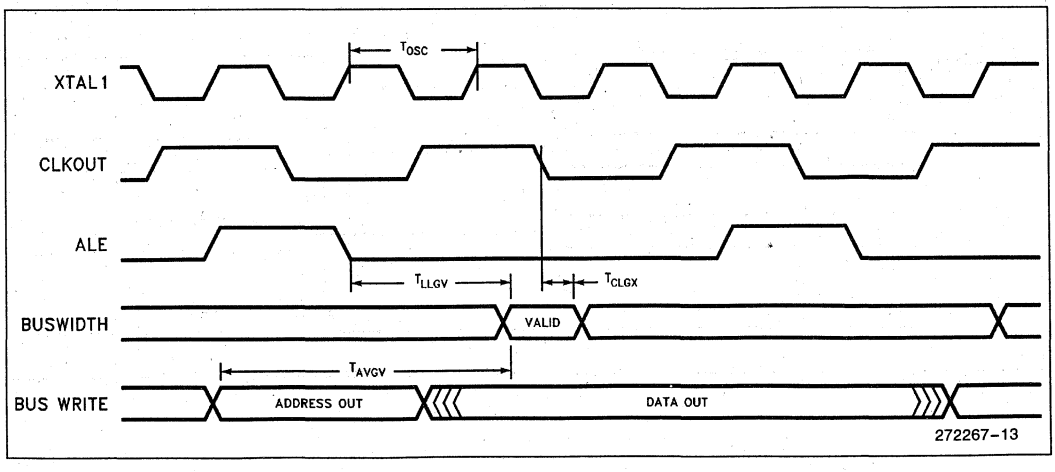
MODE 2—8XC196NT SYSTEM BUS TIMING



MODE 2—8XC196NT READY TIMINGS (ONE WAIT STATE)



MODE 2—8XC196NT BUSWIDTH TIMINGS



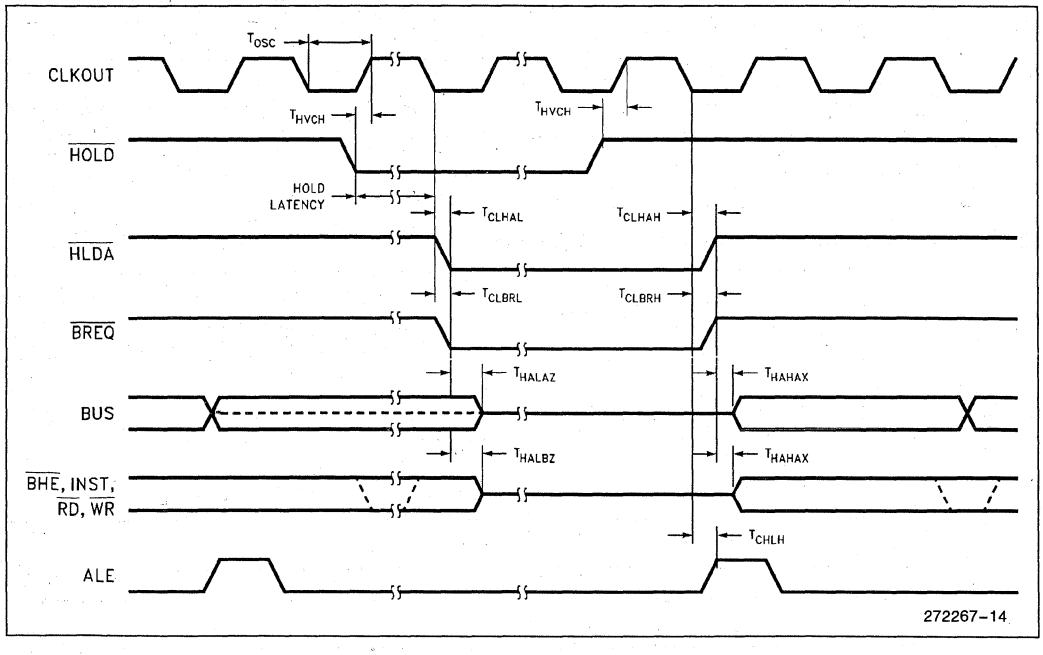
BUS MODE 0, 1, 2, and 3—$\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ TIMINGS (Over Specified Operation Conditions)

Test Conditions: Capacitance Load on All Pins = 100 pF, Rise and Fall Times = 10 ns.

Symbol	Parameter	Min	Max	Units
T_{HVCH}	$\overline{\text{HOLD}}$ Setup Time	+65		ns(1)
T_{CLHAL}	CLKOUT Low to $\overline{\text{HLDA}}$ Low	−15	+15	ns
T_{CLBRL}	CLKOUT Low to $\overline{\text{BREQ}}$ Low	−15	+15	ns
T_{HALAZ}	$\overline{\text{HLDA}}$ Low to Address Float		+25	ns
T_{HALBZ}	$\overline{\text{HLDA}}$ Low to $\overline{\text{BHE}}$, INST, $\overline{\text{RD}}$, $\overline{\text{WR}}$ Weakly Driven		+25	ns
T_{CLHAH}	CLKOUT Low to $\overline{\text{HLDA}}$ High	−25	+15	ns
T_{CLBRH}	CLKOUT Low to $\overline{\text{BREQ}}$ High	−25	+25	ns
T_{HAHAX}	$\overline{\text{HLDA}}$ High to Address No Longer Float	−15		ns
T_{HAHBV}	$\overline{\text{HLDA}}$ High to $\overline{\text{BHE}}$, INST, $\overline{\text{RD}}$, $\overline{\text{WR}}$ Valid	−10		ns

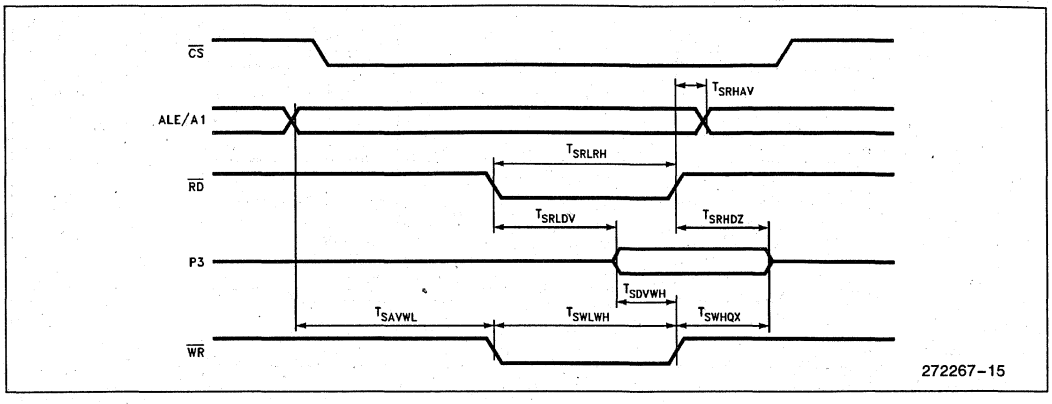
NOTE:
1. To guarantee recognition at next clock.

8XC196NT $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ TIMINGS



AC CHARACTERISTICS—SLAVE PORT

SLAVE PORT WAVEFORM—(SLPL = 0)



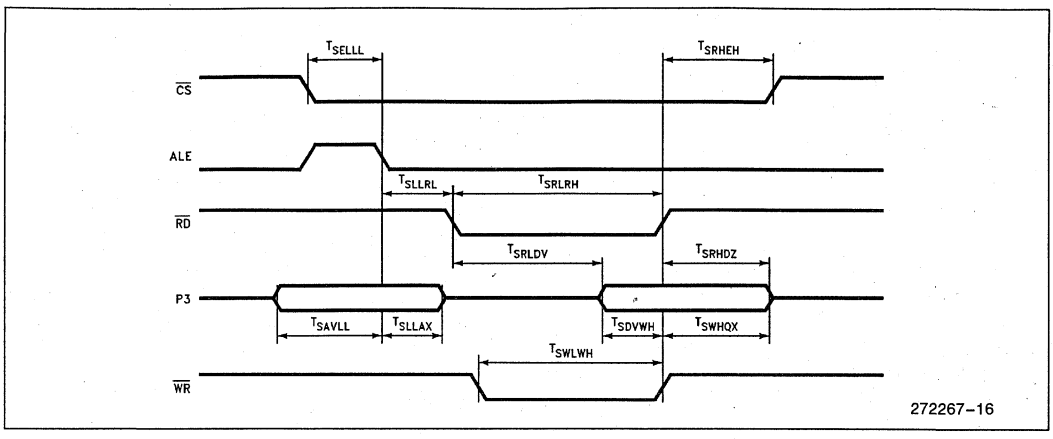
SLAVE PORT TIMING—(SLPL = 0)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to $\overline{WR}$ Low	50		ns
T_{SRHAV}	$\overline{RD}$ High to Address Valid	60		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 50 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

AC CHARACTERISTICS—SLAVE PORT (Continued)

SLAVE PORT WAVEFORM—(SLPL = 1)



SLAVE PORT TIMING—(SLPL = 1)

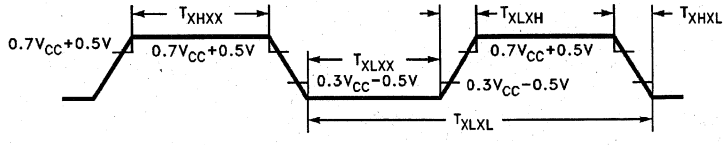
Symbol	Parameter	Min	Max	Units
T_{SELLL}	$\overline{CS}$ Low to ALE Low	20		ns
T_{SRHEH}	$\overline{RD}$ or $\overline{WR}$ High to $\overline{CS}$ High	60		ns
T_{SLLRL}	ALE Low to $\overline{RD}$ Low	T_{OSC}		ns
T_{SRLRH}	$\overline{RD}$ Low Period	T_{OSC}		ns
T_{SWLWH}	$\overline{WR}$ Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	$\overline{RD}$ Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to $\overline{WR}$ High	20		ns
T_{SWHQX}	$\overline{WR}$ High to Data Invalid	30		ns
T_{SRHDZ}	$\overline{RD}$ High to Data Float	15		ns

NOTES:
1. Test Conditions: F_{OSC} = 20 MHz, T_{OSC} = 50 ns. Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	20	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	50	250	ns
T_{XHXX}	High Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 × T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



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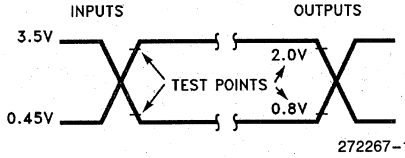
AC TESTING INPUT, OUTPUT WAVEFORMS



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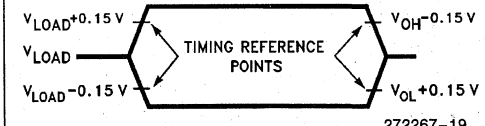
AC Testing inputs are driven at 3.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for logic "0".

FLOAT WAVEFORMS

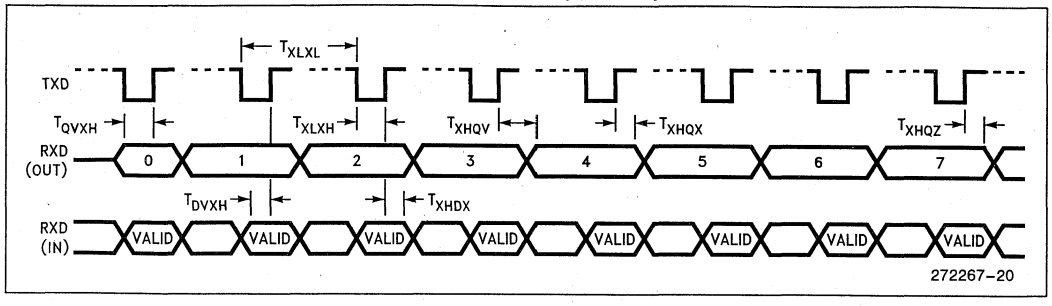


272267-19

For timing purposes a Port Pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \leq 15$ mA.

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)



AC CHARACTERISTICS—SERIAL PORT-SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)

Test Conditions: $T_A = -40°C$ to $+125°C$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0.0V$; Load Capacitance = pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}(2)	Serial Port Clock Period (BRR ≥ 8002H) Receive Only	6 T_{OSC}		ns
T_{XLXH}(2)	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} − 50	4 T_{OSC} + 50	ns
T_{XLXL}(2)	Serial Port Clock Period (BRR = 8001H) Transmit Only	4 T_{OSC}		ns
T_{XLXH}(2)	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} − 50	2 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}(1)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(1)	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTES:
1. Parameters not tested.
2. The minimum baud rate register value for Receive is 8002H. The minimum baud rate register value for Transmit is 8001H.

A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	10	15	μs(2)
F_{OSC}	Oscillator Frequency	4.0	20	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	±3.0	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±3.0	LSBs
Differential Non-Linearity		−0.75	+0.75	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	μA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 5 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	0	+70	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V(1)
T_{SAM}	Sample Time	1.0		µs(2)
T_{CONV}	Conversion Time	7	20	µs(2)
F_{OSC}	Oscillator Frequency	4.0	20	MHz

NOTES:
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD__TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Using Above Operating Conditions)(6)

Parameter	Typ*(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1.0	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1.0	LSBs
Differential Non-Linearity		−0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C(1) LSB/C(1) LSB/C(1)
Off Isolation		−60		dB(1,2,3)
Feedthrough	−60			dB(1,2)
V_{CC} Power Supply Rejection	−60			dB(1,2)
Input Resistance		750	1.2K	Ω(4)
DC Input Leakage	±1.0	0	±3.0	µA
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5)
Sampling Capacitor	3.0			pF

*An "LSB" as used here has a value of approximately 5 mV.

NOTES:
1. These values are expected for most parts at 25°C, but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer break-before-make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
6. All conversions performed with processor in IDLE mode.

OTPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature During Programming	20	30	°C
V_{CC}	Supply Voltage During Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage During Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	20.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC OTPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{PLPH}	$\overline{PROG}$ Pulse Width(2)	50		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to next $\overline{PALE}$ Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to next $\overline{PROG}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	$\overline{RESET}$ High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to $\overline{AINC}$ Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with F_{OSC} = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5V ±0.5V, T_C = 25°C ±5°C and V_{PP} = 12.5V ±0.25V. For run-time programming over a full operating range, contact factory.
2. This specification is for the word dump mode. For programming pulses use Modified Quick Pulse Algorithm.

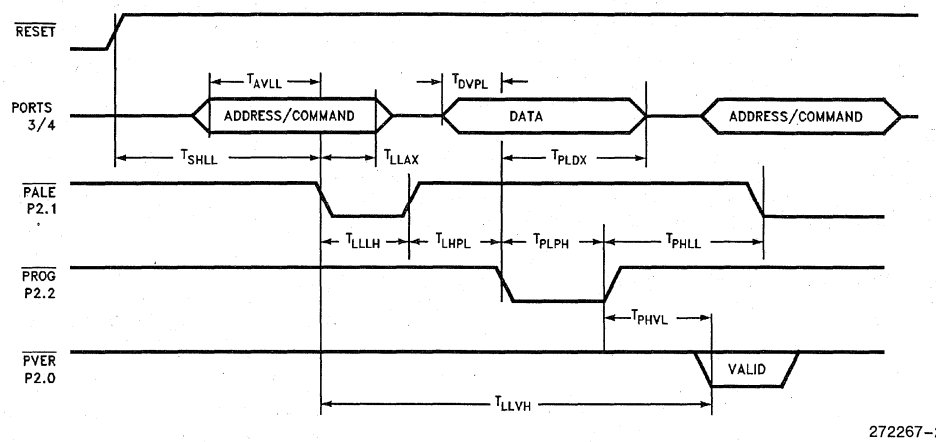
DC OTPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		200	mA

NOTE:
Do not apply V_{PP} unti V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

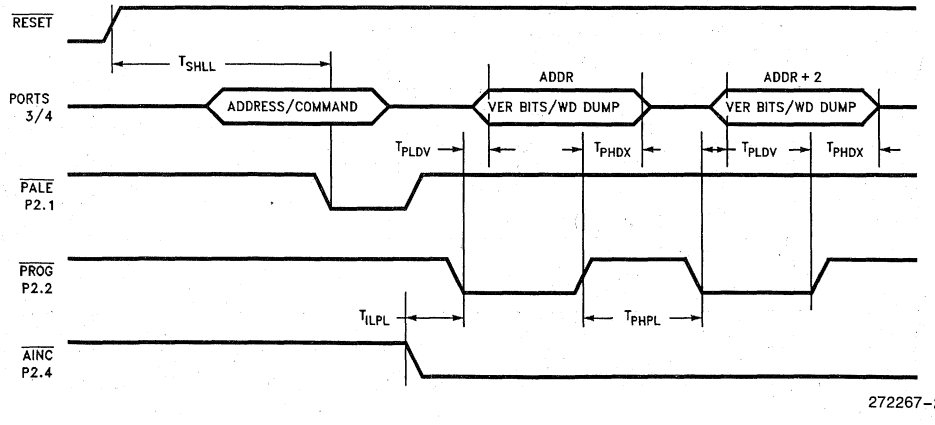
OTPROM PROGRAMMING WAVEFORMS

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



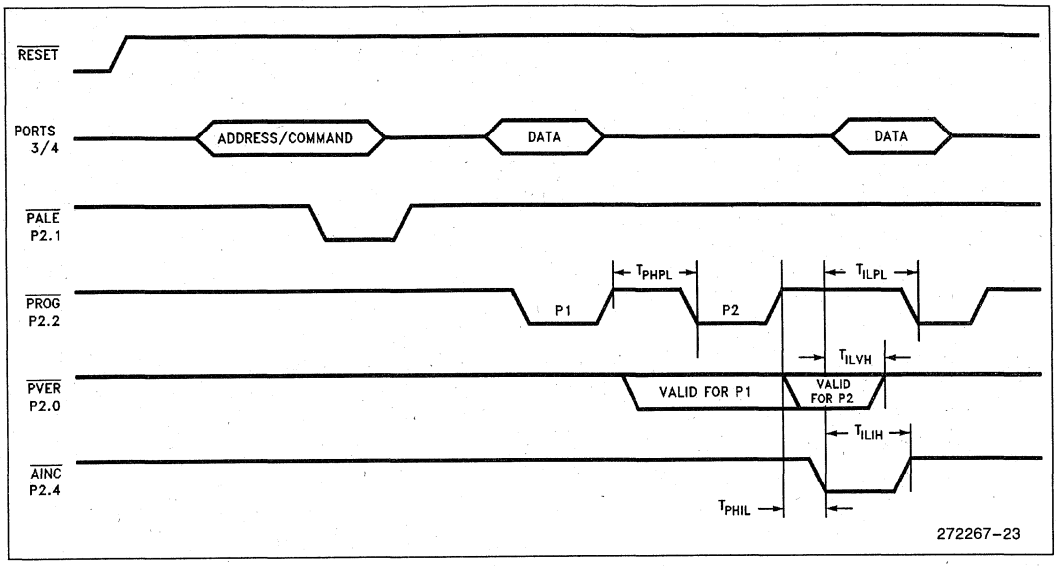
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP MODE WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT



This data sheet (272267-004) applies to devices marked with a "D" at the end of the top side tracking number.

8XC196NT Design Considerations

1. When operating in bus timing modes 1 or 2, the upper and lower address/data lines must be latched. Even in 8-bit bus mode, the upper address lines must be latched. In modes 0 and 3, the upper address lines DO NOT NEED to be latched in 8-bit bus width mode. But in 16-bit buswidth mode the upper address lines need to be latched.

8XC196NT ERRATA see Faxback #2344

1. ILLEGAL Opcode interrupt vector.
2. Aborted Interrupt vectors to lowest priority.
3. PTS Request during Interrupt latency.

DATA SHEET REVISION HISTORY

This datasheet applies to devices marked with a "D" at the end of the topside tracking number. The topside tracking number consists of nine characters and is the second line on the top side of the device. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are differences between the 272267-003 and 272267-004 datasheets:

1. Changed all references of "EPROM" to "OTPROM".
2. Added all the Slave Port pins to the package diagram and pin descriptions.
3. Added $\overline{\text{INTOUT}}$ pin to pin descriptions.
4. Changed ILI1 (input leakage current for Port 0) from $\pm 1\ \mu A$ to $\pm 3\ \mu A$.
5. Removed T_{LLYV} from AC characterisics and waveform diagrams.
6. T_{RLCL} in Mode 0 and 3, changed from $+4$ ns min. to -5 ns min.
7. T_{WHQX} in Mode 0 and 3, changed from $T_{OSC} - 30$ min. to $T_{OSC} - 35$ min.
8. Clarified the Ready waveform timings for Mode 0 and 3, by adding "$+2\ T_{OSC}$*".
9. T_{LHLL} in Mode 1, changed from $T_{OSC} - 10$ min. to $T_{OSC} - 20$ min.
10. T_{AVLL} in Mode 1, changed from $0.5\ T_{OSC} - 15$ min. to $0.5\ T_{OSC} - 20$ min.
11. T_{LLAX} in Mode 1, changed from $0.5\ T_{OSC} - 20$ min. to $0.5\ T_{OSC} - 25$ min.
12. T_{LHLL} in Mode 2, changed from $T_{OSC} - 10$ min. to $T_{OSC} - 20$ min.
13. T_{XLXL} and T_{XLXH} for the Serial Port timings were changed to reflect the minimum baudrate for receive and transmit modes.
14. Added the 8XC196NT ERRATA section.

8XC196NP
COMMERCIAL CHMOS 16-BIT MICROCONTROLLER

- 25 MHz Operation at 4.5–5.5 Volts
- 1 Mbyte of Linear Address Space
- Optional 4 Kbytes of ROM
- 1000 Bytes of Register RAM
- Register-register Architecture
- 32 I/O Port Pins
- 16 Prioritized Interrupt Sources
- 4 External Interrupt Pins and NMI Pin
- 2 Flexible 16-bit Timer/Counters with Quadrature Counting Capability
- 3 Pulse-width Modulator (PWM) Outputs with High Drive Capability
- Full-duplex Serial Port with Dedicated Baud-rate Generator
- Peripheral Transaction Server
- Event Processor Array (EPA) with 4 High-speed Capture/Compare Channels
- Chip-select Unit
  - 6 Chip Select Pins
  - Dynamic Demultiplexed/Multiplexed Address/Data Bus for Each Chip Select
  - Programmable Wait States (0, 1, 2, or 3) for Each Chip Select
  - Programmable Bus Width (8- or 16-bit) for Each Chip Select
  - Programmable Address Range for Each Chip Select
- 1.12 μs 16 x 16 Unsigned Multiplication
- 1.92 μs 32/16 Unsigned Division
- 100-pin SQFP or 100-pin QFP Package
- Complete System Development Support
- High-speed CHMOS Technology

The 8XC196NP is a member of Intel's 16-bit MCS® 96 microcontroller family. The device features 1 Mbyte of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation. When operating at 25 MHz in demultiplexed mode, the 8XC196NP can access a 100 ns memory device with zero wait states. The 8XC196NP is available without ROM (80C196NP) or with 4 Kbytes of ROM (83C196NP).

December 1996

Order Number: 272459-006

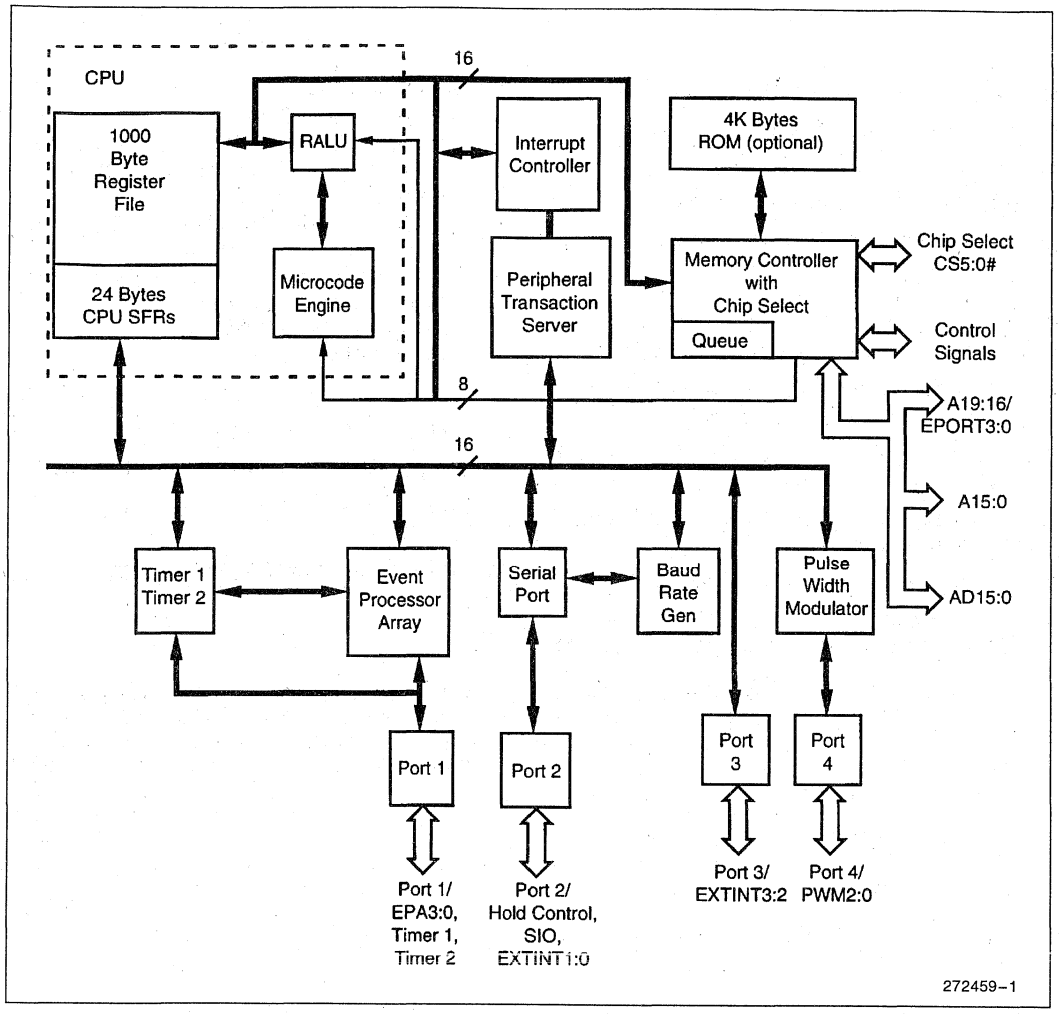


Figure 1. 8XC196NP Block Diagram

PROCESS INFORMATION

This device is manufactured on P648, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
100-pin SQFP	55°C/W	14°C/W
100-pin QFP	56°C/W	16°C/W

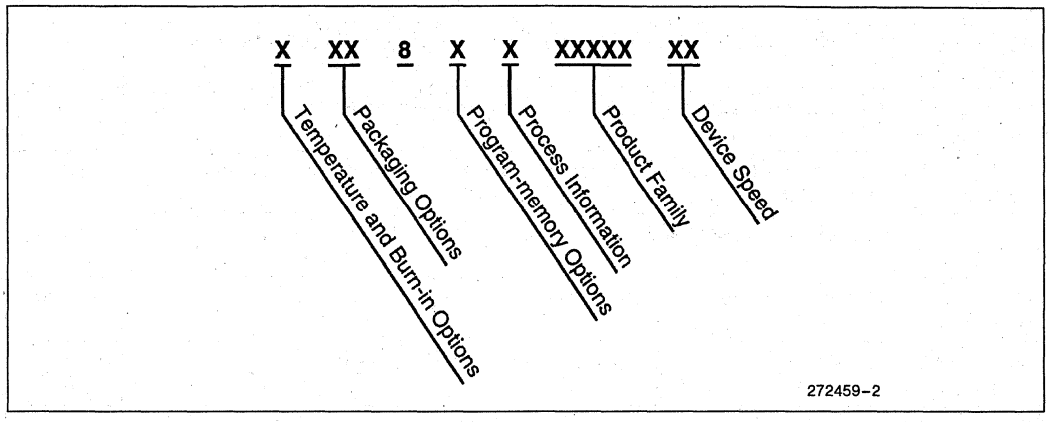


Figure 2. The 8XC196NP Family Nomenclature

Table 2. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in
Packaging Options	S SB	QFP SQFP
Program-memory Options	0 3	No ROM ROM
Process Information	C	CHMOS
Product Family	196NP	
Device Speed	no mark	25 MHz

Table 3. 8XC196NP Memory Map

Address (Note 1)	Description	Notes
FF FFFFH FF 3000H	External device (memory or I/O) connected to address/data bus	9
FF 2FFFH FF 2000H	Internal ROM or external device (memory or I/O) connected to address/data bus (determined by EA# pin)	2,9
FF 1FFFH FF 0000H	External device (memory or I/O) connected to address/data bus	3,9
FE FFFFH 0F 0000H	Overlaid memory (reserved for future devices)	3,9
0E FFFFH 01 0000H	896 Kbytes of external device (memory or I/O) connected to address/data bus	9
00 FFFFH 00 3000H	External device (memory or I/O) connected to address/data bus	9
00 2FFFH 00 2000H	External device (memory or I/O) connected to address/data bus or remapped internal ROM	5, 6,9
00 1FFFH 00 1FE0H	Memory-mapped peripheral special-function registers (SFRs)	4, 7,9
00 1FDFH 00 1F00H	Internal peripheral special-function registers (SFRs)	4, 7, 10
00 1EFFH 00 0400H	External device (memory or I/O) (reserved for future devices)	6
00 03FFH 00 0100H	Upper register file (general-purpose register RAM)	8, 10
00 00FFH 00 0018H	Lower register file (general-purpose register RAM and stack pointer)	8, 11
00 0017H 00 0000H	Lower register file (CPU SFRs)	4, 7, 8, 11

NOTES:
1. Internally, there are 24 address bits (A23:0); however, only 20 address lines (A19:0) are bonded out. The external address space is 1 Mbyte (00000–FFFFFH).
2. The 8XC196NP resets to internal address FF2080H (FF2080H in internal ROM or F2080H in external memory).
3. Do not locate code in addresses xF0000–xF00FFH. These addresses are reserved for the ICE in-circuit emulator. Unless otherwise noted, write 0FFH to reserved memory locations.
4. Unless otherwise noted, write 0 to reserved SFR bits.
5. These areas are mapped into internal ROM if the REMAP bit (CCB1.2) is set and EA# is at logic 1. Otherwise, they are mapped to external memory.
6. **WARNING:** The contents or functions of these memory locations may change with future device revisions, in which case a program that relies on one or more of these locations may not function properly.
7. Refer to the *8XC196NP User's Manual or 8XC196NP Quick Reference* for SFR descriptions.
8. Code executed in locations 000000H to 0003FFH will be forced external.
9. Address with indirect, indexed, or extended modes.
10. Address with indirect, indexed, or extended modes or through register windows.
11. Address with direct, indirect, indexed, or extended modes.

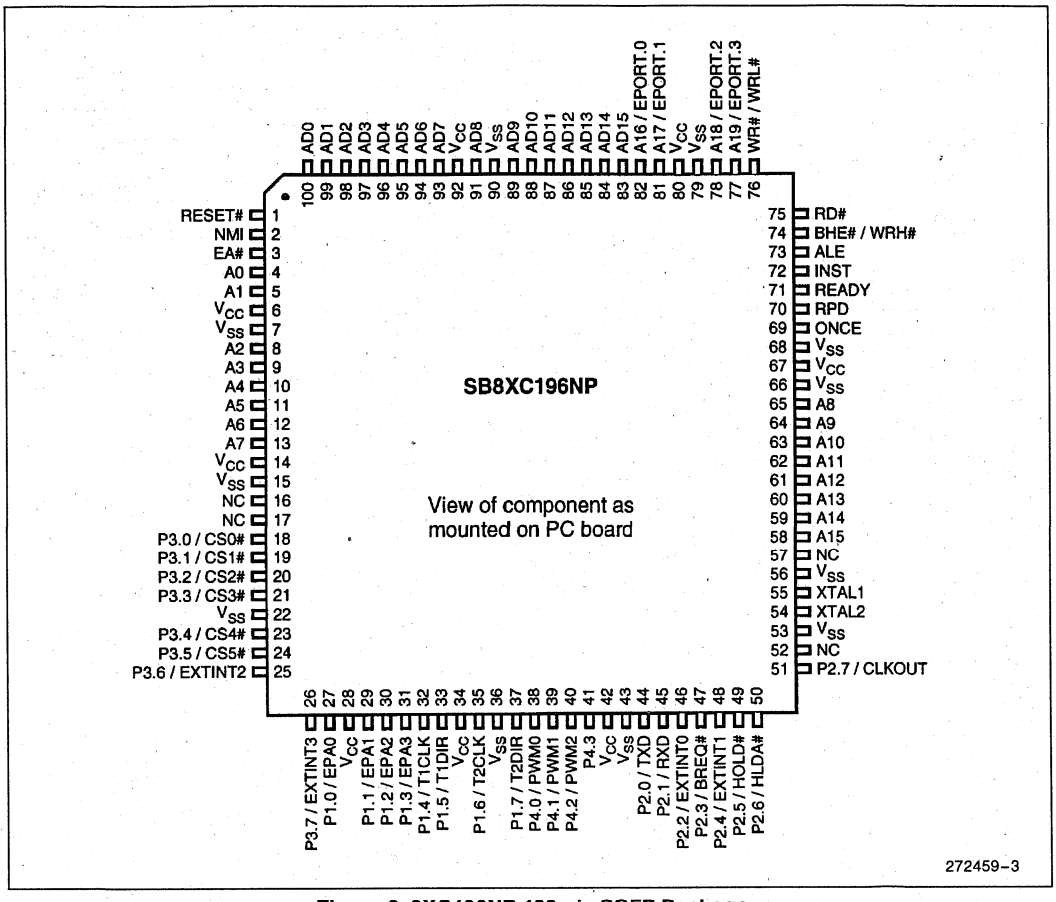


Figure 3. 8XC196NP 100-pin SQFP Package

Table 4. 8XC196NP 100-pin SQFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	RESET#	26	EXTINT3/P3.7	51	CLKOUT/P2.7	76	WR#/WRL#
2	NMI	27	EPA0/P1.0	52	NC†	77	EPORT.3/A19
3	EA#	28	V_{CC}	53	V_{SS}	78	EPORT.2/A18
4	A0	29	EPA1/P1.1	54	XTAL2	79	V_{SS}
5	A1	30	EPA2/P1.2	55	XTAL1	80	V_{CC}
6	V_{CC}	31	EPA3/P1.3	56	V_{SS}	81	EPORT.1/A17
7	V_{SS}	32	T1CLK/P1.4	57	NC†	82	EPORT.0/A16
8	A2	33	T1DIR/P1.5	58	A15	83	AD15
9	A3	34	V_{CC}	59	A14	84	AD14
10	A4	35	T2CLK/P1.6	60	A13	85	AD13
11	A5	36	V_{SS}	61	A12	86	AD12
12	A6	37	T2DIR/P1.7	62	A11	87	AD11
13	A7	38	PWM0/P4.0	63	A10	88	AD10
14	V_{CC}	39	PWM1/P4.1	64	A9	89	AD9
15	V_{SS}	40	PWM2/P4.2	65	A8	90	V_{SS}
16	NC†	41	P4.3	66	V_{SS}	91	AD8
17	NC†	42	V_{CC}	67	V_{CC}	92	V_{CC}
18	CS0#/P3.0	43	V_{SS}	68	V_{SS}	93	AD7
19	CS1#/P3.1	44	TXD/P2.0	69	ONCE	94	AD6
20	CS2#/P3.2	45	RXD/P2.1	70	RPD	95	AD5
21	CS3#/P3.3	46	EXTINT0/P2.2	71	READY	96	AD4
22	V_{SS}	47	BREQ#/P2.3	72	INST	97	AD3
23	CS4#/P3.4	48	EXTINT1/P2.4	73	ALE	98	AD2
24	CS5#/P3.5	49	HOLD#/P2.5	74	BHE#/WRH#	99	AD1
25	EXTINT2/P3.6	50	HLDA#/P2.6	75	RD#	100	AD0

† To be compatible with future versions of the Nx family, tie the no connection (NC) pins as follows: Pin 57 = V_{SS}, Pin 16 = V_{CC}, Pin 17 = V_{SS} (5 volts on this pin will enable a clock doubler on future devices), and Pin 52 = V_{CC}.

Table 5. 100-pin SQFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
A0	4
A1	5
A2	8
A3	9
A4	10
A5	11
A6	12
A7	13
A8	65
A9	64
A10	63
A11	62
A12	61
A13	60
A14	59
A15	58
A16	82
A17	81
A18	78
A19	77
AD0	100
AD1	99
AD2	98
AD3	97
AD4	96
AD5	95
AD6	94
AD7	93
AD8	91
AD9	89
AD10	88
AD11	87
AD12	86

Address & Data (cont)	
Name	**Pin**
AD13	85
AD14	84
AD15	83

Bus Control & Status	
Name	**Pin**
ALE	73
BHE#/WRH#	74
BREQ#	47
HOLD#	49
HLDA#	50
INST	72
RD#	75
READY	71
WR#/WRL#	76

Processor Control	
Name	**Pin**
CLKOUT	51
EA#	3
EXTINT0	46
EXTINT1	48
EXTINT2	25
EXTINT3	26
NMI	2
ONCE	69
RESET#	1
RPD	70
XTAL1	55
XTAL2	54

Input/Output	
Name	**Pin**
CS0#/P3.0	18
CS1#/P3.1	19
CS2#/P3.2	20
CS3#/P3.3	21
CS4#/P3.4	23
CS5#/P3.5	24
EPA0/P1.0	27
EPA1/P1.1	29
EPA2/P1.2	30
EAP3/P1.3	31
EPORT.0	82
EPORT.1	81
EPORT.2	78
EPORT.3	77
P2.2	46
P2.3	47
P2.4	48
P2.5	49
P2.6	50
P2.7	51
P3.6	25
P3.7	26
P4.3	41
PWM0/P4.0	38
PWM1/P4.1	39
PWM2/P4.2	40
RXD/P2.1	45
T1CLK/P1.4	32
T1DIR/P1.5	33
T2CLK/P1.6	35
T2DIR/P1.7	37
TXD/P2.0	44

Power & Ground	
Name	**Pin**
V_{CC}	6
V_{CC}	14
V_{CC}	28
V_{CC}	34
V_{CC}	42
V_{CC}	67
V_{CC}	80
V_{CC}	92
V_{SS}	7
V_{SS}	15
V_{SS}	22
V_{SS}	36
V_{SS}	43
V_{SS}	53
V_{SS}	56
V_{SS}	66
V_{SS}	68
V_{SS}	79
V_{SS}	90

No Connection	
Name	**Pin**
NC	16
NC	17
NC	52
NC	57

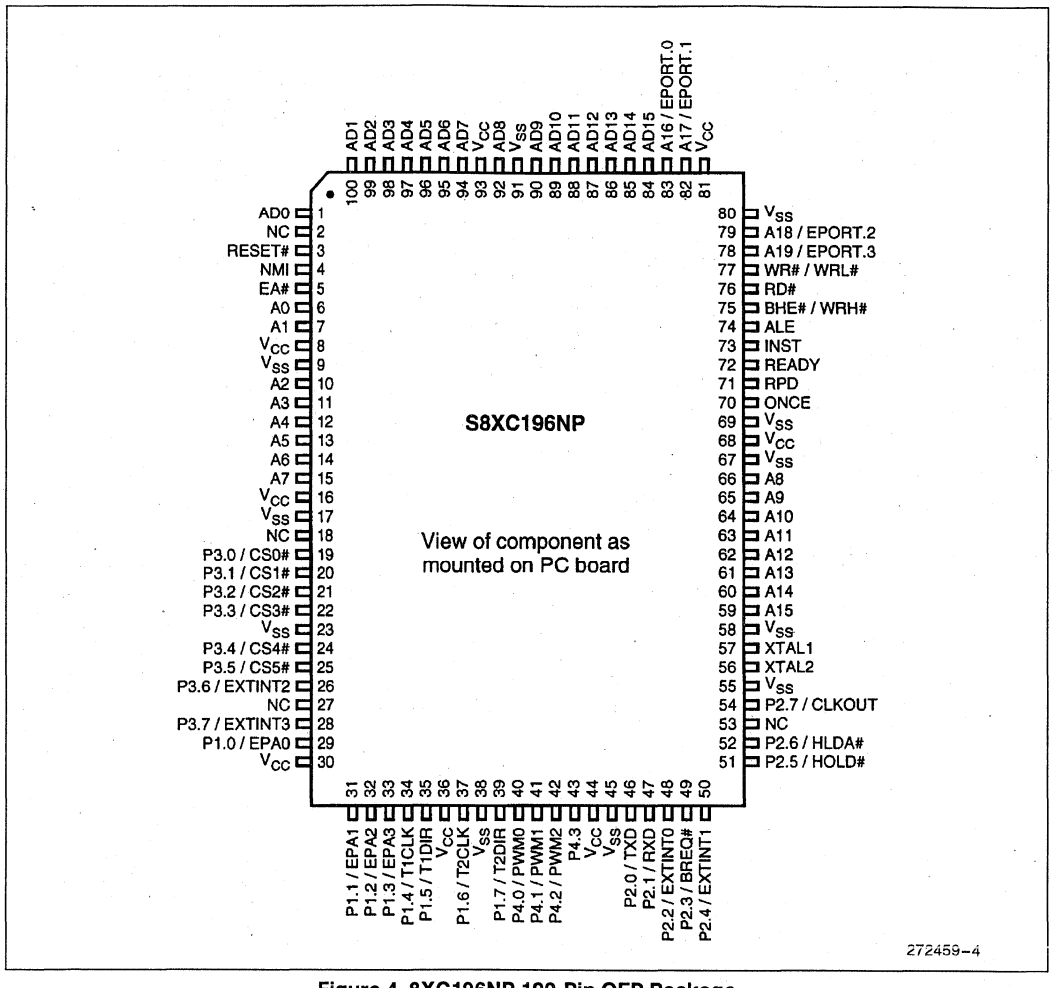


Figure 4. 8XC196NP 100-Pin QFP Package

Table 6. 100-Pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	No Connection	27	No Connection	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	No Connection	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	EA#	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	No Connection	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	V_{SS}	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

Table 7. 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	Pin
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88
AD12	87

Address & Data (cont)	
Name	Pin
AD13	86
AD14	85
AD15	84

Bus Control & Status	
Name	Pin
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	Pin
CLKOUT	54
EA#	5
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56

Input/Output	
Name	Pin
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EAP3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	Pin
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	69
V_{SS}	80
V_{SS}	91

No Connection	
Name	Pin
NC	2
NC	18
NC	27
NC	53

PIN DESCRIPTIONS

Table 8. Pin Descriptions

Name	Type	Description	Multiplexed with
A15:0	I/O	System Address Bus These address lines provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.	—
A19:16	I/O	Address Lines 16–19 These address lines provide address bits 16–19 during the entire external memory cycle, supporting extended addressing of the 1-Mbyte address space. Internally, there are 24 address bits; however, only 20 address lines (A19:0) are bonded out. The external address space is 1 Mbyte (00000–FFFFFH) and the internal address space is 16 Mbytes (000000–FFFFFFH). The 8XC196NP resets to internal address FF2080H (FF2080H in internal ROM or F2080H in external memory).	EPORT.3:0
AD15:0	I/O	Address/Data Lines The function of these pins depends on the bus size and mode. **16-bit Multiplexed Bus Mode:** AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **8-bit Multiplexed Bus Mode:** AD15:8 drive address bits 8–15 during the entire bus cycle. AD7:0 drive address bits 0–7 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **16-bit Demultiplexed Mode:** AD15:0 drive or receive data during the entire bus cycle. **8-bit Demultiplexed Mode:** AD7:0 drive or receive data during the entire bus cycle. AD15:8 drive the data that is currently on the high byte of the internal bus.	—
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A19:16 and AD15:0 for a multiplexed bus; A19:0 for a demultiplexed bus). ALE differs from ADV# in that it does not remain active during the entire bus cycle. An external latch can use this signal to demultiplex the address bits 0–15 from the address/data bus in multiplexed mode.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
BHE#	O	Byte High Enable The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#. During 16-bit bus cycles, this active-low output signal is asserted for word reads and writes and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with A0, to determine which memory byte is being transferred over the system bus: **BHE# A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only	WRH#
BREQ#	O	Bus Request This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. The device can assert BREQ# at the same time as or after it asserts HLDA#. Once it is asserted, BREQ# remains asserted until HOLD# is removed. You must enable the bus-hold protocol before using this signal.	P2.3
CLKOUT	O	Clock Output Output of the internal clock generator. The CLKOUT frequency is ½ the internal operating frequency (F_{XTAL1}). CLKOUT has a 50% duty cycle.	P2.7
CS5#:0	O	Chip-select Lines 0–5 The active-low output CSx# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select x. If the external memory address is outside the range assigned to the six chip selects, no chip-select output is asserted and the bus configuration defaults to the CS5# values. Immediately following reset, CS0# is automatically assigned to the range FF2000–FF20FFH (F2000–F20FFH if external).	P3.5:0
EA#	I	External Access This input determines whether memory accesses to special-purpose and program memory partitions (FF2000–FF2FFFH) are directed to internal or external memory. These accesses are directed to internal memory if EA# is held high and to external memory if EA# is held low. For an access to any other memory location, the value of EA# is irrelevant. EA# is not latched and can be switched dynamically during normal operating mode. Be sure to thoroughly consider the issues, such as different access times for internal and external memory, before using this dynamic switching capability. On devices with no internal nonvolatile memory, always connect EA# to V_{SS}.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
EPA3:0	I/O	Event Processor Array (EPA) Input/Output pins These are the high-speed input/output pins for the EPA capture/compare channels. For high-speed PWM applications, the outputs of two EPA channels (either EPA0 and EPA1 or EPA2 and EPA3) can be remapped to produce a PWM waveform on a shared output pin.	P1.3:0
EPORT.3:0	I/O	Extended Addressing Port This is a 4-bit, bidirectional, memory-mapped I/O port. The pins are shared with the extended address bus A19:16.	A19:16
EXTINT0 EXTINT1 EXTINT2 EXTINT3	I	External Interrupts In normal operating mode, a rising edge on EXTINTx sets the EXTINTx interrupt pending bit. EXTINTx is sampled during phase 2 (CLKOUT high). The minimum high time is one state time. In powerdown mode, asserting the EXTINTx signal for at least 1 state time causes the device to resume normal operation. The interrupt need not be enabled, but the pin must be configured as a special-function input. If the EXTINTx interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation.	P2.2 P2.4 P3.6 P3.7
HLDA#	O	Bus Hold Acknowledge This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#.	P2.6
HOLD#	I	Bus Hold Request An external device uses this active-low input signal to request control of the bus. This pin functions as HOLD# only if the pin is configured for its special function and the bus-hold protocol is enabled. Setting bit 7 of the window selection register enables the bus-hold protocol.	P2.5
INST	O	Instruction Fetch This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.	—
NMI	I	Nonmaskable Interrupt In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
ONCE	I	On-circuit Emulation Holding ONCE high during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. This mode puts all pins into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator. To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent accidental entry into ONCE mode, connect the ONCE pin to V_{SS}.	—
P1.3:0 P1.4 P1.5 P1.6 P1.7	I/O	Port 1 This is a standard, bidirectional port that is multiplexed with individually selectable special-function signals.	EPA3:0 T1CLK T1DIR T2CLK T2DIR
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	I/O	Port 2 This is a standard, bidirectional port that is multiplexed with individually selectable special-function signals.	TXD RXD EXTINT0 BREQ# EXTINT1 HOLD# HLDA# CLKOUT
P3.5:0 P3.6 P3.7	I/O	Port 3 This is an 8-bit, bidirectional, standard I/O port.	CS5:0# EXTINT2 EXTINT3
P4.2:0 P4.3	I/O	Port 4 This is a 4-bit, bidirectional, standard I/O port with high-current drive capability.	PWM2:0
PWM2:0	O	Pulse Width Modulator Outputs These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable.	P4.2:0
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads.	—
READY	I	Ready Input This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states in addition to the wait states that are generated internally. When READY is high, CPU operation continues in a normal manner with wait states inserted as programmed in the chip configuration registers, Register 0, or the chip-select x bus control register. READY is ignored for all internal memory accesses.	—

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
RESET#	I/O	Reset A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown, standby, and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. After a device reset, the first instruction fetch is from FF2080H (or F2080H in external memory). For the 80C196NP, the program and special-purpose memory locations (FF2000–FF2FFFH) reside in external memory. For the 83C196NP, these locations can reside either in external memory or in internal ROM.	—
RPD	I	Return from Powerdown Timing pin for the return-from-powerdown circuit. If your application uses powerdown mode, connect a capacitor between RPD and V_{SS} if the internal oscillator is the clock source. The capacitor causes a delay that enables the oscillator to stabilize before the internal CPU and peripheral clocks are enabled. The capacitor is not required if your application uses powerdown mode and if an external clock input is the clock source. If your application does not use powerdown mode, leave this pin unconnected.	—
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data.	P2.1
T1CLK	I	Timer 1 External Clock External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode. and External clock for the serial I/O baud-rate generator input (program selectable).	P1.4
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. Also used in conjunction with T2DIR for quadrature counting mode.	P1.6
T1DIR	I	Timer 1 External Direction External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode.	P1.5
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. Also used in conjunction with T2CLK for quadrature counting mode.	P1.7

Table 8. Pin Descriptions (Continued)

Name	Type	Description	Multiplexed with
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD is used to transmit serial port data. In mode 0, it is used as the serial clock output.	P2.0
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.	—
V_{SS}	GND	Digital Circuit Ground Connect each V_{SS} pin to ground through the lowest possible impedance path.	—
WR#	O	Write This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.	WRL#
WRH#	O	Write High During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.	BHE#
WRL#	O	Write Low During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations. The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.	WR#
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.	—
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.	—

ELECTRICAL CHARACTERISTICS

NOTICE: This document contains information on products in the design phase of development. The specifications are subject to change without notice. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales Office that you have the latest datasheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −60°C to +150°C
Supply Voltage with Respect to V_{SS} ..... −0.5V to +7.0V
Power Dissipation 1.5W

**WARNING:* *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5V to 5.5V
F_{XTAL1} (Input Frequency for V_{CC} = 4.5V–5.5V)
(Note 1) ..... 8 MHz to 25 MHz

NOTES:
1. This device is static and should operate below 1 Hz, but has been tested only down to 8 MHz.

DC Characteristics

Table 9. DC Characteristics at V_{CC} = 4.5–5.5V (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		80	120	mA	XTAL1 = 25 MHz V_{CC} = 5.5V Device in Reset
I_{IDLE}	Idle Mode Current		24	36	mA	XTAL1 = 25 MHz V_{CC} = 5.5V
I_{PD}	Powerdown Mode Current (Note 2)		50	75	µA	V_{CC} = 5.5V
I_{LI}	Input Leakage Current (all input pins except RESET)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage (all pins)	−0.5		0.8	V	
V_{IH}	Input High Voltage	0.2 V_{CC} +1		V_{CC} +0.5	V	
V_{IL1}	Input Low Voltage XTAL1	−0.5		0.3 V_{CC}	V	
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage (output configured as complementary) (Notes 3,6)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (output configured as complementary) (Note 6)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7.0 mA
V_{OL1}	Output Low Voltage on P4.x (output configured as complementary)			0.45 0.6	V V	I_{OL} = 10 mA I_{OL} = 15 mA

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
5. Pin capacitance is not tested. C_S is based on design simulations.
6. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)
P1	42	42
P2	42	42
P3	42	42
P4	45	21
EPORT	21	21
Individual		
P1, P2, P3	10	10
P4	18	10

Table 9. DC Characteristics at V_{CC} = 4.5–5.5V (Note 1) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OL2}	Output Low Voltage in RESET on ALE, INST, and NMI			0.45	V	I_{OL} = 3 µA
V_{OH1}	Output High Voltage in RESET (Note 4)	V_{CC} – 0.7			V	I_{OH} = –3 µA
V_{OL3}	Output Low Voltage in RESET for ONCE pin			0.45	V	I_{OL} = 30 µA
V_{OL4}	Output Low Voltage on XTAL2			0.3 0.45 1.5	V V V	I_{OL} = 100 µA I_{OL} = 700 µA I_{OL} = 3 mA
V_{OH2}	Output High Voltage on XTAL2	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –100 µA I_{OH} = –700 µA I_{OH} = –3 mA
V_{TH+} – V_{TH-}	Hysteresis voltage width on RESET# pin		0.3		V	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 5)			10	pF	
R_{RST}	RESET Pull-up Resistor	9		95	kΩ	V_{CC} = 5.5 V, V_{IN} = 4.0V

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
5. Pin capacitance is not tested. C_S is based on design simulations.
6. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)
P1	42	42
P2	42	42
P3	42	42
P4	45	21
EPORT	21	21
Individual		
P1, P2, P3	10	10
P4	18	10

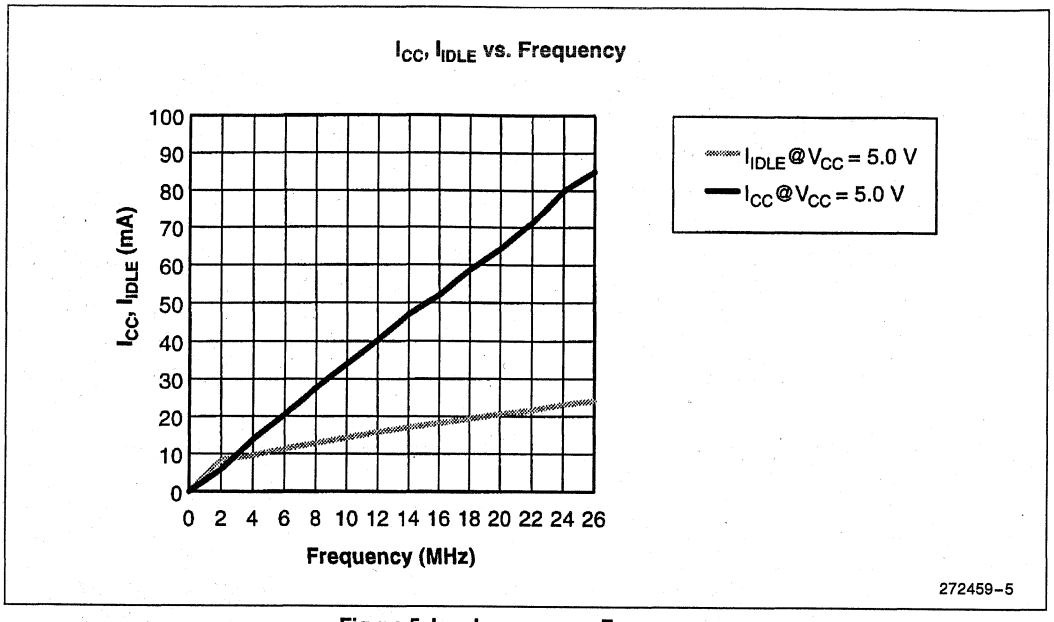


Figure 5. I_{CC}, I_{IDLE} versus Frequency

AC Characteristics—Multiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 10. AC Characteristics, Multiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications				
F_{XTAL1}	Input frequency on XTAL1	8	25	MHz
T_{XTAL1}	Period, $1/F_{XTAL1}$	40	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High/Low	10	110	ns
T_{CLCL}	CLKOUT Cycle Time	$2T_{XTAL1}$		ns
T_{CHCL}	CLKOUT High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVRL}	AD15:0 Valid to RD# Low	$2T_{XTAL1} - 20$		ns
T_{AVWL}	AD15:0 Valid to WR# Low	$2T_{XTAL1} - 10$		ns
T_{WHSH}	A19:16, CSx# Hold after WR# Rising Edge	0		
T_{RHSH}	A19:16, CSx# Hold after RD# Rising Edge	0		
T_{CLLH}	CLKOUT Low to ALE High	−10	10	ns
T_{LLCH}	ALE Low to CLKOUT High	−15	10	ns
T_{LHLH}	ALE Cycle Time	$4T_{XTAL1}$		ns (2)
T_{LHLL}	ALE High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVLL}	AD15:0 Valid to ALE Low	$T_{XTAL1} - 15$		ns
T_{LLAX}	AD15:0 Hold after ALE Low	$T_{XTAL1} - 25$		ns
T_{LLRL}	ALE Low to RD# Low	$T_{XTAL1} - 15$		ns
T_{RLCL}	RD# Low to CLKOUT Low	0	20	ns
T_{RLRH}	RD# Low Period	T_{XTAL1}		ns (2)
T_{RHLH}	RD# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 15$	ns (3)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Low to WR# Low	$T_{XTAL1} - 15$		ns
T_{CLWL}	CLKOUT Low to WR# Low	−15	10	ns
T_{QVWH}	Data Valid before WR# High	$T_{XTAL1} - 15$		ns (2)
T_{CHWH}	CLKOUT High to WR# High	−10	10	ns
T_{WLWH}	WR# Low Period	$T_{XTAL1} - 5$		ns (2)

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

Table 10. AC Characteristics, Multiplexed Bus Mode (Continued)

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications (Continued)				
T_{WHQX}	Data Hold after WR# High	$T_{XTAL1} - 20$		ns
T_{WHLH}	WR# High to ALE High	$T_{XTAL1} - 12$	$T_{XTAL1} + 20$	ns (3)
T_{WHBX}	BHE#, INST Hold after WR# High	$T_{XTAL1} - 10$		ns
T_{WHAX}	AD15:8 Hold after WR# High	$T_{XTAL1} - 10$		ns (4)
T_{RHBX}	BHE#, INST Hold after RD# High	$T_{XTAL1} - 10$		ns
T_{RHAX}	AD15:8 Hold after RD# High	$T_{XTAL1} - 10$		ns (4)

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.

Table 11. AC Characteristics, Multiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
The External Memory System Must Meet These Specifications				
T_{AVYV}	AD15:0 Valid to READY Setup		$2T_{XTAL1} - 50$	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{XTAL1} - 10$	ns (1)
T_{AVDV}	AD15:0 Valid to Input Data Valid		$3T_{XTAL1} - 40$	ns (2)
T_{RLDV}	RD# Active to Input Data Valid		$T_{XTAL1} - 20$	ns (2)
T_{SLDV}	Chip-select Low, A19:16 Valid to Data Valid		$4T_{XTAL1} - 50$	
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{XTAL1} - 35$	ns
T_{RHDZ}	End of RD# to Input Data Float		$T_{XTAL1} - 5$	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.

SYSTEM BUS TIMINGS, MULTIPLEXED BUS

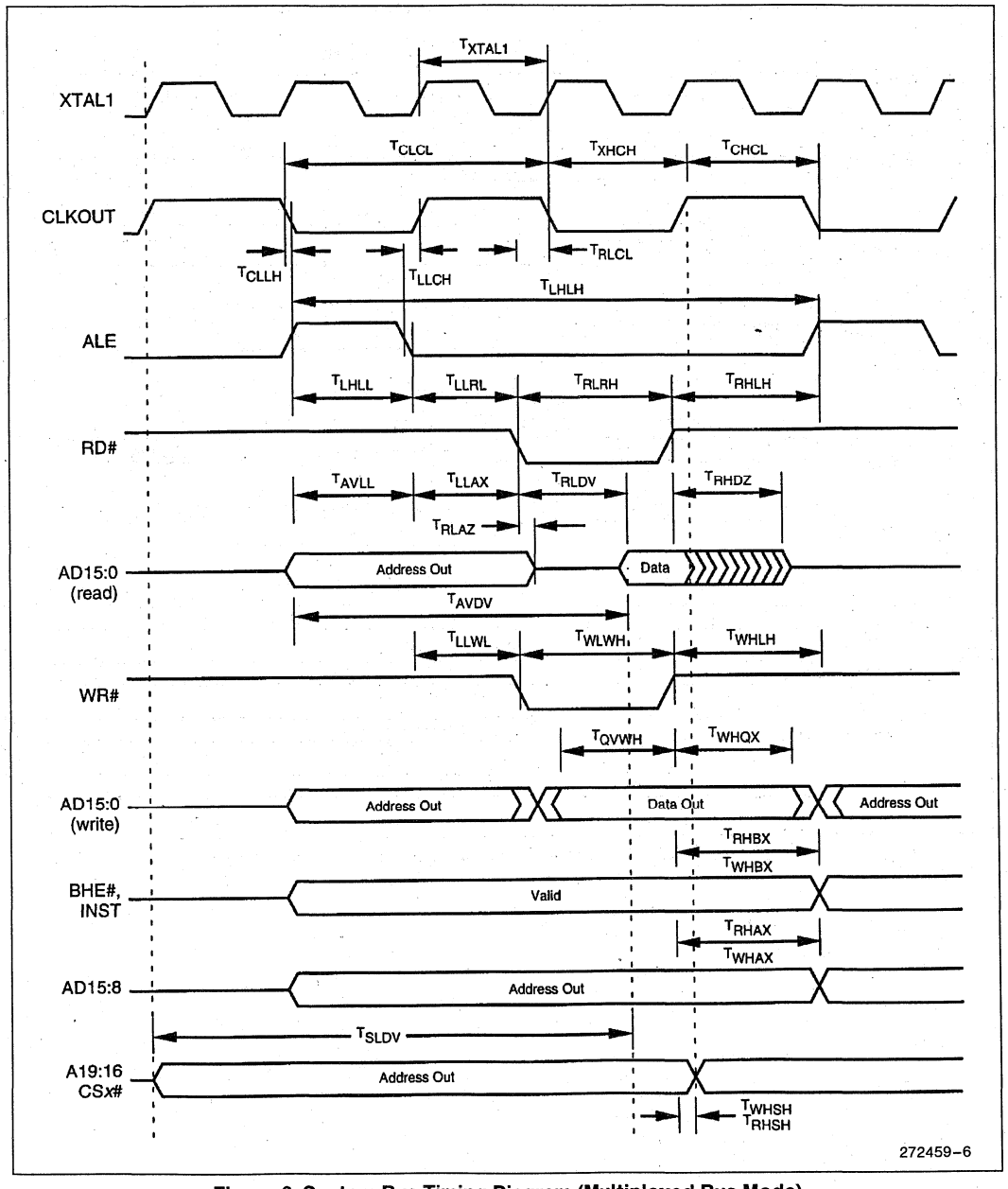


Figure 6. System Bus Timing Diagram (Multiplexed Bus Mode)

READY TIMING, MULTIPLEXED BUS

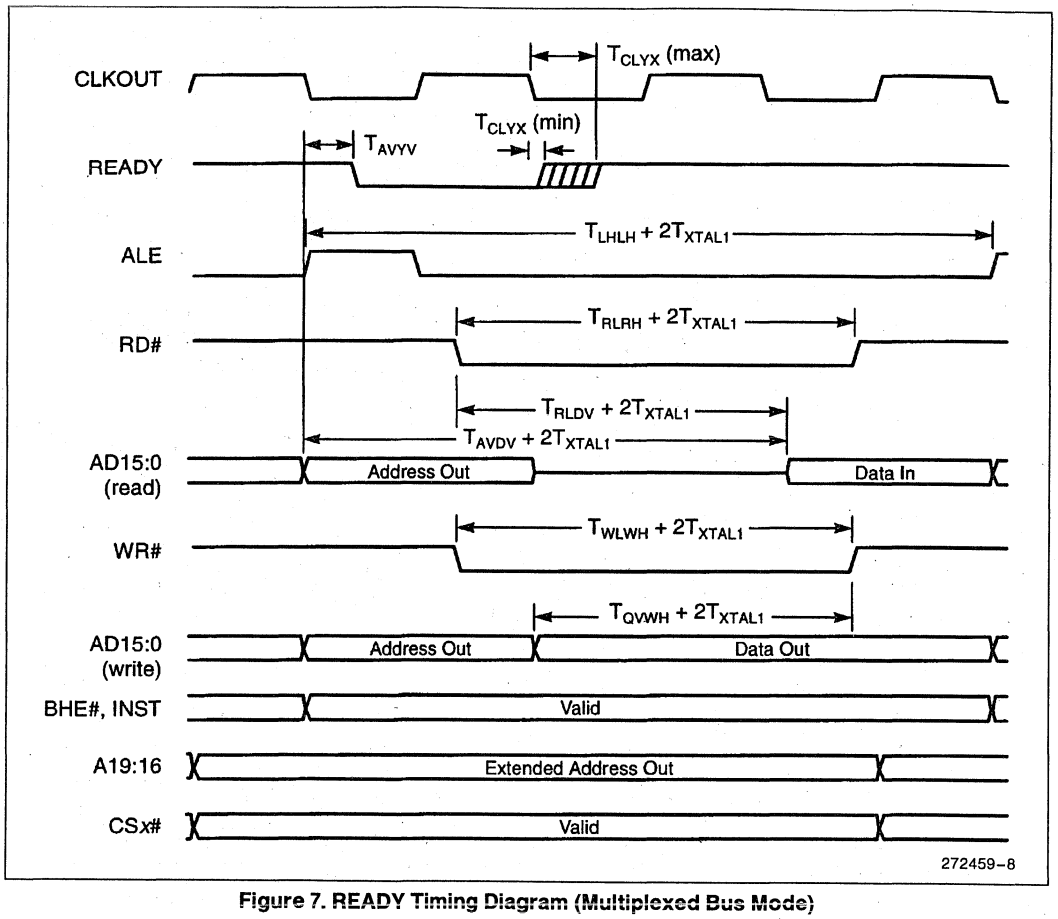


Figure 7. READY Timing Diagram (Multiplexed Bus Mode)

AC Characteristics—Demultiplexed Bus Mode

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 12. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications				
F_{XTAL1}	Input frequency on XTAL1	8	25	MHz
T_{XTAL1}	Period, $1/F_{XTAL1}$	40	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High/Low	10	110	ns
T_{CLCL}	CLKOUT Cycle Time	$2T_{XTAL1}$		ns
T_{CHCL}	CLKOUT High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVRL}	A19:0, CSx# Valid to RD# Low	$2T_{XTAL1} - 30$		ns
T_{AVWL}	A19:0, CSx# Valid to WR# Low	$2T_{XTAL1} - 25$		ns
T_{CLLH}	CLKOUT Low to ALE High	−10	10	ns
T_{LLCH}	ALE Low to CLKOUT High	−15	10	ns
T_{LHLH}	ALE Cycle Time	$4T_{XTAL1}$		ns (2)
T_{LHLL}	ALE High Period	$T_{XTAL1} - 10$	$T_{XTAL1} + 10$	ns
T_{AVLL}	Address Valid to ALE Low	NA		ns
T_{LLAX}	Address Hold after ALE Low	NA		ns
T_{LLRL}	ALE Low to RD# Low	NA		ns
T_{RLCH}	RD# Low to CLKOUT High	0	15	ns
T_{RLRH}	RD# Low Period	$2T_{XTAL1} - 10$		ns (2)
T_{RHLH}	RD# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 20$	ns (3)
T_{RLAZ}	RD# Low to Address Float		NA	ns
T_{LLWL}	ALE Low to WR# Low	NA		ns
T_{WLCH}	WR# Low to CLKOUT High	− 5	10	ns
T_{QVWH}	Data Valid before WR# High	$3T_{XTAL1} - 37$		ns (2)
T_{CHWH}	CLKOUT High to WR# High	− 15	5	ns
T_{WLWH}	WR# Low Period	$2T_{XTAL1} - 10$		ns (2)
T_{WHQX}	Data Hold after WR# High	$T_{XTAL1} - 20$		ns
T_{WHLH}	WR# High to ALE High	$T_{XTAL1} - 5$	$T_{XTAL1} + 20$	ns (3)
T_{WHBX}	BHE#, INST Hold after WR# High	$T_{XTAL1} - 10$		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.

Table 12. AC Characteristics, Demultiplexed Bus Mode (Continued)

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
The 8XC196NP Will Meet These Specifications (Continued)				
T_{WHAX}	A19:0, CSx# Hold after WR# High	0		ns
T_{RHBX}	BHE#, INST Hold after RD# High	T_{XTAL1} – 10		ns
T_{RHAX}	A19:0, CSx# Hold after RD# High	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. Assuming back-to-back bus cycles.

Table 13. AC Characteristics, Demultiplexed Bus Mode

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
The External Memory System Must Meet These Specifications				
T_{AVYV}(3)	A19:0, CSx# Valid to READY Setup		$3T_{XTAL1}$ – 60	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{XTAL1} – 10	ns (1)
T_{AVDV}	A19:0, CSx# Valid to Input Data Valid		$4T_{XTAL1}$ – 50	ns (2)
T_{RLDV}	RD# Active to Input Data Valid		$2T_{XTAL1}$ – 25	ns (2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{XTAL1} – 35	ns
T_{RHDZ}	End of RD# to Input Data Float		T_{XTAL1} – 5	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns

NOTES:
1. Exceeding the maximum specification causes additional wait states.
2. If wait states are used, add $2T_{XTAL1} \times n$, where n = number of wait states.
3. When forcing wait states using the BUSCON register, add $2t \times n$.

SYSTEM BUS TIMINGS, DEMULTIPLEXED BUS

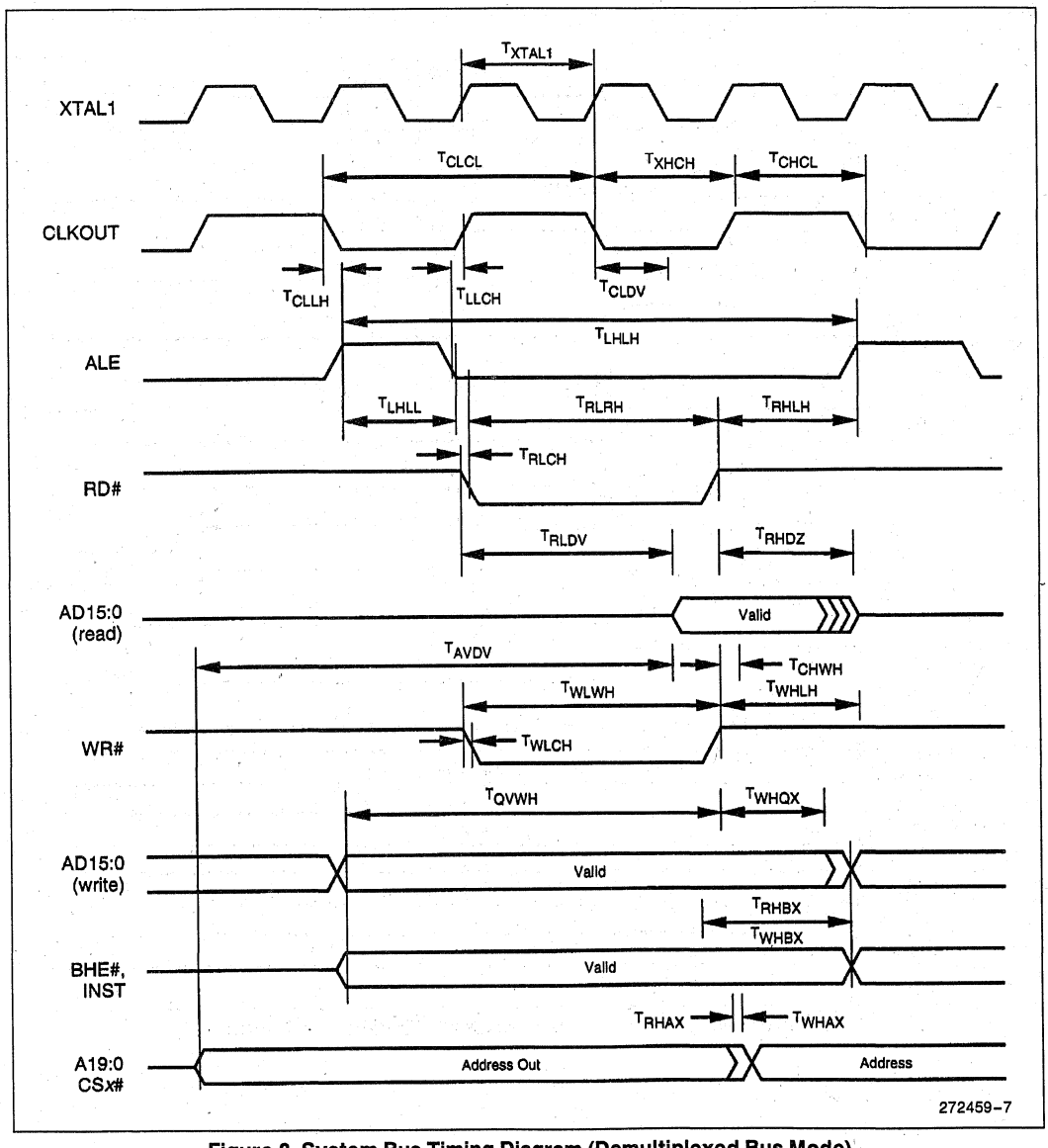


Figure 8. System Bus Timing Diagram (Demultiplexed Bus Mode)

READY TIMING, DEMULTIPLEXED BUS

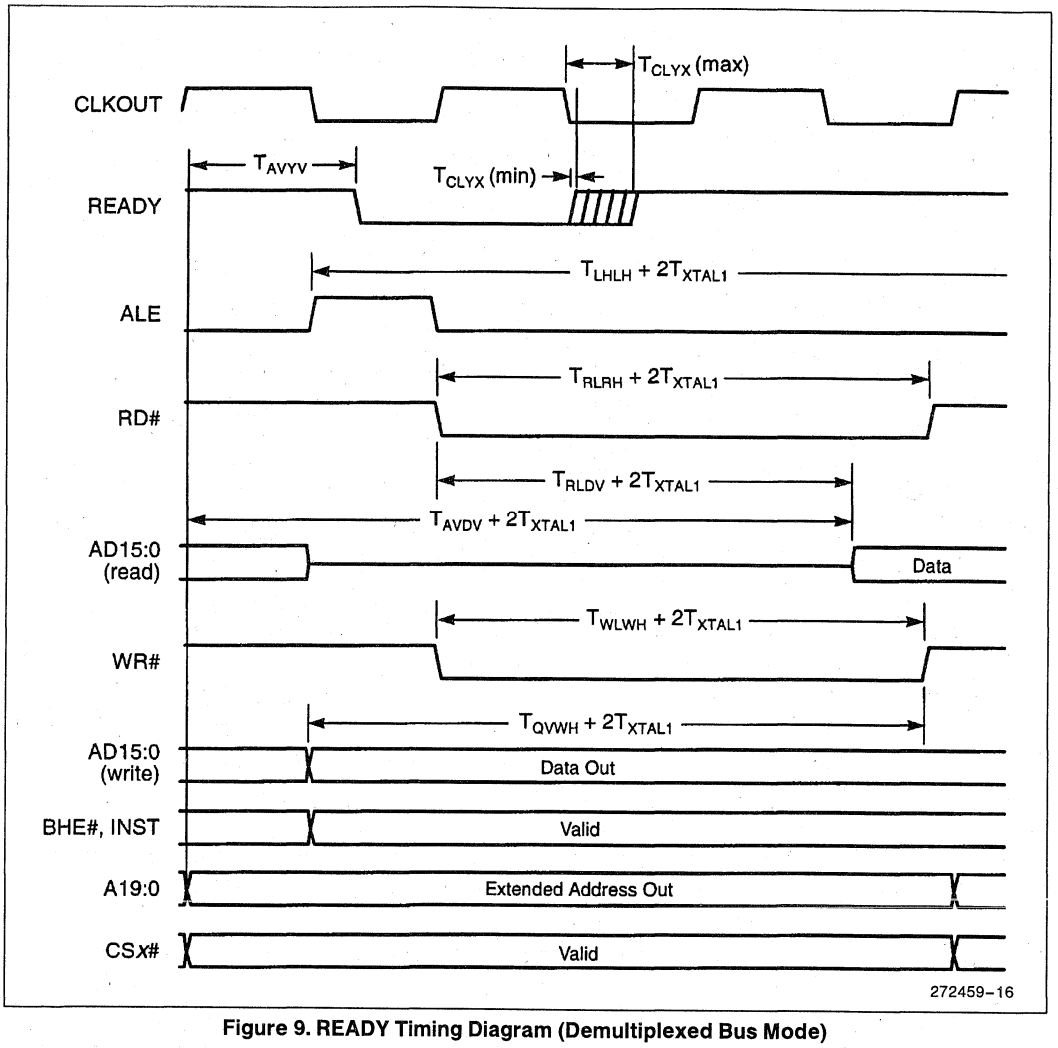


Figure 9. READY Timing Diagram (Demultiplexed Bus Mode)

HOLD#/HLDA# Timing

Table 14. HOLD#/HLDA# Timings

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
T_{HVCH}	HOLD# Setup Time	65		ns (1)
T_{CLHAL}	CLKOUT Low to HLDA# Low	−15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	−15	15	ns
T_{HALAZ}	HLDA# Low to Address Float		33	ns
T_{HALBZ}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	−25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	−25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	−20		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	−20		ns

NOTE:
1. To guarantee recognition at next clock.

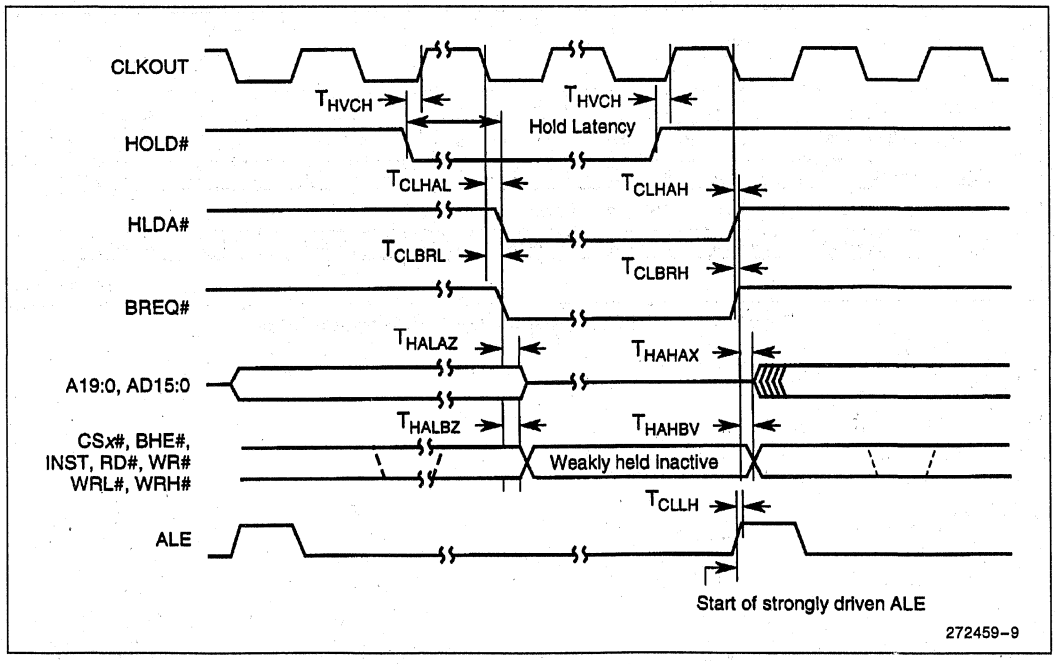


Figure 10. HOLD#/HLDA# Timing Diagram

AC Characteristics—Serial Port, Shift Register Mode

Table 15. Serial Port Timing—Shift Register Mode

Symbol	Parameter	V_{CC} = 4.5V–5.5V		Units
		Min	Max	
T_{XLXL}	Serial Port Clock period (SP_BAUD ≥ x002H) (SP_BAUD = x001H) (Note 1)	 $6T_{XTAL1}$ $4T_{XTAL1}$		 ns ns
T_{QVXH}	Output data setup to clock high	$3T_{XTAL1}$		ns
T_{XHQX}	Output data hold after clock high	$2T_{XTAL1} - 50$		ns
T_{XHQV}	Next output data valid after clock high		$2T_{XTAL1} + 50$	ns
T_{DVXH}	Input data setup to clock high	$2T_{XTAL1} + 200$		ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		$5T_{XTAL1}$	ns

NOTE:
1. The minimum baud-rate register (SP_BAUD) value for receive is x002H and the minimum baud-rate register value for transmit is x001H.

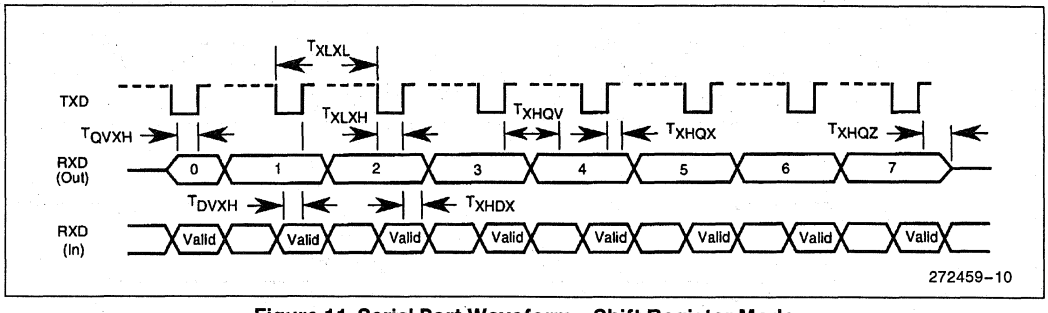


Figure 11. Serial Port Waveform—Shift Register Mode

External Clock Drive

Table 16. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Input frequency	8	25	MHz
T_{XLXL}	Period (T_{XTAL1})	40	125	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

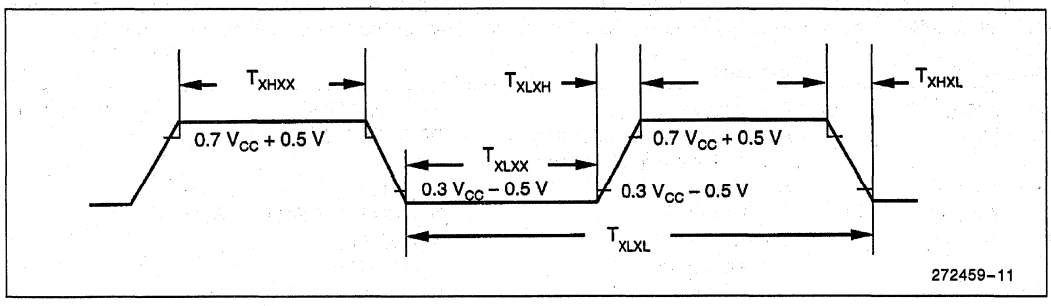
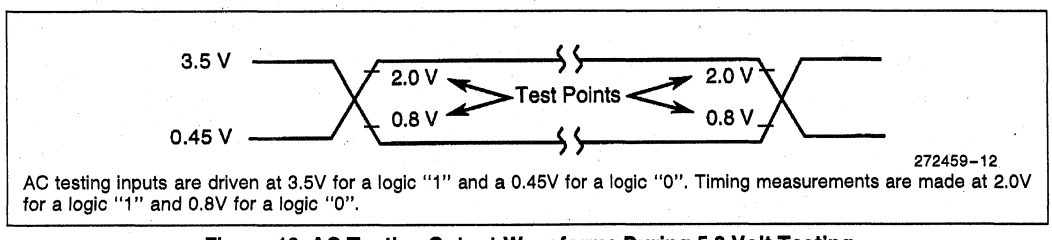
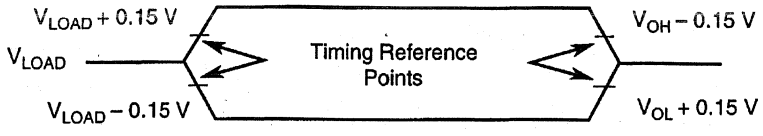


Figure 12. External Clock Drive Waveforms



AC testing inputs are driven at 3.5V for a logic "1" and a 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

Figure 13. AC Testing Output Waveforms During 5.0 Volt Testing



For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loaded V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

Figure 14. Float Waveforms During 5.0 Volt Testing

EXPLANATION OF AC SYMBOLS

Each AC timing symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:	Signals:	
H — High	A — Address	L — ALE/ADV#
L — Low	AD — Address/Data Bus for Multiplexed Bus Mode	BR — BREQ#
V — Valid	B — BHE#	R — RD#
X — No Longer Valid	C — CLKOUT	W — WR#/WRH#/WRL#
Z — Floating	D — DATA	X — XTAL1
	G — Buswidth	Y — READY
	H — HOLD#	Q — Data Out
	HA — HLDA#	S — Chip Select

8XC196NP ERRATA

Change identifiers have been used on embedded products since 1990. The change identifier is the last character in the FPO number. The FPO number is typically a nine character number located on the second line of the topside package mark. The following errata listing is applicable to the B-step (denoted by a "B" or "C" at the end of the topside tracking number):

1. Any jump, conditional jump, or call instruction located within six bytes of the top of a page, i.e., 0FFFA-0FFFFH, may cause a jump to the wrong page. To ensure this problem does not occur, place at least six NOPs at the top of each page.

The following errata listing is applicable to the A-step (denoted by an "A" at the end of the topside tracking number):

1. Any jump, conditional jump, or call instruction located within six bytes of the top of a page, i.e., 0FFFA-0FFFFH, may cause a jump to the wrong page. To ensure this problem does not occur, place at least six NOPs at the top of each page.
2. The illegal opcode interrupt vector is not taken when an illegal opcode is encountered. A branch to an unknown location occurs.
3. (1-Mbyte mode only.) If an interrupt is aborted, intentionally or unintentionally, an undesired branch to the lowest priority interrupt vector (FF2000H) may occur even if the lowest priority interrupt is not enabled. This may occur if any bit in the INT_MASK, INT_MASK1, INT_PEND, or INT_PEND1 register is cleared after the corresponding INT_PEND or INT_PEND1 bit is set.
4. (1-Mbyte mode only.) If a standard interrupt occurs at approximately the same time (this time is code dependent and therefore cannot be stated as an exact number of state times) as a PTS serviced interrupt, the PTS interrupt may be processed as a standard interrupt. The standard interrupt service routine for a PTS serviced interrupt (End-of-PTS) is typically used to modify the PTS control block and re-enable the PTS by setting the corresponding bit in the PTSSEL register. When this anomaly occurs, the End-of-PTS service routine will execute regardless of the value in PTSCOUNT. As a result, an undetermined number of PTS cycles will not occur. This applies to all PTS interrupts.

DATA SHEET REVISION HISTORY

This data sheet is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are important changes to the 272459-005 datasheet:

1. Revised Tables 8 through 15 and Figures 5, 6, 7, and 13 to reflect new or changed information.
2. Added Table 3 and Figure 9.
3. The input frequency on XTAL1, formerly called F_{OSC}, is now denoted by F_{XTAL1}.
4. The AC characteristics tables have been divided into the following: the timing specifications met by the device, and the timing specifications that must be met by the external memory system.
5. Maximum IOL and IOH specifications added to the DC characteristics tables.
6. AC timings T_{AVWL} and T_{AVRL} added to the AC characteristics-multiplexed bus mode tables.

8XC196NU COMMERCIAL CHMOS 16-BIT MICROCONTROLLER

- 50 MHz Operation†
- 1 Mbyte of Linear Address Space
- Optional 48 Kbytes of ROM
- 1 Kbyte of Register RAM
- Register-register Architecture
- Footprint and Functionally Compatible Upgrade for the 8XC196NP
- 32 I/O Port Pins
- 16 Prioritized Interrupt Sources
- 4 External Interrupt Pins and NMI Pin
- 2 Flexible 16-bit Timer/Counters with Quadrature Counting Capability
- 3 Pulse-width Modulator (PWM) Outputs with High Drive Capability
- Full-duplex Serial Port with Dedicated Baud-rate Generator
- Peripheral Transaction Server

† 40 MHz standard; 50 MHz is Speed Premium

- Chip-select Unit
  - 6 Chip-select Pins
  - Dynamic Demultiplexed/Multiplexed Address/Data Bus for Each Chip Select
  - Programmable Wait States (0–3) for Each Chip Select
  - Programmable Bus Width (8- or 16-bit) for Each Chip Select
  - Programmable Address Range for Each Chip Select
- Event Processor Array (EPA) with 4 High-speed Capture/Compare Channels
- Multiply and Accumulate Executes in 640 ns Using the 32-bit Hardware Accumulator
- 960 ns 32/16 Unsigned Division
- 100-pin SQFP or 100-pin QFP Package
- Complete System Development Support
- High-speed CHMOS Technology

The 8XC196NU is a member of Intel's 16-bit MCS® 96 microcontroller family. The device features 1 Mbyte of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation.

1.0 PRODUCT OVERVIEW

The 8XC196NU is a member of Intel's 16-bit MCS® 96 microcontroller family. The device features 1 Mbyte of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation.

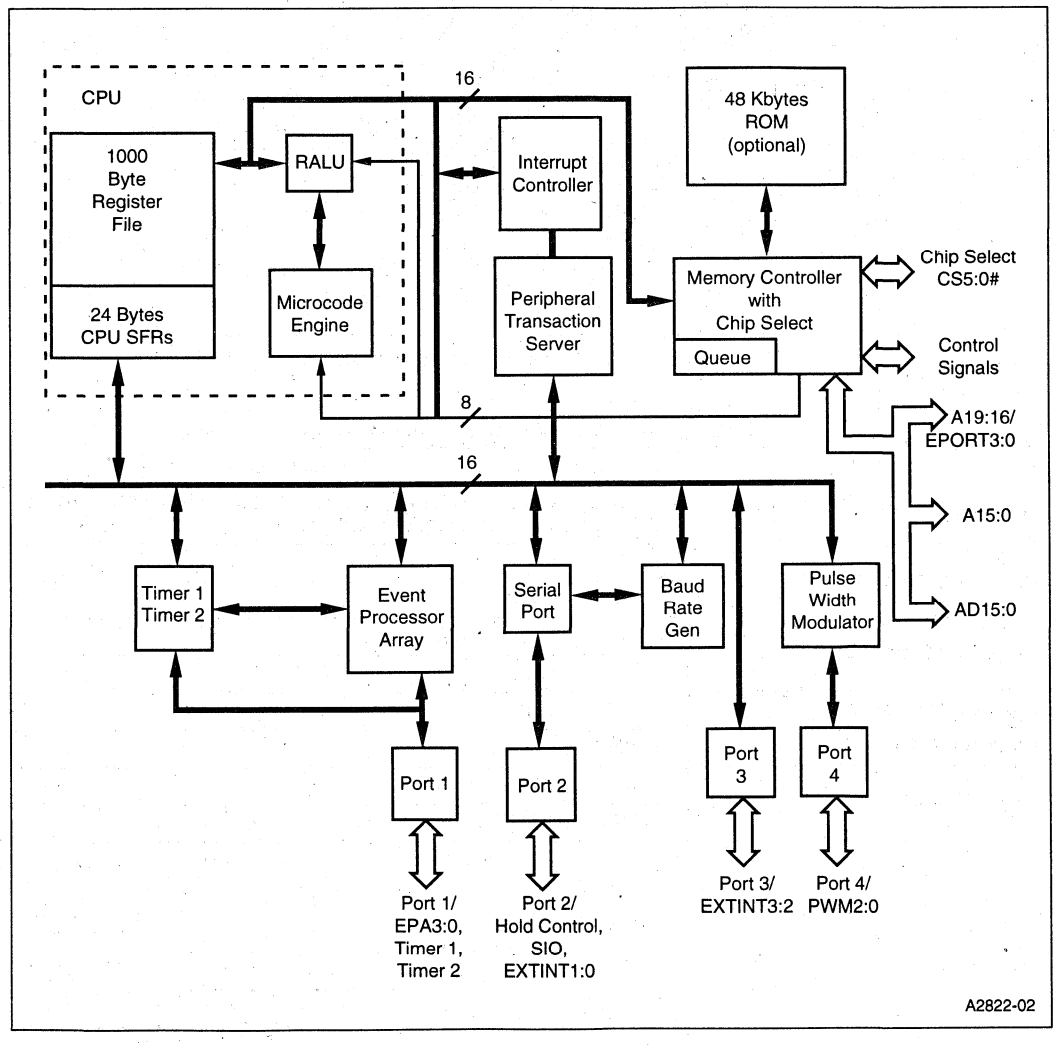


Figure 1. 8XC196NU Block Diagram

2.0 NOMENCLATURE OVERVIEW

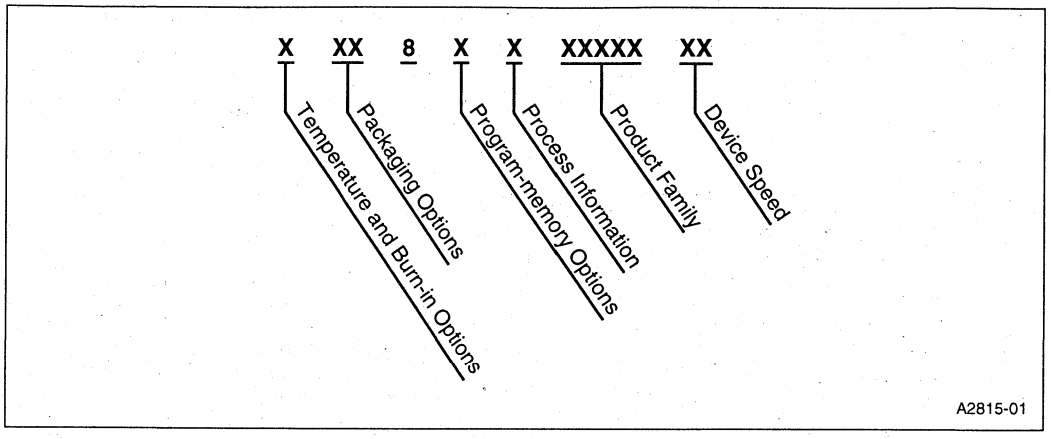


Figure 2. The 8XC196NU Family Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	S	QFP
	SB	SQFP
Program–memory Options	0	Without ROM
	3	ROM
Process Information	C	CHMOS
Product Family	196NU	—
Device Speed	no mark	40 MHz
	50	50 MHz

3.0 PINOUT

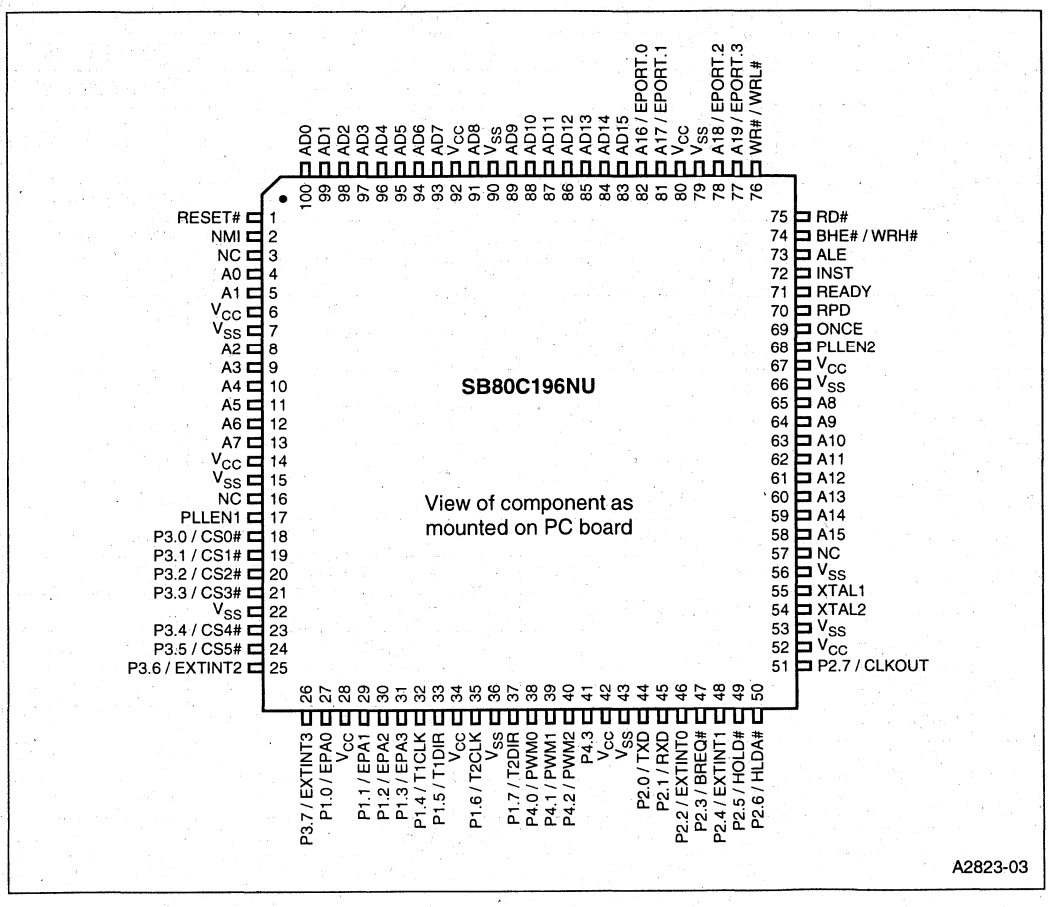


Figure 3. 80C196NU 100-pin SQFP Package

Table 2. 80C196NU 100-pin SQFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	RESET#	26	EXTINT3/P3.7	51	CLKOUT/P2.7	76	WR#/WRL#
2	NMI	27	EPA0/P1.0	52	V_{CC}	77	EPORT.3/A19
3	NC	28	V_{CC}	53	V_{SS}	78	EPORT.2/A18
4	A0	29	EPA1/P1.1	54	XTAL2	79	V_{SS}
5	A1	30	EPA2/P1.2	55	XTAL1	80	V_{CC}
6	V_{CC}	31	EPA3/P1.3	56	V_{SS}	81	EPORT.1/A17
7	V_{SS}	32	T1CLK/P1.4	57	NC	82	EPORT.0/A16
8	A2	33	T1DIR/P1.5	58	A15	83	AD15
9	A3	34	V_{CC}	59	A14	84	AD14
10	A4	35	T2CLK/P1.6	60	A13	85	AD13
11	A5	36	V_{SS}	61	A12	86	AD12
12	A6	37	T2DIR/P1.7	62	A11	87	AD11
13	A7	38	PWM0/P4.0	63	A10	88	AD10
14	V_{CC}	39	PWM1/P4.1	64	A9	89	AD9
15	V_{SS}	40	PWM2/P4.2	65	A8	90	V_{SS}
16	NC	41	P4.3	66	V_{SS}	91	AD8
17	PLLEN1	42	V_{CC}	67	V_{CC}	92	V_{CC}
18	CS0#/P3.0	43	V_{SS}	68	PLLEN2	93	AD7
19	CS1#/P3.1	44	TXD/P2.0	69	ONCE	94	AD6
20	CS2#/P3.2	45	RXD/P2.1	70	RPD	95	AD5
21	CS3#/P3.3	46	EXTINT0/P2.2	71	READY	96	AD4
22	V_{SS}	47	BREQ#/P2.3	72	INST	97	AD3
23	CS4#/P3.4	48	EXTINT1/P2.4	73	ALE	98	AD2
24	CS5#/P3.5	49	HOLD#/P2.5	74	BHE#/WRH#	99	AD1
25	EXTINT2/P3.6	50	HLDA#/P2.6	75	RD#	100	AD0

NOTE: To be compatible with future products, tie the NC (no connection) pins as follows: Pin 57 = V_{SS}, Pin 16 = V_{CC}, and Pin 3 = NC.

Table 3. 80C196NU 100-pin SQFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	Pin
A0	4
A1	5
A2	8
A3	9
A4	10
A5	11
A6	12
A7	13
A8	65
A9	64
A10	63
A11	62
A12	61
A13	60
A14	59
A15	58
A16	82
A17	81
A18	78
A19	77
AD0	100
AD1	99
AD2	98
AD3	97
AD4	96
AD5	95
AD6	94
AD7	93
AD8	91
AD9	89
AD10	88
AD11	87

Address & Data (continued)	
Name	Pin
AD12	86
AD13	85
AD14	84
AD15	83

Bus Control & Status	
Name	Pin
ALE	73
BHE#/WRH#	74
BREQ#	47
HOLD#	49
HLDA#	50
INST	72
RD#	75
READY	71
WR#/WRL#	76

Processor Control	
Name	Pin
CLKOUT	51
EXTINT0	46
EXTINT1	48
EXTINT2	25
EXTINT3	26
NMI	2
ONCE	69
RESET#	1
RPD	70
XTAL1	55
XTAL2	54
PLLEN1	17
PLLEN2	68

Input/Output	
Name	Pin
CS0#/P3.0	18
CS1#/P3.1	19
CS2#/P3.2	20
CS3#/P3.3	21
CS4#/P3.4	23
CS5#/P3.5	24
EPA0/P1.0	27
EPA1/P1.1	29
EPA2/P1.2	30
EPA3/P1.3	31
EPORT.0	82
EPORT.1	81
EPORT.2	78
EPORT.3	77
P2.2	46
P2.3	47
P2.4	48
P2.5	49
P2.6	50
P2.7	51
P3.6	25
P3.7	26
P4.3	41
PWM0/P4.0	38
PWM1/P4.1	39
PWM2/P4.2	40
RXD/P2.1	45
T1CLK/P1.4	32
T1DIR/P1.5	33
T2CLK/P1.6	35
T2DIR/P1.7	37
TXD/P2.0	44

Power & Ground	
Name	Pin
V_{CC}	6
V_{CC}	14
V_{CC}	28
V_{CC}	34
V_{CC}	42
V_{CC}	52
V_{CC}	67
V_{CC}	80
V_{CC}	92
V_{SS}	7
V_{SS}	15
V_{SS}	22
V_{SS}	36
V_{SS}	43
V_{SS}	53
V_{SS}	56
V_{SS}	66
V_{SS}	79
V_{SS}	90

No Connection	
Name	Pin
NC	3
NC	16
NC	57

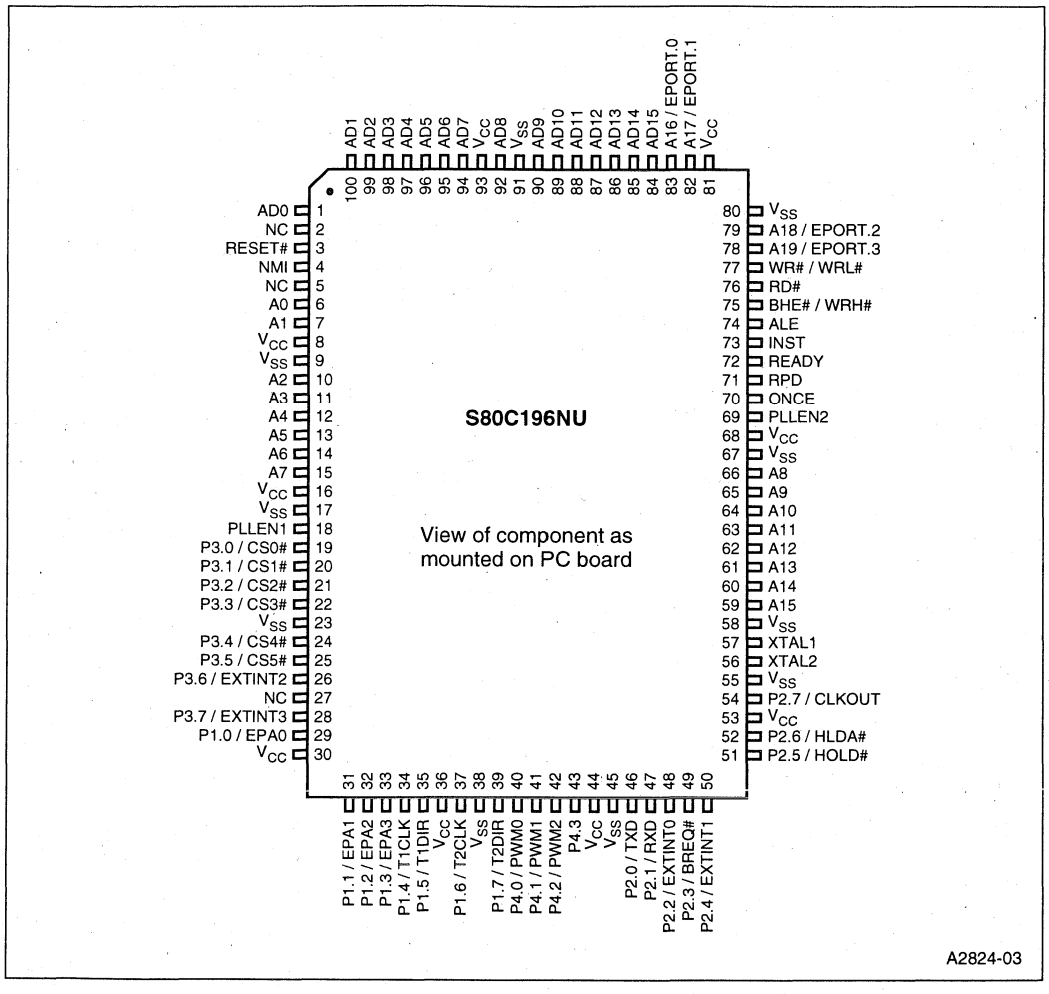


Figure 4. 80C196NU 100-pin QFP Package

Table 4. 80C196NU 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	NC	27	NC	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	V_{CC}	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	NC	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	PLLEN1	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	PLLEN2	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

Table 5. 80C196NU 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	Pin
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88

Address & Data (continued)	
Name	Pin
AD12	87
AD13	86
AD14	85
AD15	84

Bus Control & Status	
Name	Pin
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	Pin
CLKOUT	54
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56
PLLEN1	18
PLLEN2	69

Input/Output	
Name	Pin
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EPA3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	Pin
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	53
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	80
V_{SS}	91

No Connection	
Name	Pin
NC	2
NC	5
NC	27

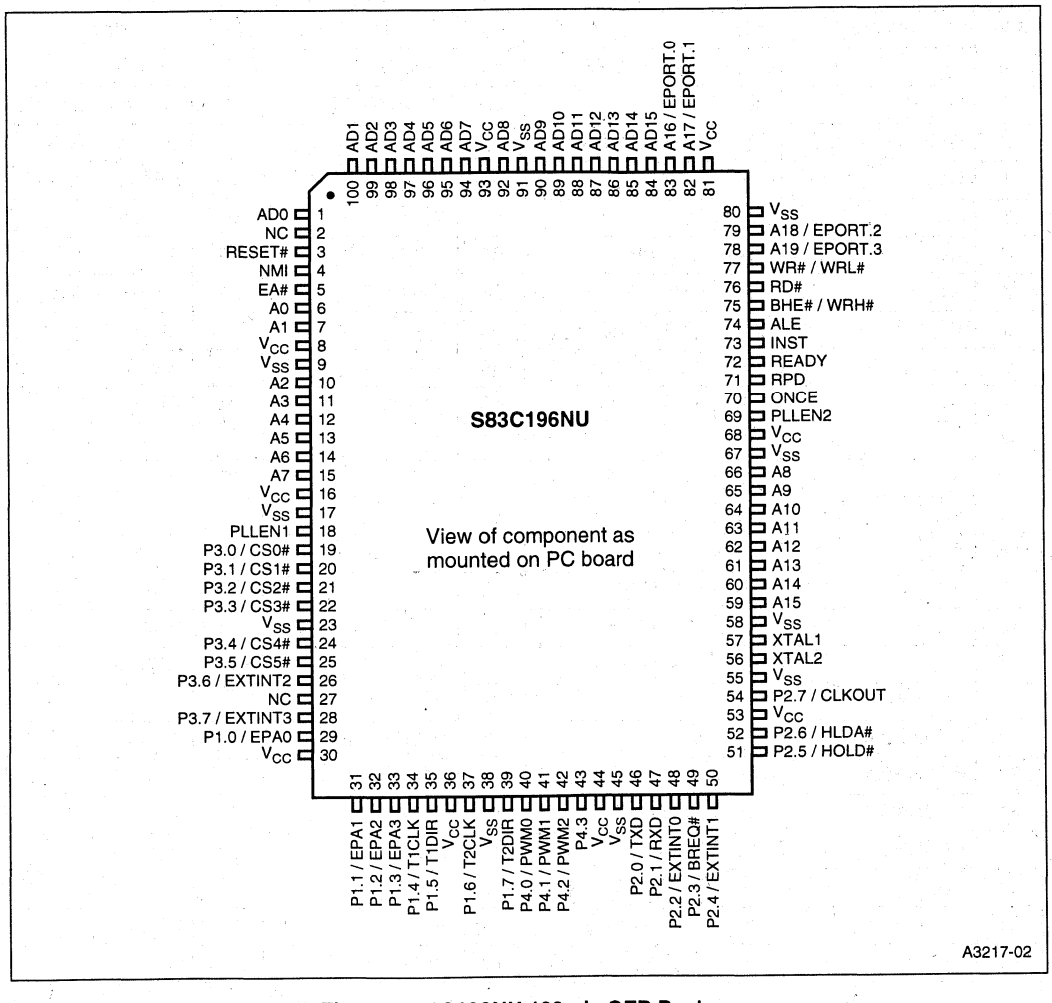


Figure 5. 83C196NU 100-pin QFP Package

Table 6. 83C196NU 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	NC	27	NC	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	V_{CC}	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	EA#	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	PLLEN1	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	PLLEN2	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

Table 7. 83C196NU 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	Pin
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88

Address & Data (continued)	
Name	Pin
AD12	87
AD13	86
AD14	85
AD15	84
Bus Control & Status	
Name	Pin
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	Pin
CLKOUT	54
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56
PLLEN1	18
PLLEN2	69
EA#	5

Input/Output	
Name	Pin
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EPA3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	Pin
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	53
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	80
V_{SS}	91

No Connection	
Name	Pin
NC	2
NC	27

4.0 SIGNALS

Table 8. Signal Descriptions

Name	Type	Description
A15:0	I/O	System Address Bus These address lines provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.
A19:16	I/O	Address Lines 16–19 These address lines provide address bits 16–19 during the entire external memory cycle, supporting extended addressing of the 1 Mbyte address space. **NOTE:** Internally, there are 24 address bits; however, only 20 external address pins (A19:0) are implemented. The internal address space is 16 Mbytes (000000–FFFFFFH) and the external address space is 1 Mbyte (00000–FFFFFH). The device resets to FF2080H in internal memory or F2080H in external memory. A19:16 are multiplexed with EPORT.3:0.
AD15:0	I/O	Address/Data Lines The functions of these pins depend on the bus size and mode. When a bus access is not occurring, these pins revert to their I/O port function. **16-bit Multiplexed Bus Mode**: AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **8-bit Multiplexed Bus Mode**: AD15:8 drive address bits 8–15 during the entire bus cycle. AD7:0 drive address bits 0–7 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **16-bit Demultiplexed Mode**: AD15:0 drive or receive data during the entire bus cycle. **8-bit Demultiplexed Mode**: AD7:0 drive or receive data during the entire bus cycle. AD15:8 drive the data that is currently on the high byte of the internal bus.
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A19:16 and AD15:0 for a multiplexed bus; A19:0 for a demultiplexed bus). ALE differs from ADV# in that it does not remain active during the entire bus cycle. An external latch can use this signal to demultiplex the address bits 0–15 from the address/data bus in multiplexed mode.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
BHE#	O	Byte High Enable†
		During 16-bit bus cycles, this active-low output signal is asserted for word reads and writes and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with A0, to determine which memory byte is being transferred over the system bus:
		BHE# A0 Byte(s) Accessed 0 0 both bytes 0 1 high byte only 1 0 low byte only
		BHE# is multiplexed with WRH#.
		† The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
BREQ#	O	Bus Request
		This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. When the bus-hold protocol is enabled (WSR.7 is set), the P2.3/BREQ# pin can function only as BREQ#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared).
		BREQ# is multiplexed with P2.3.
CLKOUT	O	Clock Output
		Output of the internal clock generator. The CLKOUT frequency is ½ the internal operating frequency (f). CLKOUT has a 50% duty cycle.
		CLKOUT is multiplexed with P2.7.
CS5#:0	O	Chip-select Lines 0–5
		The active-low output CS*x*# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select *x*. If the external memory address is outside the range assigned to the six chip selects, no chip-select output is asserted and the bus configuration defaults to the CS5# values.
		Immediately following reset, CS0# is automatically assigned to the range FF2000–FF20FFH (F2000–F20FFH if external).
		CS5:0# is multiplexed with P3.5:0.
EA#	I	External Access
		This active-low input signal determines whether memory accesses to special purpose and program memory partitions (FF2000–FFDFFFH) are directed to internal or external memory. These memory accesses are directed to internal memory if EA# is deasserted and to external memory if EA# is asserted. For an access to any other memory location, the value of EA# is irrelevant.
		EA# is not latched and can be switched dynamically during normal operating mode. Be sure to thoroughly consider the issues, such as different access times for internal and external memory, before using this dynamic switching capability.
		Always connect EA# to V_{SS} when using a microcontroller that has no internal nonvolatile memory.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
EPA3:0	I/O	Event Processor Array (EPA) Input/Output pins These are the high-speed input/output pins for the EPA capture/compare channels. For high-speed PWM applications, the outputs of two EPA channels (either EPA0 and EPA1 or EPA2 and EPA3) can be remapped to produce a PWM waveform on a shared output pin. EPA3:0 are multiplexed with P1.3:0.
EPORT.3:0	I/O	Extended Addressing Port This is a standard, 4-bit, bidirectional I/O port. EPORT.3:0 are multiplexed with A19:16.
EXTINT3:0	I	External Interrupts In normal operating mode, a rising edge on EXTINT*x* sets the EXTINT*x* interrupt pending bit. EXTINT*x* is sampled during phase 2 (CLKOUT high). The minimum high time is one state time. In standby and powerdown modes, asserting the EXTINT*x* signal for at least 50 ns causes the device to resume normal operation. The interrupt need not be enabled, but the pin must be configured as a special-function input. If the EXTINT*x* interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation. EXTINT0 is multiplexed with P2.2, EXTINT1 is multiplexed with P2.4, EXTINT2 is multiplexed with P3.6, and EXTINT3 is multiplexed with P3.7.
HLDA#	O	Bus Hold Acknowledge This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#. When the bus-hold protocol is enabled (WSR.7 is set), the P2.6/HLDA# pin can function only as HLDA#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). HLDA# is multiplexed with P2.6.
HOLD#	I	Bus Hold Request An external device uses this active-low input signal to request control of the bus. When the bus-hold protocol is enabled (WSR.7 is set), the P2.5/HOLD# pin can function only as HOLD#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). HOLD# is multiplexed with P2.5.
INST	O	Instruction Fetch This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
NMI	I	Nonmaskable Interrupt In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.
ONCE	I	On-circuit Emulation Holding ONCE high during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. This mode puts all pins into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator. To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent accidental entry into ONCE mode, connect the ONCE pin to V_{SS}.
P1.7:0	I/O	Port 1 This is a standard bidirectional port that is multiplexed with individually selectable special-function signals. Port 1 is multiplexed as follows: P1.0/EPA0, P1.1/EPA1, P1.2/EPA2, P1.3/EPA3, P1.4/T1CLK, P1.5/T1DIR, P1.6/T2CLK, and P1.7/T2DIR.
P2.7:0	I/O	Port 2 This is a standard bidirectional port that is multiplexed with individually selectable special-function signals. Port 2 is multiplexed as follows: P2.0/TXD, P2.1/RXD, P2.2/EXTINT0, P2.3/BREQ#, P2.4/EXTINT1, P2.5/HOLD#, P2.6/HLDA#, and P2.7/CLKOUT.
P3.7:0	I/O	Port 3 This is an 8-bit, bidirectional, standard I/O port. Port 3 is multiplexed as follows: P3.0/CS0#, P3.1/CS1#, P3.2/CS2#, P3.3/CS3#, P3.4/CS4#, P3.5/CS5#, P3.6/EXTINT2, and P3.7/EXTINT3.
P4.3:0	I/O	Port 4 This is a 4-bit, bidirectional, standard I/O port with high-current drive capability. Port 4 is multiplexed as follows: P4.0/PWM0, P4.1/PWM1, and P4.2/PWM2. P4.3 is not multiplexed.
PLLEN2:1	I	Phase-locked Loop 1 and 2 Enable These input pins are used to enable the on-chip clock multiplier feature and select either the doubled or quadrupled clock speed as follows: **PLLEN2** **PLLEN1** **Mode** 0 0 Standard mode; clock multiplier circuitry disabled. Internal clock equals the XTAL1 input frequency. 1 0 Reserved† 0 1 Doubled mode; clock multiplier circuitry enabled. Internal clock is twice the XTAL1 input frequency. 1 1 Quadrupled mode; clock multiplier circuitry enabled. Internal clock is four times the XTAL1 input frequency. † This reserved combination causes the device to enter an unsupported test mode.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
PWM2:0	O	Pulse Width Modulator Outputs These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable. PWM2:0 are multiplexed with P4.2:0.
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads.
READY	I	Ready Input This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states in addition to the wait states that are generated internally. When READY is high, CPU operation continues in a normal manner with wait states inserted as programmed in the chip configuration registers or the chip-select *x* bus control register. READY is ignored for all internal memory accesses.
RESET#	I/O	Reset A level-sensitive reset input to and open-drain system reset output from the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown, standby, and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. If the phase-locked loop (PLL) clock circuitry is enabled, you must hold RESET# low for at least 2 ms to allow the PLL to stabilize before the internal CPU and peripheral clocks are enabled. After a device reset, the first instruction fetch is from FF2080H (or F2080H in external memory). The program and special-purpose memory locations (FF2000–FF2FFFH) reside in external memory.
RPD	I	Return from Powerdown Timing pin for the return-from-powerdown circuit. If your application uses powerdown mode, connect a capacitor between RPD and V_{SS} if **either** of the following conditions is true: • the internal oscillator is the clock source • the phase-locked loop (PLL) circuitry is enabled (see PLLEN2:1 signal description) The capacitor causes a delay that enables the oscillator and PLL circuitry to stabilize before the internal CPU and peripheral clocks are enabled. The capacitor is not required if your application uses powerdown mode and if **both** of the following conditions are true: • an external clock input is the clock source • the phase-locked loop circuitry is disabled If your application does not use powerdown mode, leave this pin unconnected.
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data. RXD is multiplexed with P2.1.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
T1CLK	I	Timer 1 External Clock External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode. **and** External clock for the serial I/O baud-rate generator input (program selectable). T1CLK is multiplexed with P1.4.
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. Also used in conjunction with T2DIR for quadrature counting mode. T2CLK is multiplexed with P1.6.
T1DIR	I	Timer 1 External Direction External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode. T1DIR is multiplexed with P1.5.
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. Also used in conjunction with T2CLK for quadrature counting mode. T2DIR is multiplexed with P1.7.
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmits serial port output data. In mode 0, it is the serial clock output. TXD is multiplexed with P2.0.
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{SS}	GND	Digital Circuit Ground Connect each V_{SS} pin to ground through the lowest possible impedance path.
WR#	O	Write† This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. WR# is multiplexed with WRL#. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRH#	O	Write High† During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. WRH# is multiplexed with BHE#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.

Table 8. Signal Descriptions (Continued)

Name	Type	Description
WRL#	O	Write Low[†] During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# is multiplexed with WR#. [†] The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator, phase-locked loop circuitry, and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1 (see datasheet).
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses a external clock source instead of the on-chip oscillator.

5.0 ADDRESS MAP

Table 9. 8XC196NU Address Map

Hex Address	Description	Addressing Modes
FF FFFFH FF E000H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF DFFFH FF 2080H	Program memory (Note 1)	Indirect, indexed, extended
FF 207FH FF 2000H	Special-purpose memory (Note 1)	Indirect, indexed, extended
FF 1FFFH FF 0100H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
FF 00FFH FF 0000H	Reserved for ICE (Note 2)	—
FE FFFFH 0F 0000H	Overlaid memory (reserved for future devices) (Note 2)	Indirect, indexed, extended
0E FFFFH 01 0000H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
00 FFFFH 00 E000H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
00 DFFFH 00 2000H	External device (memory or I/O) connected to address/data bus or remapped internal ROM (determined by EA# pin) (Note 3)	Indirect, indexed, extended
00 1FFFH 00 1F00H	Internal peripheral special-function registers (SFRs) (Note 4)	Indirect, indexed, extended, windowed direct
00 1EFFH 00 0400H	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
00 03FFH 00 0100H	Upper register file (general-purpose register RAM)	Indirect, indexed, windowed direct
00 00FFH 00 001AH	Lower register file (general-purpose register RAM)	Direct, indirect, indexed, windowed direct
00 0019H 00 0018H	Lower register file (stack pointer)	Direct, indirect, indexed, windowed direct
00 0017H 00 0000H	Lower register file (CPU SFRs) (Note 4)	Direct, indirect, indexed, windowed direct

NOTES:
1. For the 80C196NU, the program and special-purpose memory locations (FF2000–FFDFFFH) reside in external memory. For the 83C196NU, these locations can reside either in external memory or in internal ROM.
2. Locations *x*F0000–*x*F00FFH are reserved, write 0FFH to these locations.
3. For the 80C196NU, this address range (FF2080–FFDFFFH) is always external memory. For the 83C196NU, this address range is mapped into internal ROM if the REMAP bit (CCB1.2) is set and EA# is at logic 1. Otherwise, they are mapped to external memory.
4. Unless otherwise noted, write 0 to reserved SFR bits.

6.0 ELECTRICAL CHARACTERISTICS

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... –60°C to +150°C
Supply Voltage with Respect to V_{SS} ..... –0.5 V to +7.0 V
Power Dissipation ..... 1.5 W

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
F_{XTAL1} (Input frequency for V_{CC} = 4.5 V – 5.5 V)
(Note 1, 2, 3) ..... 16 MHz to 50 MHz

NOTES:
1. This device is static and should operate below 1 Hz, but has been tested only down to 16 MHz.
2. The maximum crystal that can be used is 25 MHz.
3. The minimum XTAL1 frequency when using the PLL is 8 MHz.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.1 DC Characteristics

Table 10. DC Characteristics Over Specified Operating Conditions

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		90	120	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V Device in Reset
I_{IDLE}	Idle Mode Current		45	60	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V
I_{PD}	Powerdown Mode Current		20	50	µA	V_{CC} = 5.5 V (Note 2)
I_{STDBY}	Standby Mode		8	15	mA	V_{CC} = 5.5 V
I_{LI}	Input Leakage Current (Standard Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage (all pins)	–0.5		0.8	V	
V_{IH}	Input High Voltage	0.2 V_{CC} + 1		V_{CC} + 0.5	V	
V_{IL1}	Input Low Voltage XTAL1	–0.5		0.3 V_{CC}	V	
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (Reset pin) (Note 3)	0.2 V_{CC} + 1.4		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (output configured as complementary) (Note 4, 5)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (output configured as complementary) (Note 5)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA

NOTES:
1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. B-step only.
4. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
5. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

6. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
7. Pin capacitance is not tested. This value is based on design simulations.

Table 10. DC Characteristics Over Specified Operating Conditions (Continued)

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
V_{OL1}	Output Low Voltage on P4.*x* (output configured as complementary) (Note 5)			0.45 0.6	V V	I_{OL} = 10 mA I_{OL} = 15 mA
V_{OL2}	Output Low Voltage in RESET on ALE, INST, and NMI			0.45	V	I_{OL} = 3 µA
V_{OH1}	Output High Voltage in RESET (Note 6)	V_{CC} – 0.7			V	I_{OH} = –3 µA
V_{OL3}	Output Low Voltage in RESET for ONCE pin			0.45	V	I_{OL} = 30 µA
V_{OL4}	Output Low Voltage on XTAL2			0.3 0.45 1.5	V V V	I_{OL} = 100 µA I_{OL} = 700 µA I_{OL} = 3 mA
V_{OH2}	Output High Voltage on XTAL2	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –100 µA I_{OH} = –700 µA I_{OH} = –3 mA
V_{TH+} – V_{TH-}	Hysteresis voltage width on RESET# pin		0.3		V	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 7)			10	pF	
R_{RST}	RESET Pull-up Resistor	9		95	kΩ	V_{CC} = 5.5 V, V_{IN} = 4.0 V

NOTES:

1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. B-step only.
4. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
5. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

6. For all pins that were weakly pulled high during RESET. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
7. Pin capacitance is not tested. This value is based on design simulations.

6.2 AC Characteristics

6.2.1 RELATIONSHIP OF XTAL1 TO CLKOUT

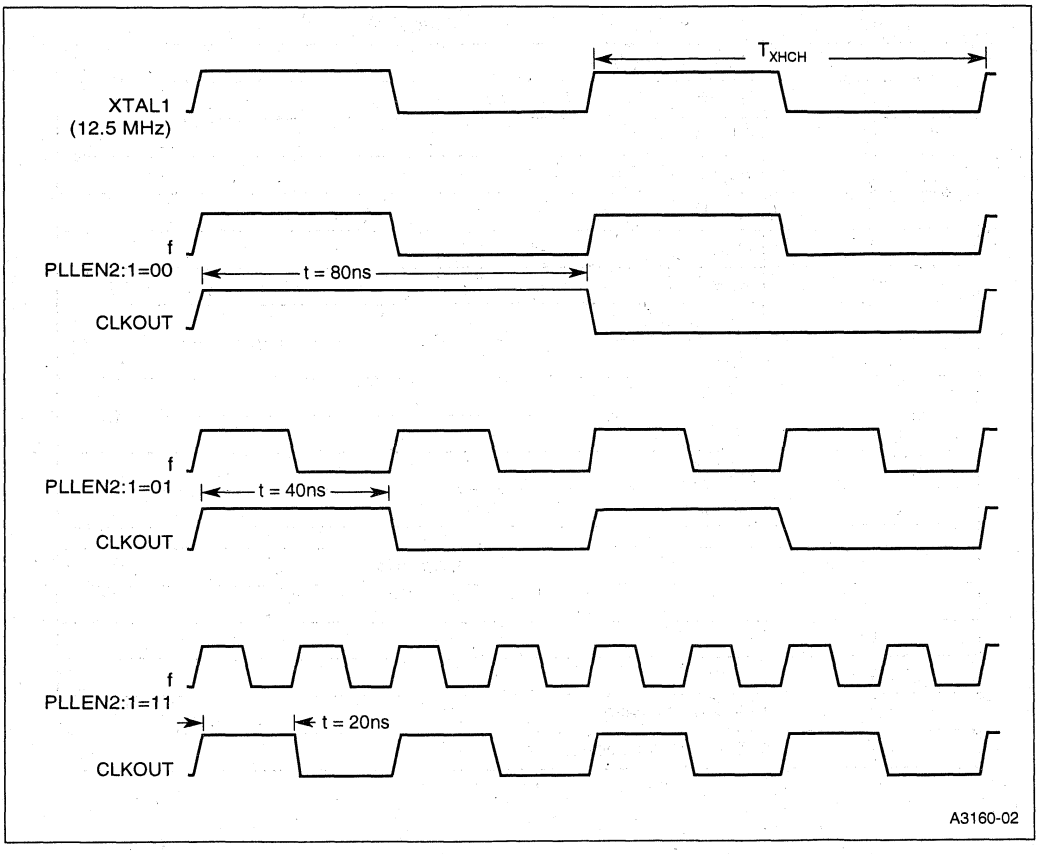


Figure 6. Effect of Clock Mode on CLKOUT

6.2.2 EXPLANATION OF AC SYMBOLS

Each AC timing symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Table 11. AC Timing Symbol Definitions

Character	Signal(s)
A	AD15:0, A19:0
B	BHE#
C	CLKOUT
D	AD15:0, AD7:0
H	HOLD#
HA	HLDA#
L	ALE
Q	AD15:0, AD7:0
R	RD#
S	CS*x*#
W	WR#, WRL#
X	XTAL1
Y	READY

Character	Condition
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating (low impedance)

6.2.3 AC CHARACTERISTICS — MULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 12. AC Characteristics the 8XC196NU Will Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{XHCH}	XTAL1 Rising Edge to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{AVWL}	Address Valid to WR# Falling Edge	2t – 25		ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	– 10	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	– 15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (3)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{AVLL}	Address Valid to ALE Falling Edge	t – 14		ns
T_{LLAX}	Address Hold after ALE Falling Edge	t – 10		ns
T_{LLRL}	ALE Falling Edge to RD# Falling Edge	t – 15		ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	– 10	20	ns
T_{RLRH}	RD# Low Period	t – 10		ns (3)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 5	t + 15	ns (4)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Falling Edge to WR# Falling Edge	t – 11		ns
T_{QVWH}	Data Stable to WR# Rising Edge	t – 14		ns (3)
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 15	5	ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 12. AC Characteristics the 8XC196NU Will Meet, Multiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WLWH}	WR# Low Period	t – 10		ns (3)
T_{WHQX}	Data Hold after WR# Rising Edge	t – 7		ns
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 14	t + 20	ns
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge A-step B-step	 t – 4 0		ns
T_{WHAX}	AD15:8 Hold after WR# Rising Edge	t – 4		ns (5)
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge A-step B-step	 t 0		ns
T_{RHAX}	AD15:8 Hold after RD# Rising Edge	t		ns (5)
T_{WHSH}	A19:16, CS# Hold after WR# Rising Edge	0		ns
T_{RHSH}	A19:16, CS# Hold after RD# Rising Edge	0		ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 13. AC Characteristics the External Memory System Must Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	AD15:0 Valid to Input Data Valid		3t – 32	ns (1)
T_{RLDV}	RD# Active to Input Data Valid		t – 22	ns (1)
T_{SLDV}	Chip Select Low to Data Valid		4t – 32	ns (1)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t – 5	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{AVYV}	AD15:0 Valid to READY Setup		2t – 38	ns (2)
T_{CLYX}	READY Hold after CLKOUT Low	0	2t – 36	ns (3)
T_{YLYH}	Non-READY Time	No Upper Limit		ns

NOTES:
1. If wait states are used, add $2t \times n$, where n = number of wait states.
2. When forcing wait states using the BUSCON register, add $2t \times n$.
3. Exceeding the maximum specification causes additional wait states.

6.2.3.1 System Bus Timings, Multiplexed Bus

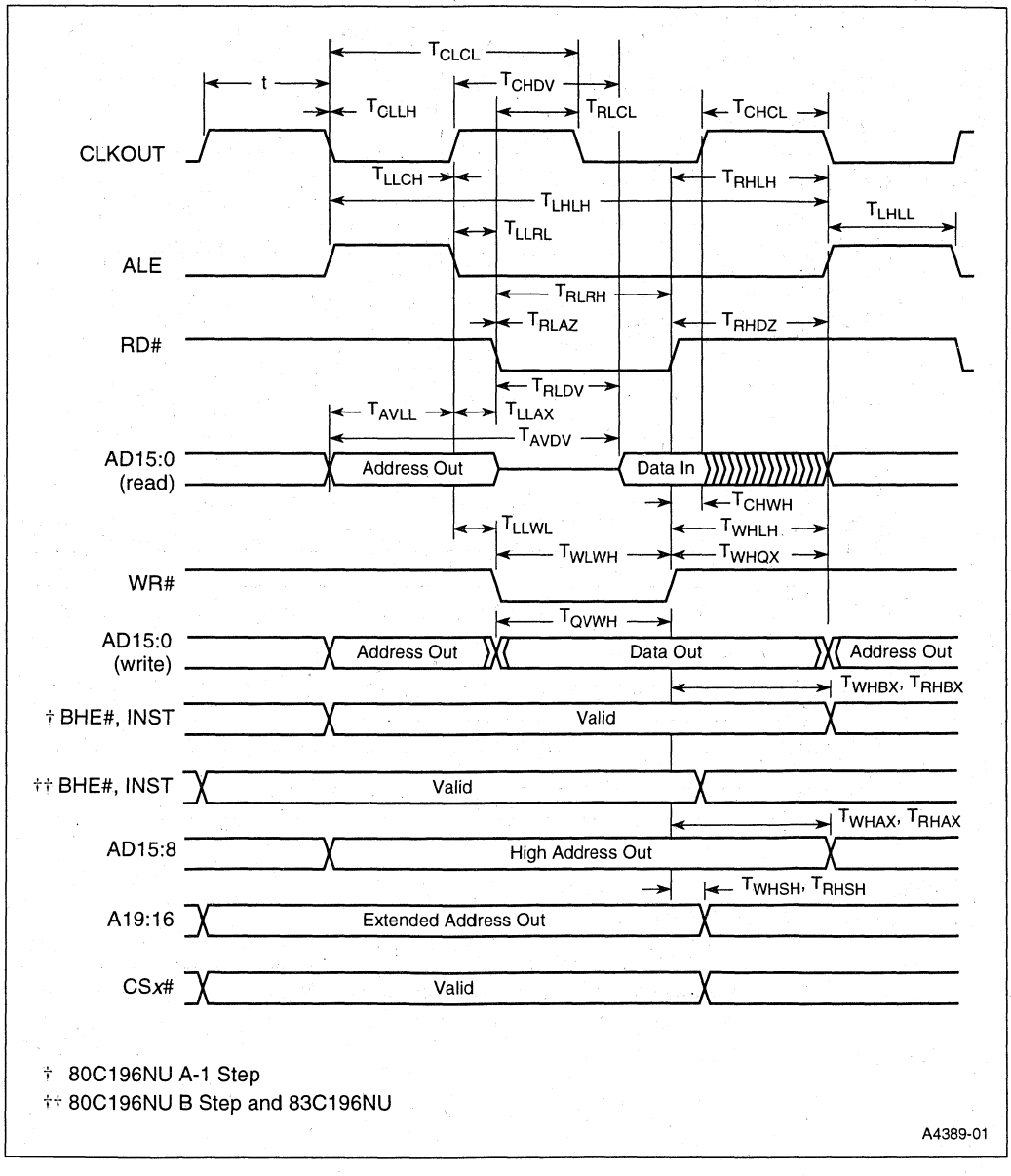


Figure 7. System Bus Timings, Multiplexed Bus Mode

6.2.3.2 READY Timing, Multiplexed Bus

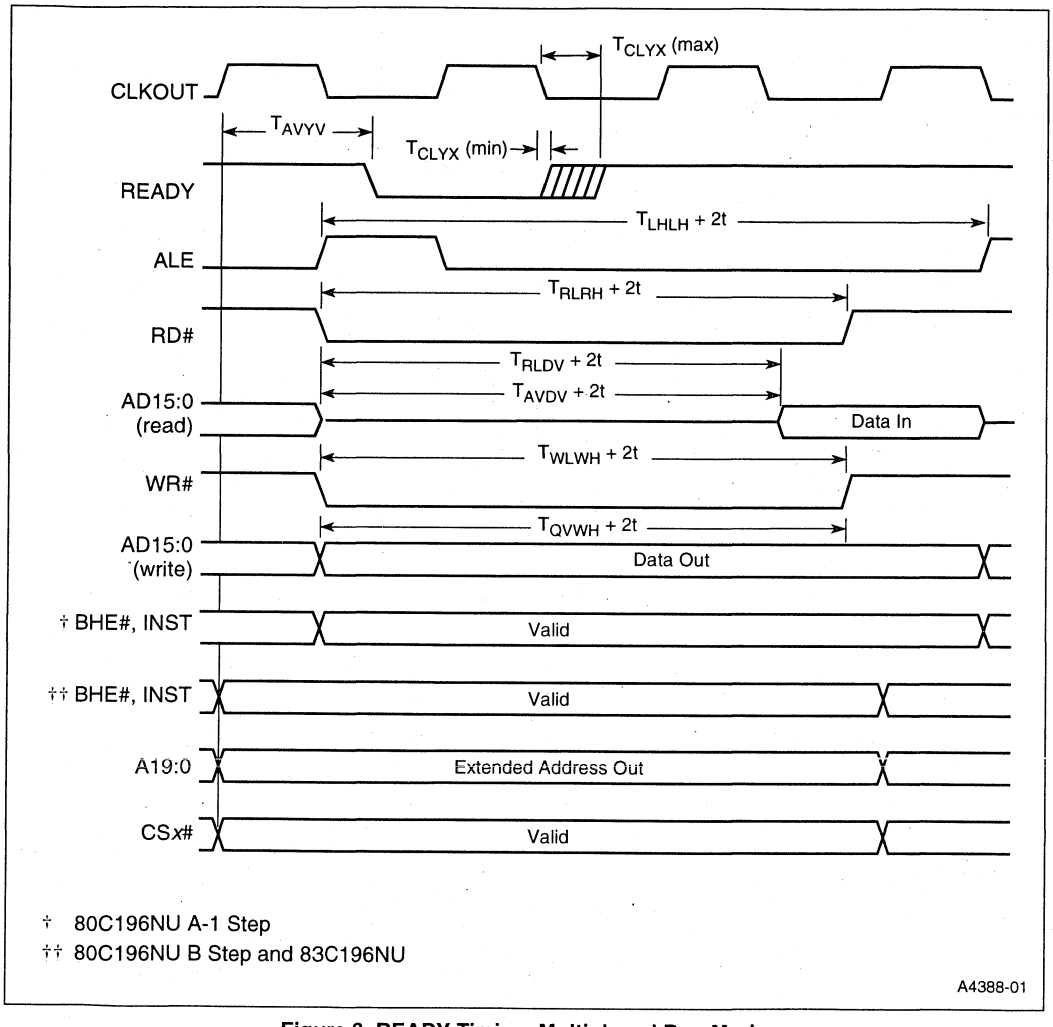


Figure 8. READY Timing, Multiplexed Bus Mode

6.2.4 AC CHARACTERISTICS — DEMULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 14. AC Characteristics the 8XC196NU Will Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{AVWL}	Address Valid to WR# Falling Edge	t – 8		ns(3)
T_{AVRL}	Address Valid to RD# Falling Edge	t – 8		ns(3)
T_{RHRL}	Read High to Next Read Low	t – 5		ns(3)
T_{XHCH}	XTAL1 High to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	– 10	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	– 15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (3,4,5)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	– 5	11	ns
T_{RLRH}	RD# Low Period	3t – 18		ns (4)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 4	t + 15	ns (3)
T_{WLCL}	WR# Low to CLKOUT Falling Edge	– 8	5	ns
T_{QVWH}	Data Stable to WR# Rising Edge	3t – 25		ns (4)
T_{CHWH}	CLKOUT High to WR# Rising Edge	– 11	10	ns
T_{WLWH}	WR# Low Period	3t – 18		ns (4)
T_{WHQX}	Data Hold after WR# Rising Edge	t	t + 20	ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. For deferred bus cycle, add 2t (1 state) if CS*x*# changes or if the write cycle follows a read cycle.
4. If wait states are used, add 2t × *n*, where *n* = number of wait states.
5. Assuming back-to-back bus cycles.

Table 14. AC Characteristics the 8XC196NU Will Meet, Demultiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 5	t + 10	ns (3)
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge A-step B-step	 t – 5 0		ns
T_{WHAX}	A19:0, CS*x*# Hold after WR# Rising Edge	0		ns
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge A-step B-step	 t – 5 0		ns
T_{RHAX}	A19:0, CS*x*# Hold after RD# Rising Edge	0		ns

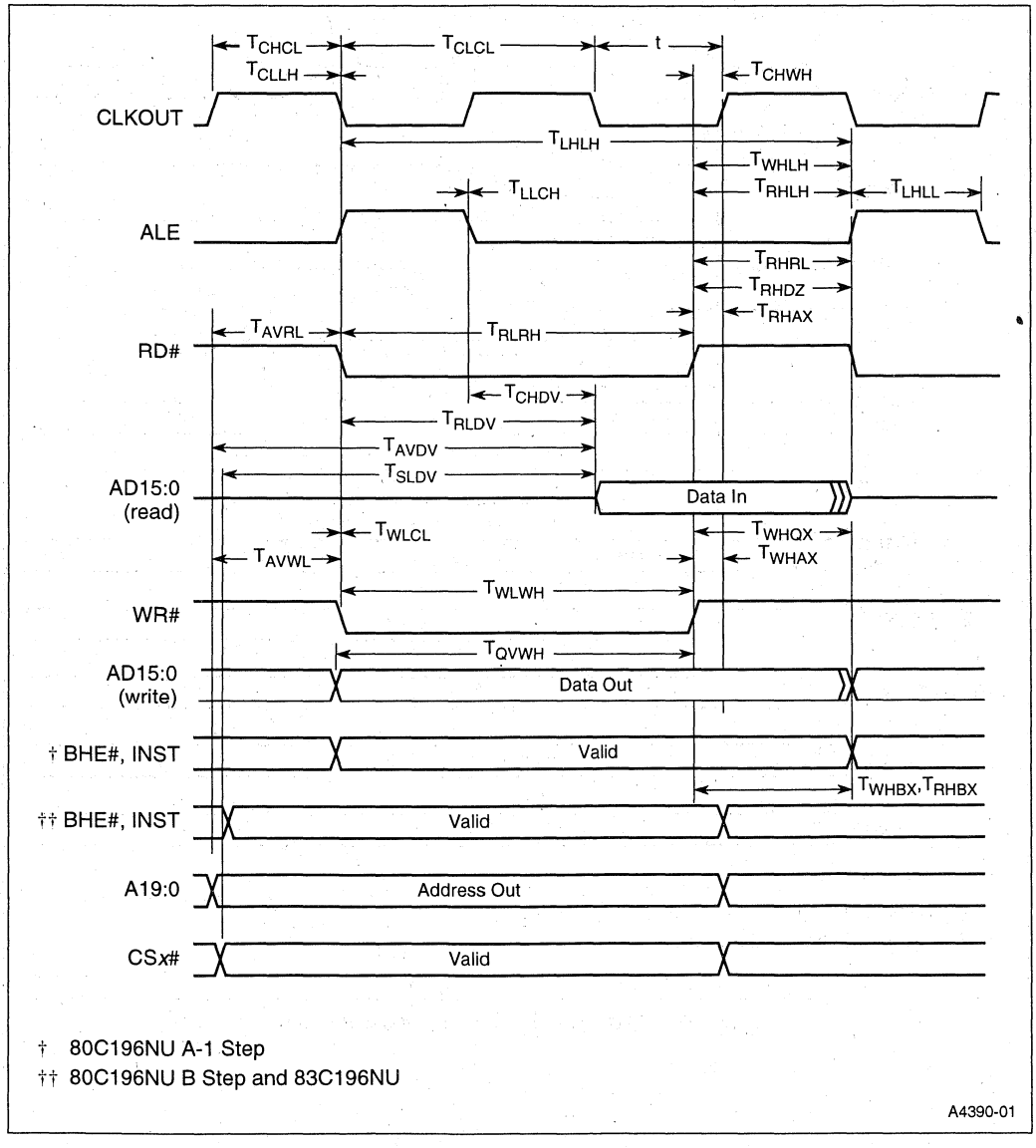
NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. For deferred bus cycle, add 2t (1 state) if CS*x*# changes or if the write cycle follows a read cycle.
4. If wait states are used, add 2t × *n*, where *n* = number of wait states.
5. Assuming back-to-back bus cycles.

Table 15. AC Characteristics the External Memory System Must Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	A19:0 Valid to Input Data Valid		4t – 30	ns (1,2)
T_{RLDV}	RD# Active to Input Data Valid		3t – 35	ns (1)
T_{SLDV}	Chip Select Low to Data Valid		4t – 30	ns (1,2)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t	ns(2)
T_{RXDX}	Data Hold after RD# Inactive	0		ns
T_{AVYV}	A19:0 Valid to READY Setup		3t – 45	ns (3)
T_{CLYX}	READY Hold after CLKOUT Low	0	2t – 36	ns (4)
T_{YLYH}	Non READY Time	No Upper Limit		ns

NOTES:
1. If wait states are used, add 2t × *n*, where *n* = number of wait states.
2. For deferred bus cycle, add 2t (1 state) if CS*x*# changes or if the write cycle follows a read cycle.
3. When forcing wait states using the BUSCON register, add 2t × *n*.
4. Exceeding the maximum specification causes additional wait states.

6.2.4.1 System Bus Timings, Demultiplexed Bus



† 80C196NU A-1 Step
†† 80C196NU B Step and 83C196NU

A4390-01

Figure 9. System Bus Timings, Demultiplexed Bus Mode

6.2.4.2 READY Timing, Demultiplexed Bus

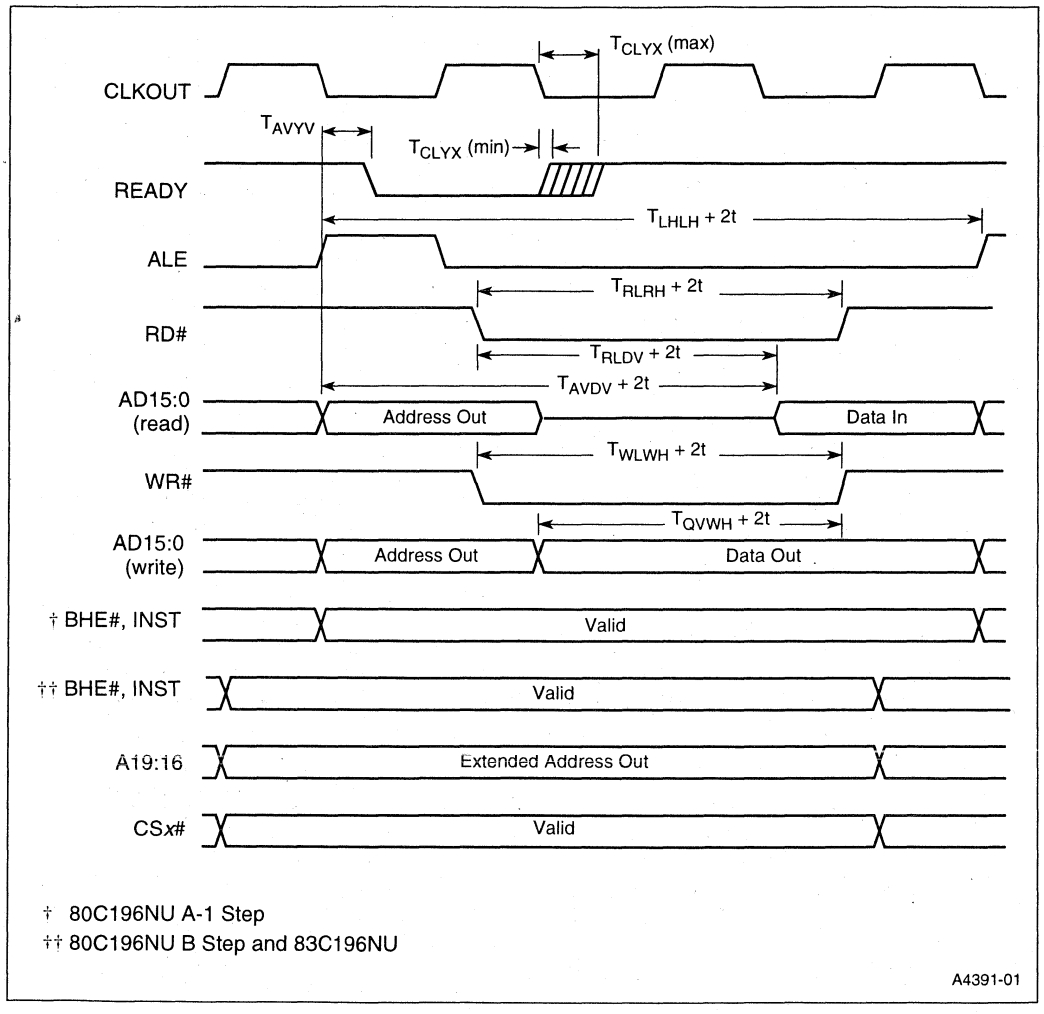


Figure 10. READY Timing, Demultiplexed Bus Mode

6.2.4.3 8XC196NU Deferred Bus Timing Mode

The deferred bus cycle mode (enabled by setting CCB1.5) is designed to reduce bus contention when using the 8XC196NU in demultiplexed mode with slow memories. When the deferred mode is enabled, a delay will occur (equal to 2t) in the first bus cycle following a chip-select change or the first write cycle following a read cycle. This mode will work in parallel with wait states. Refer to Figure 11 to determine which control signals are affected.

Cycle 1 is a normal 4t read cycle. Cycle 2 is a write cycle that follows a read cycle, so a 2t delay is inserted. Notice that the chip-select change at the beginning of cycle 2 did not cause a double delay (4t). The chip-select change in cycle 3, a read cycle, causes a 2t delay.

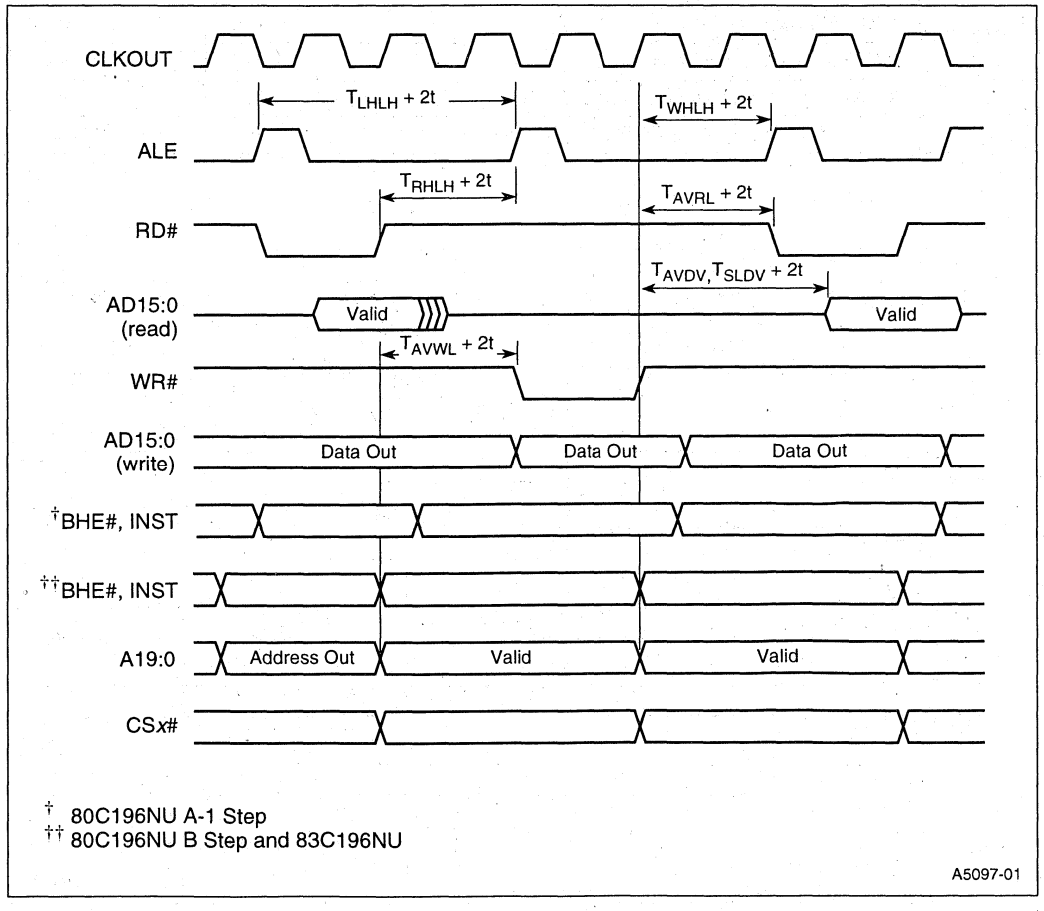


Figure 11. Deferred Bus Mode Timing Diagram

6.2.5 HOLD#, HLDA# TIMINGS

Table 16. HOLD#, HLDA# Timings

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD# Setup Time (To guarantee recognition at next clock)	65		ns
T_{CLHAL}	CLKOUT Low to HLDA# Low	–15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	–15	15	ns
T_{HALAZ}	HLDA# Low to Address Float		33	ns
T_{HALBZ}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	–25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	–25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	–20		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	–20		ns

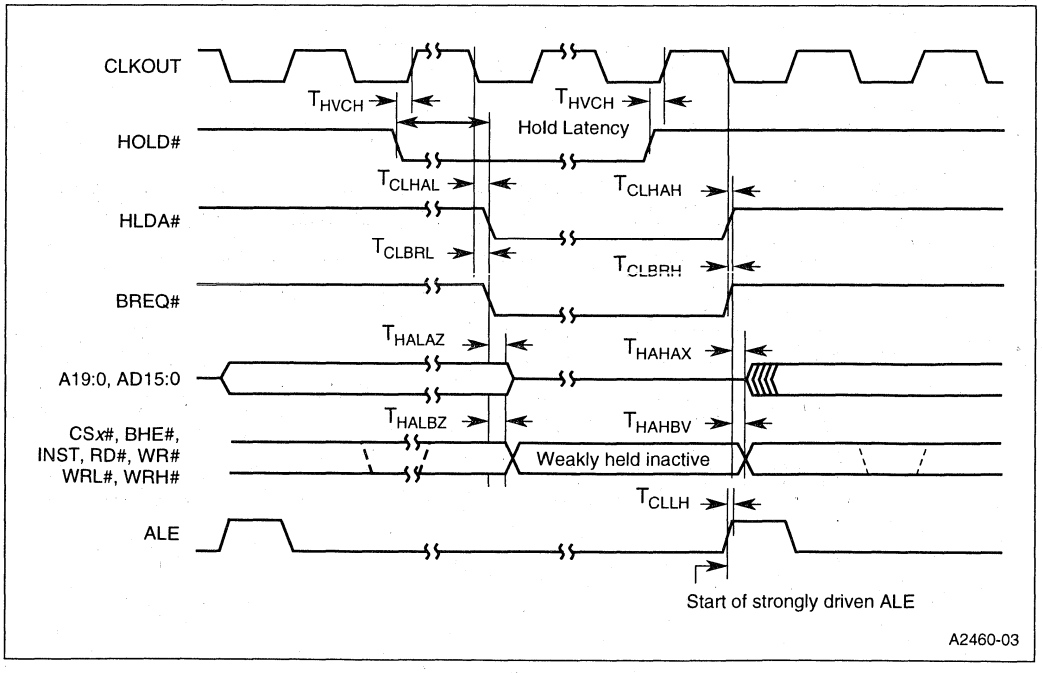


Figure 12. HOLD#, HLDA# Timing Diagram

6.2.6 AC CHARACTERISTICS — SERIAL PORT, SYNCHRONOUS MODE 0

Table 17. Serial Port Timing — Synchronous Mode 0

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock period			
	SP_BAUD ≥ *x*002H	6t		ns
	SP_BAUD = *x*001H (Note 1)	4t		ns
T_{XLXH}	Serial Port Clock falling edge to rising edge			
	SP_BAUD ≥ *x*002H	4t – 27	4t + 27	ns
	SP_BAUD = *x*001H (Note 1)	2t – 27	2t + 27	ns
T_{QVXH}	Output data setup to clock high	4t – 30		ns
T_{XHQX}	Output data hold after clock high	2t – 30		ns
T_{XHQV}	Next output data valid after clock high		2t + 30	ns
T_{DVXH}	Input data setup to clock high	2t + 30		ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		t + 30	ns

NOTE:
1. The minimum baud-rate (SP_BAUD) register value for receive is *x*002H and the minimum baud-rate (SP_BAUD) register value for transmit is *x*001H.

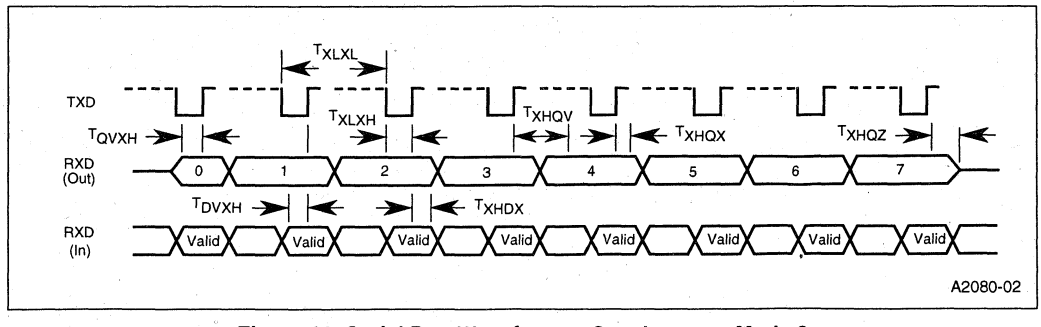


Figure 13. Serial Port Waveform — Synchronous Mode 0

6.2.7 EXTERNAL CLOCK DRIVE

Table 18. External Clock Drive

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	External Input Frequency ($1/T_{XLXL}$), PLL disabled	16	50†	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 2x mode	8	25	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 4x mode	8	12.5	MHz
T_{XTAL1}	Oscillator Period (T_{XLXL}), PLL disabled	20	62.5	ns
	Oscillator Period (T_{XLXL}), PLL in 2x mode	40	125	ns
	Oscillator Period (T_{XLXL}), PLL in 4x mode	80	125	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

† Assumes an external clock; the maximum input frequency for an external crystal oscillator is 25 MHz.

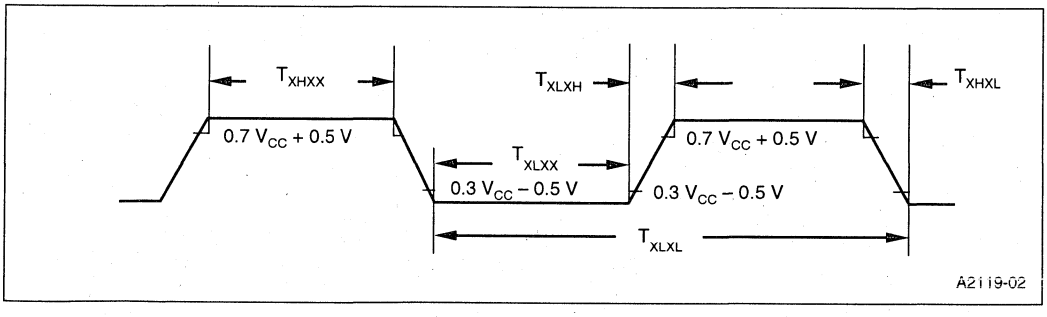


Figure 14. External Clock Drive Waveforms

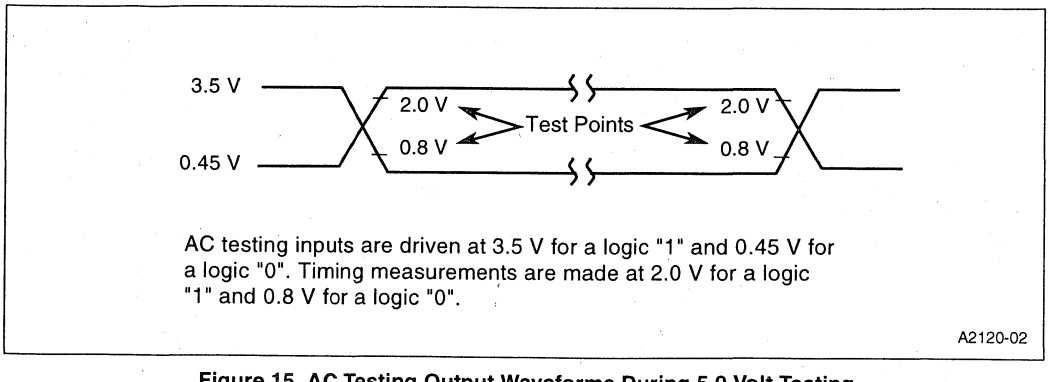


Figure 15. AC Testing Output Waveforms During 5.0 Volt Testing

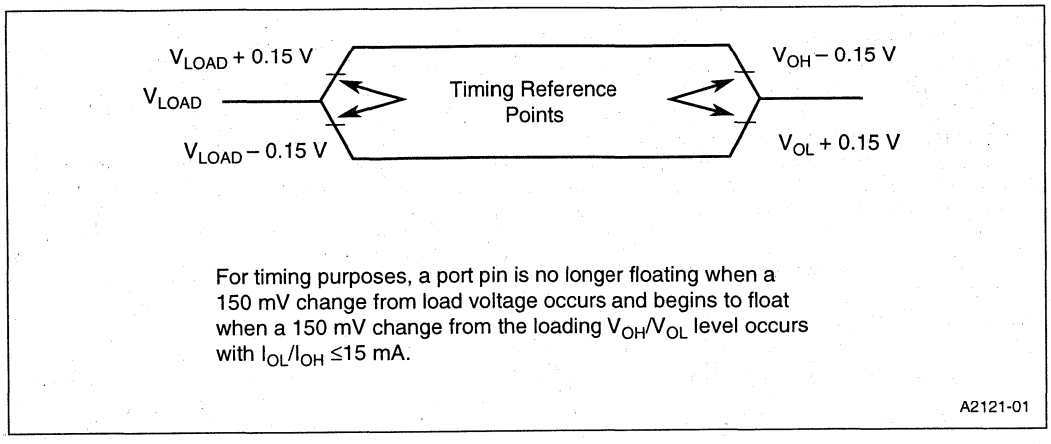


Figure 16. Float Waveforms During 5.0 Volt Testing

7.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 19. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
100-pin QFP 80C196NU	55°C/W	11°C/W
100-pin SQFP 80C196NU	66°C/W	16.5°C/W
100-pin QFP 83C196NU	55°C/W	11°C/W

8.0 8XC196NU ERRATA

The 8XC196NU may contain design defects or errors known as errata. Characterized errata that may cause the 8XC196NU's behavior to deviate from published specifications are documented in the *8XC196NU Specification Update* (272864-001). Specification updates can be obtained from your local Intel sales office or from the World Wide Web (*www.intel.com*).

9.0 DATASHEET REVISION HISTORY

This datasheet is valid for devices with a "B" or "C" designation at the end of the topside tracking number. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This is the -003 version of the datasheet. The following changes were made in this version:

1. A heading was added for Section 1.0, "Product Overview," and the remaining sections were renumbered.
2. List of features, the 8XC196NU has four options (0–3) for programmable wait states for each chip select, not sixteen (0–15) as previously stated.
3. The ROM SQFP (SB83C196NU) pinout and pin assignment tables have been deleted.
4. Figure 5, package designator in diagram changed to "S" from "SB" to correctly indicate the QFP package type.
5. Table 8, EA# signal description added.
6. Table 8, signal descriptions for BREQ#, HLDA#, HOLD#, PLLEN2:1, and RESET# have been modified.
7. Table 9, redesigned and footnotes reordered.
8. Table 10, V_{IH2} specification added with footnote.
9. Figure 6, corrected to state PLLEN2:1=01 (not PLLEN2:1=10).
10. Tables 12 and 14, B-step timing added for T_{WHBX} min and T_{RHBX} min.
11. Table 12, deleted notes 4 and 5, added note 2, and reordered remaining notes.
12. Table 13, deleted notes 1, 3, and 6 and reordered remaining notes.
13. Table 14, deleted notes 4, 5, and 6, added note 2, and reordered remaining notes.
14. Table 15, deleted notes 1, 3, and 6 and reordered remaining notes.
15. Tables 13 and 15, the minimum timing for T_{RXDX} improved from 2 ns to 0 ns.
16. Figures 7–11, updated to reflect both A- and B-step timings on the BHE#, INST signal.
17. Section 5.4.3, the second sentence of the first paragraph, the word "and" replaced by "or".
18. Table 19, thermal characteristics specifications have been changed and expanded.
19. The errata list was replaced with a reference to the specification update document.

The following changes were made in the -002 version of the datasheet:

1. The input frequency on XTAL1, formerly called F_{OSC}, is now called F_{XTAL1}. The internal operating frequency and operating period are denoted by (f) and (t), respectively.
2. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
3. The minimum frequency input with PLL in 4x mode has changed from 4 MHz to 8MHz.
4. The AC characteristics tables have been divided into the following: the timing specifications met by the device, and the timing specifications that must be met by the external memory system.
5. Electrical characteristics notes #2 and #3 added to section 3.0.
6. Maximum I_{OL} and I_{OH} specifications added to

the DC characteristics tables.

7. AC timings T_{AVWL} and T_{SLDV} added to the AC characteristics–multiplexed bus mode tables.
8. Figure 7 added, and figures 8–12 have been revised.
9. Thermal characteristics for the 100-pin SQFP package have been added in section 1.0.
10. Specifications for the 83C196NU have been added.
11. Several AC timing specifications have changed.

ADVANCE INFORMATION

80296SA COMMERCIAL CHMOS 16-BIT MICROCONTROLLER

- 50 MHz Operation†
- 6 Mbytes of Linear Address Space
- 512 Bytes of Register RAM
- 2 Kbytes of Code/Data RAM
- Register-register Architecture
- Footprint and Functionally Compatible Upgrade for the 8XC196NP and 80C196NU
- Optional Phase-locked Loop (PLL) Circuitry with 2x or 4x Clock Multiplier
- 32 I/O Port Pins
- 19 Interrupt Sources, 14 with Programmable Priorities
- 4 External Interrupt Pins and NMI Pin
- 2 Flexible 16-bit Timer/Counters with Quadrature Counting Capability
- 3 Pulse-width Modulator (PWM) Outputs with High Drive Capability
- Full-duplex Serial Port with Dedicated Baud-rate Generator

† 40 MHz standard; 50 MHz is Speed Premium

- Chip-select Unit
  - 6 Chip-select Pins
  - Dynamic Demultiplexed/Multiplexed Address/Data Bus for Each Chip Select
  - Programmable Wait States (0–15) for Each Chip Select
  - Programmable Bus Width (8- or 16-bit) for Each Chip Select
  - Programmable Address Range for Each Chip Select
- Event Processor Array (EPA) with 4 High-speed Capture/Compare Channels
- Multiply and Accumulate Executes in 80 ns Using the 40-bit Hardware Accumulator
- 880 ns 32/16 Unsigned Division
- 100-pin SQFP or 100-pin QFP Package
- Complete System Development Support
- High-speed CHMOS Technology

The 80296SA is a member of Intel's 16-bit MCS® 96 microcontroller family. The 80296SA features 6 Mbytes of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation. The device has hardware and instructions to support various digital signal processing algorithms.

NOTE

This datasheet contains information on products being sampled or in the initial production phase of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 272748-002

1.0 PRODUCT OVERVIEW

The 80296SA is a member of Intel's 16-bit MCS® 96 microcontroller family. The 80296SA features 6 Mbytes of linear address space, a demultiplexed bus, and a chip-select unit. The external bus can dynamically switch between multiplexed and demultiplexed operation. The device has hardware and instructions to support various digital signal processing algorithms.

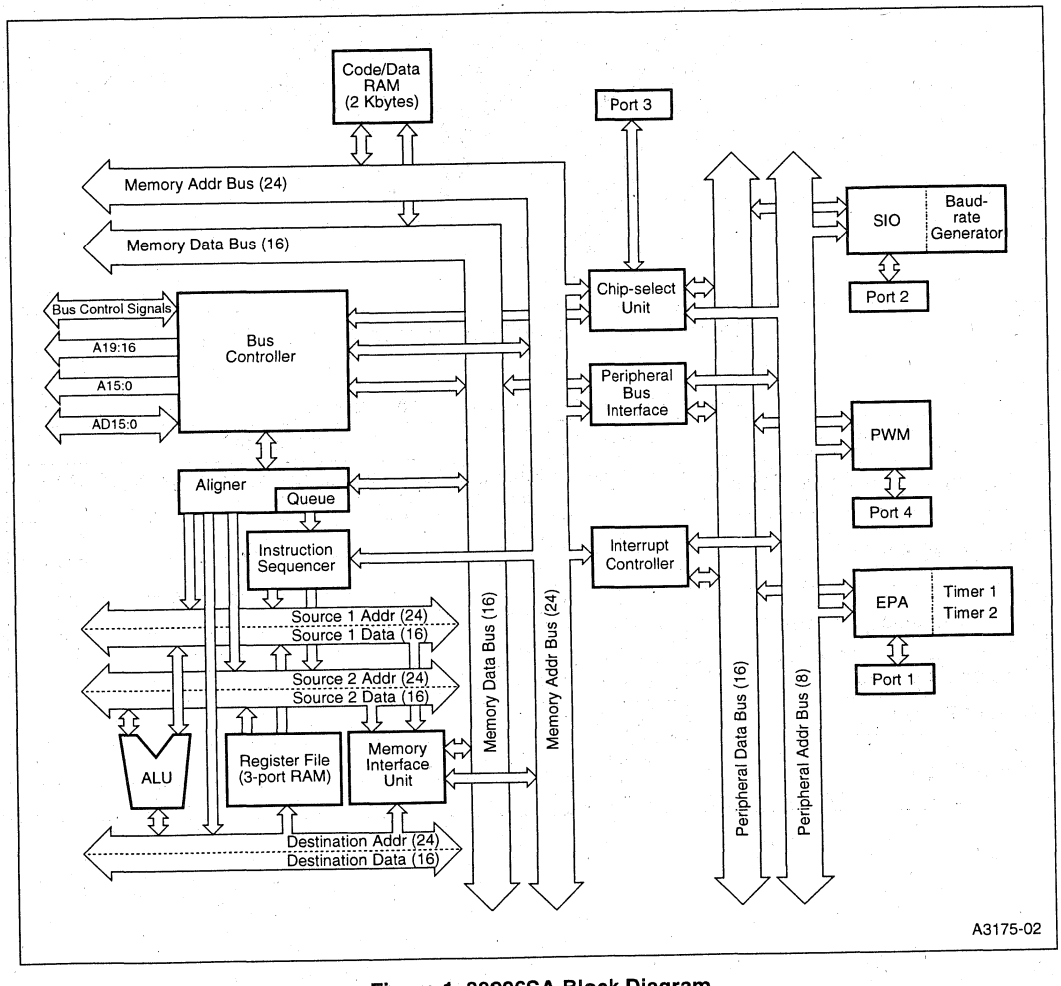


Figure 1. 80296SA Block Diagram

2.0 NOMENCLATURE OVERVIEW

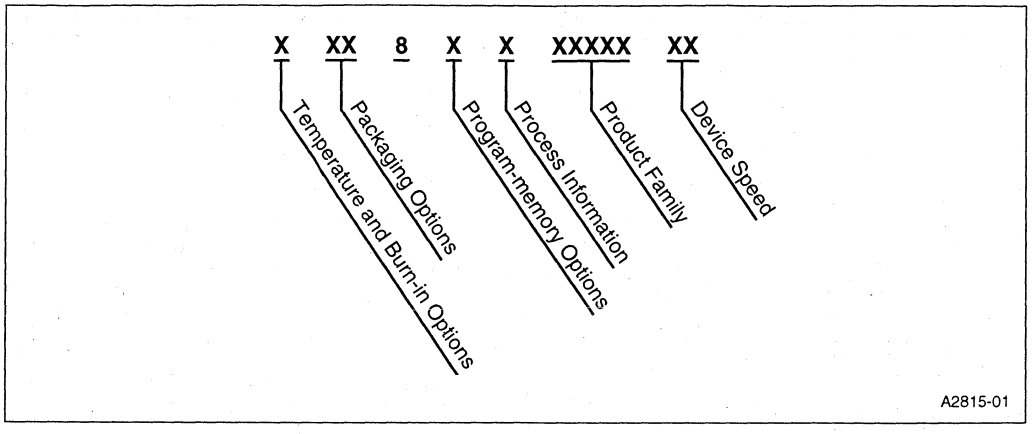


Figure 2. The 80296SA Family Nomenclature

Table 1. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	S	QFP
	SB	SQFP
Program–memory Options	0	Without ROM
	3	ROM
Process Information	no mark	CHMOS
Product Family	296SA	—
Device Speed	no mark	40 MHz
	50	50 MHz

3.0 PINOUT

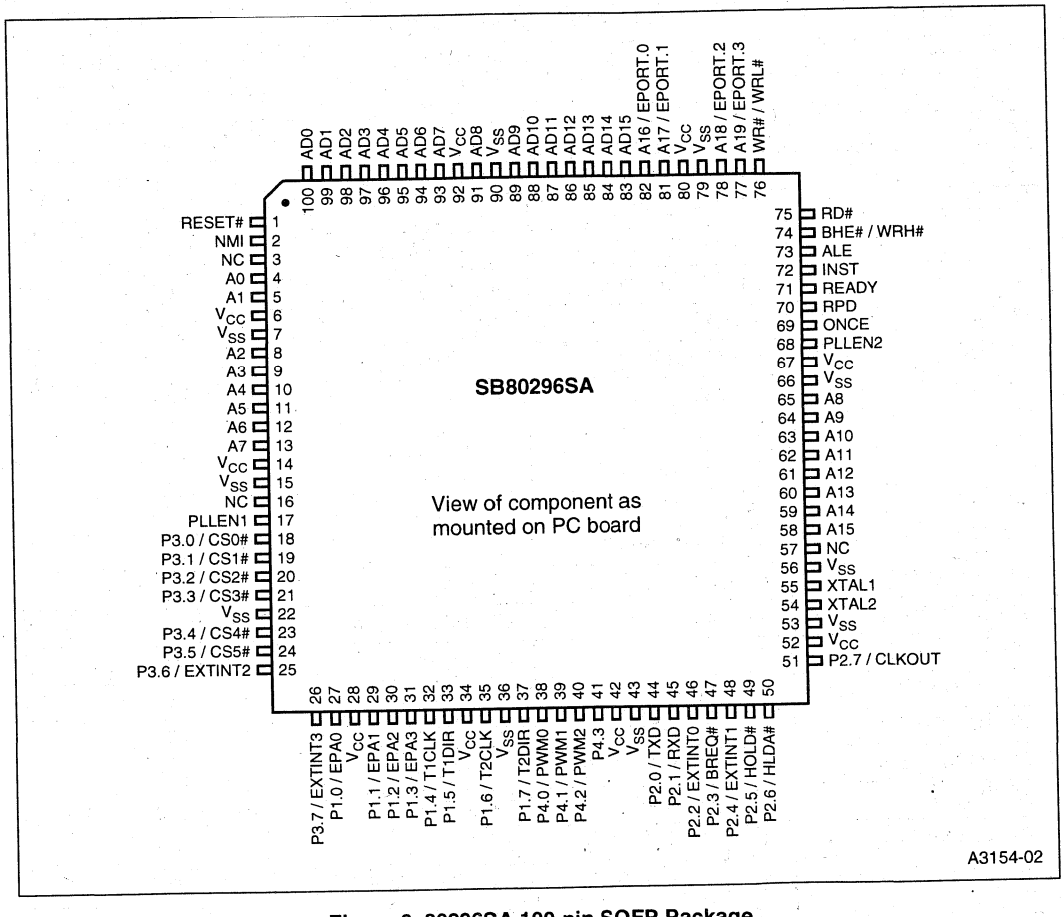


Figure 3. 80296SA 100-pin SQFP Package

Table 2. 80296SA 100-pin SQFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	RESET#	26	EXTINT3/P3.7	51	CLKOUT/P2.7	76	WR#/WRL#
2	NMI	27	EPA0/P1.0	52	V_{CC}	77	EPORT.3/A19
3	NC (see Note)	28	V_{CC}	53	V_{SS}	78	EPORT.2/A18
4	A0	29	EPA1/P1.1	54	XTAL2	79	V_{SS}
5	A1	30	EPA2/P1.2	55	XTAL1	80	V_{CC}
6	V_{CC}	31	EPA3/P1.3	56	V_{SS}	81	EPORT.1/A17
7	V_{SS}	32	T1CLK/P1.4	57	NC (see Note)	82	EPORT.0/A16
8	A2	33	T1DIR/P1.5	58	A15	83	AD15
9	A3	34	V_{CC}	59	A14	84	AD14
10	A4	35	T2CLK/P1.6	60	A13	85	AD13
11	A5	36	V_{SS}	61	A12	86	AD12
12	A6	37	T2DIR/P1.7	62	A11	87	AD11
13	A7	38	PWM0/P4.0	63	A10	88	AD10
14	V_{CC}	39	PWM1/P4.1	64	A9	89	AD9
15	V_{SS}	40	PWM2/P4.2	65	A8	90	V_{SS}
16	NC (see Note)	41	P4.3	66	V_{SS}	91	AD8
17	PLLEN1	42	V_{CC}	67	V_{CC}	92	V_{CC}
18	CS0#/P3.0	43	V_{SS}	68	PLLEN2	93	AD7
19	CS1#/P3.1	44	TXD/P2.0	69	ONCE	94	AD6
20	CS2#/P3.2	45	RXD/P2.1	70	RPD	95	AD5
21	CS3#/P3.3	46	EXTINT0/P2.2	71	READY	96	AD4
22	V_{SS}	47	BREQ#/P2.3	72	INST	97	AD3
23	CS4#/P3.4	48	EXTINT1/P2.4	73	ALE	98	AD2
24	CS5#/P3.5	49	HOLD#/P2.5	74	BHE#/WRH#	99	AD1
25	EXTINT2/P3.6	50	HLDA#/P2.6	75	RD#	100	AD0

NOTE: For compatibility with future products, tie pin 3 to V_{CC} and leave pins 16 and 57 unconnected.

Table 3. 80296SA 100-pin SQFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	Pin
A0	4
A1	5
A2	8
A3	9
A4	10
A5	11
A6	12
A7	13
A8	65
A9	64
A10	63
A11	62
A12	61
A13	60
A14	59
A15	58
A16	82
A17	81
A18	78
A19	77
AD0	100
AD1	99
AD2	98
AD3	97
AD4	96
AD5	95
AD6	94
AD7	93
AD8	91
AD9	89
AD10	88
AD11	87

Address & Data (continued)	
Name	Pin
AD12	86
AD13	85
AD14	84
AD15	83

Bus Control & Status	
Name	Pin
ALE	73
BHE#/WRH#	74
BREQ#	47
HOLD#	49
HLDA#	50
INST	72
RD#	75
READY	71
WR#/WRL#	76

Processor Control	
Name	Pin
CLKOUT	51
EXTINT0	46
EXTINT1	48
EXTINT2	25
EXTINT3	26
NMI	2
ONCE	69
RESET#	1
RPD	70
XTAL1	55
XTAL2	54
PLLEN1	17
PLLEN2	68

Input/Output	
Name	Pin
CS0#/P3.0	18
CS1#/P3.1	19
CS2#/P3.2	20
CS3#/P3.3	21
CS4#/P3.4	23
CS5#/P3.5	24
EPA0/P1.0	27
EPA1/P1.1	29
EPA2/P1.2	30
EPA3/P1.3	31
EPORT.0	82
EPORT.1	81
EPORT.2	78
EPORT.3	77
P2.2	46
P2.3	47
P2.4	48
P2.5	49
P2.6	50
P2.7	51
P3.6	25
P3.7	26
P4.3	41
PWM0/P4.0	38
PWM1/P4.1	39
PWM2/P4.2	40
RXD/P2.1	45
T1CLK/P1.4	32
T1DIR/P1.5	33
T2CLK/P1.6	35
T2DIR/P1.7	37
TXD/P2.0	44

Power & Ground	
Name	Pin
V_{CC}	6
V_{CC}	14
V_{CC}	28
V_{CC}	34
V_{CC}	42
V_{CC}	52
V_{CC}	67
V_{CC}	80
V_{CC}	92
V_{SS}	7
V_{SS}	15
V_{SS}	22
V_{SS}	36
V_{SS}	43
V_{SS}	53
V_{SS}	56
V_{SS}	66
V_{SS}	79
V_{SS}	90

No Connection	
Name	Pin
NC	3
NC	16
NC	57

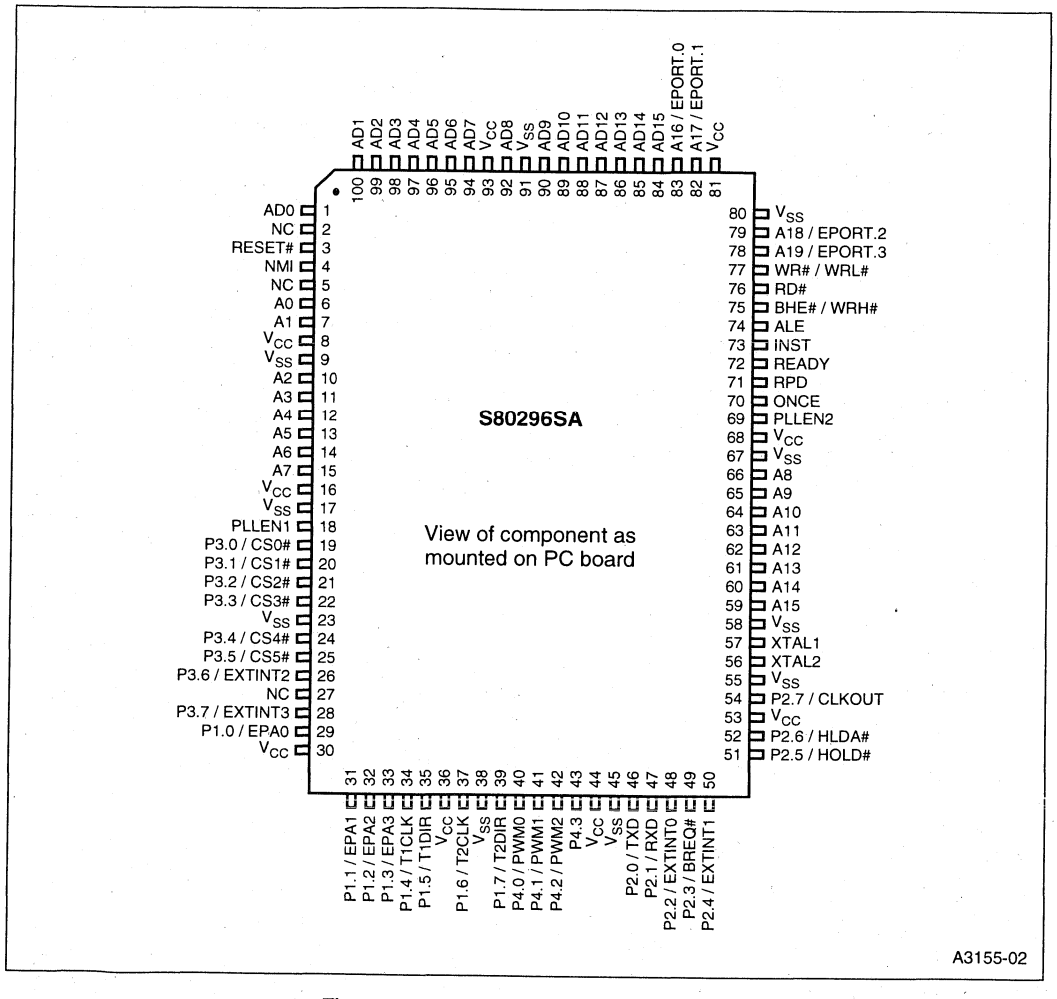


Figure 4. 80296SA 100-pin QFP Package

Table 4. 80296SA 100-pin QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AD0	26	EXTINT2/P3.6	51	HOLD#/P2.5	76	RD#
2	NC (see Note)	27	NC (see Note)	52	HLDA#/P2.6	77	WR#/WRL#
3	RESET#	28	EXTINT3/P3.7	53	V_{CC}	78	EPORT.3/A19
4	NMI	29	EPA0/P1.0	54	CLKOUT/P2.7	79	EPORT.2/A18
5	NC (see Note)	30	V_{CC}	55	V_{SS}	80	V_{SS}
6	A0	31	EPA1/P1.1	56	XTAL2	81	V_{CC}
7	A1	32	EPA2/P1.2	57	XTAL1	82	EPORT.1/A17
8	V_{CC}	33	EPA3/P1.3	58	V_{SS}	83	EPORT.0/A16
9	V_{SS}	34	T1CLK/P1.4	59	A15	84	AD15
10	A2	35	T1DIR/P1.5	60	A14	85	AD14
11	A3	36	V_{CC}	61	A13	86	AD13
12	A4	37	T2CLK/P1.6	62	A12	87	AD12
13	A5	38	V_{SS}	63	A11	88	AD11
14	A6	39	T2DIR/P1.7	64	A10	89	AD10
15	A7	40	PWM0/P4.0	65	A9	90	AD9
16	V_{CC}	41	PWM1/P4.1	66	A8	91	V_{SS}
17	V_{SS}	42	PWM2/P4.2	67	V_{SS}	92	AD8
18	PLLEN1	43	P4.3	68	V_{CC}	93	V_{CC}
19	CS0#/P3.0	44	V_{CC}	69	PLLEN2	94	AD7
20	CS1#/P3.1	45	V_{SS}	70	ONCE	95	AD6
21	CS2#/P3.2	46	TXD/P2.0	71	RPD	96	AD5
22	CS3#/P3.3	47	RXD/P2.1	72	READY	97	AD4
23	V_{SS}	48	EXTINT0/P2.2	73	INST	98	AD3
24	CS4#/P3.4	49	BREQ#/P2.3	74	ALE	99	AD2
25	CS5#/P3.5	50	EXTINT1/P2.4	75	BHE#/WRH#	100	AD1

NOTE: For compatibility with future products, tie pin 5 to V_{CC} and leave pins 2 and 27 unconnected.

Table 5. 80296SA 100-pin QFP Pin Assignment Arranged by Functional Categories

Address & Data	
Name	Pin
A0	6
A1	7
A2	10
A3	11
A4	12
A5	13
A6	14
A7	15
A8	66
A9	65
A10	64
A11	63
A12	62
A13	61
A14	60
A15	59
A16	83
A17	82
A18	79
A19	78
AD0	1
AD1	100
AD2	99
AD3	98
AD4	97
AD5	96
AD6	95
AD7	94
AD8	92
AD9	90
AD10	89
AD11	88

Address & Data (continued)	
Name	Pin
AD12	87
AD13	86
AD14	85
AD15	84
Bus Control & Status	
Name	Pin
ALE	74
BHE#/WRH#	75
BREQ#	49
HOLD#	51
HLDA#	52
INST	73
RD#	76
READY	72
WR#/WRL#	77

Processor Control	
Name	Pin
CLKOUT	54
EXTINT0	48
EXTINT1	50
EXTINT2	26
EXTINT3	28
NMI	4
ONCE	70
RESET#	3
RPD	71
XTAL1	57
XTAL2	56
PLLEN1	18
PLLEN2	69

Input/Output	
Name	Pin
CS0#/P3.0	19
CS1#/P3.1	20
CS2#/P3.2	21
CS3#/P3.3	22
CS4#/P3.4	24
CS5#/P3.5	25
EPA0/P1.0	29
EPA1/P1.1	31
EPA2/P1.2	32
EPA3/P1.3	33
EPORT.0	83
EPORT.1	82
EPORT.2	79
EPORT.3	78
P2.2	48
P2.3	49
P2.4	50
P2.5	51
P2.6	52
P2.7	54
P3.6	26
P3.7	28
P4.3	43
PWM0/P4.0	40
PWM1/P4.1	41
PWM2/P4.2	42
RXD/P2.1	47
T1CLK/P1.4	34
T1DIR/P1.5	35
T2CLK/P1.6	37
T2DIR/P1.7	39
TXD/P2.0	46

Power & Ground	
Name	Pin
V_{CC}	8
V_{CC}	16
V_{CC}	30
V_{CC}	36
V_{CC}	44
V_{CC}	53
V_{CC}	68
V_{CC}	81
V_{CC}	93
V_{SS}	9
V_{SS}	17
V_{SS}	23
V_{SS}	38
V_{SS}	45
V_{SS}	55
V_{SS}	58
V_{SS}	67
V_{SS}	80
V_{SS}	91

No Connection	
Name	Pin
NC	2
NC	5
NC	27

4.0 SIGNALS

Table 6. Signal Descriptions

Name	Type	Description
A15:0	I/O	System Address Bus These address lines provide address bits 0–15 during the entire external memory cycle during both multiplexed and demultiplexed bus modes.
A19:16	I/O	Address Lines 16–19 These address lines provide address bits 16–19 during the entire external memory cycle, supporting extended addressing of the 1 Mbyte address space. **NOTE:** Internally, there are 24 address bits; however, only 20 external address pins (A19:0) are implemented. The internal address space is 16 Mbytes (000000–FFFFFFH) and the external address space is 1 Mbyte (00000–FFFFFH). The device resets to FF2080H in internal memory or F2080H in external memory. A19:16 share package pins with EPORT.3:0.
AD15:0	I/O	Address/Data Lines The functions of these pins depend on the bus size and mode. When a bus access is not occurring, these pins revert to their I/O port function. **16-bit Multiplexed Bus Mode**: AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **8-bit Multiplexed Bus Mode**: AD15:8 drive address bits 8–15 during the entire bus cycle. AD7:0 drive address bits 0–7 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle. **16-bit Demultiplexed Mode**: AD15:0 drive or receive data during the entire bus cycle. **8-bit Demultiplexed Mode**: AD7:0 drive or receive data during the entire bus cycle. AD15:8 drive the data that is currently on the high byte of the internal bus.
ALE	O	Address Latch Enable This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A19:16 and AD15:0 for a multiplexed bus; A19:0 for a demultiplexed bus). ALE differs from ADV# in that it does not remain active during the entire bus cycle. An external latch can use this signal to demultiplex the address bits 0–15 from the address/data bus in multiplexed mode.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
BHE#	O	Byte High Enable† During 16-bit bus cycles, this active-low output signal is asserted for word reads and writes and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus. Use BHE#, in conjunction with A0, to determine which memory byte is being transferred over the system bus: **BHE# A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only BHE# shares a package pin with WRH#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
BREQ#	O	Bus Request This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle. When the bus-hold protocol is enabled (WSR.7 is set), the P2.3/BREQ# pin can function only as BREQ#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). The microcontroller can assert BREQ# at the same time as or after it asserts HLDA#. Once it is asserted, BREQ# remains asserted until HOLD# is deasserted. BREQ# shares a package pin with P2.4.
CLKOUT	O	Clock Output Output of the internal clock generator. The CLKOUT frequency is ½ the internal operating frequency (f). CLKOUT has a 50% duty cycle. CLKOUT shares a package pin with P2.7.
CS5#:0	O	Chip-select Lines 0–5 The active-low output CS*x*# is asserted during an external memory cycle when the address to be accessed is in the range programmed for chip select *x*. If the external memory address is outside the range assigned to the six chip selects, no chip-select output is asserted and the bus configuration defaults to the CS5# values. Immediately following reset, CS0# is automatically assigned to the range FF2000–FF20FFH (F2000–F20FFH if external). CS5:0# shares a package pin with P3.5:0.
EPA3:0	I/O	Event Processor Array (EPA) Input/Output pins These are the high-speed input/output pins for the EPA capture/compare channels. For high-speed PWM applications, the outputs of two EPA channels (either EPA0 and EPA1 or EPA2 and EPA3) can be remapped to produce a PWM waveform on a shared output pin. EPA3:0 share package pins with P1.3:0.
EPORT.3:0	I/O	Extended Addressing Port This is a standard, 4-bit, bidirectional I/O port. EPORT.3:0 share package pins with A19:16.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
EXTINT3:0	I	External Interrupts In normal operating mode, a rising edge on EXTINT*x* sets the EXTINT*x* interrupt pending bit. EXTINT*x* is sampled during phase 2 (CLKOUT high). The minimum high time is one state time. In standby and powerdown modes, asserting the EXTINT*x* signal for at least 50 ns causes the device to resume normal operation. The interrupt need not be enabled, but the pin must be configured as a special-function input. If the EXTINT*x* interrupt is enabled, the CPU executes the interrupt service routine. Otherwise, the CPU executes the instruction that immediately follows the command that invoked the power-saving mode. In idle mode, asserting any enabled interrupt causes the device to resume normal operation. These signals share package pins as follows: EXTINT0 with P2.2, EXTINT1 iwith P2.4, EXTINT2 with P3.6, and EXTINT3 with P3.7.
HLDA#	O	Bus Hold Acknowledge This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD#. When the bus-hold protocol is enabled (WSR.7 is set), the P2.6/HLDA# pin can function only as HLDA#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared).
HOLD#	I	Bus Hold Request An external device uses this active-low input signal to request control of the bus. When the bus-hold protocol is enabled (WSR.7 is set), the P2.5/HOLD# pin can function only as HOLD#, regardless of the configuration selected through the port configuration registers (P2_MODE, P2_DIR, and P2_REG). An attempt to change the pin configuration is ignored until the bus-hold protocol is disabled (WSR.7 is cleared). HOLD# shares a package pin with P2.5.
INST	O	Instruction Fetch This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.
NMI	I	Nonmaskable Interrupt In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts. Assert NMI for greater than one state time to guarantee that it is recognized.
ONCE	I	On-circuit Emulation Holding ONCE high during the rising edge of RESET# places the device into on-circuit emulation (ONCE) mode. This mode puts all pins except READY, RESET#, ONCE, and NMI into a high-impedance state, thereby isolating the device from other components in the system. The value of ONCE is latched when the RESET# pin goes inactive. While the device is in ONCE mode, you can debug the system using a clip-on emulator. To exit ONCE mode, reset the device by pulling the RESET# signal low. To prevent accidental entry ihto ONCE mode, connect the ONCE pin to V_{SS}.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
P1.7:0	I/O	Port 1 Port 1 is a standard bidirectional port that is multiplexed with individually selectable special-function signals. These signals share package pins as follows: P1.0 with EPA0, P1.1 with EPA1, P1.2 with EPA2, P1.3 with EPA3, P1.4 with T1CLK, P1.5 with T1DIR, P1.6 with T2CLK, and P1.7 with T2DIR.
P2.7:0	I/O	Port 2 Port 2 is a standard bidirectional port that is multiplexed with individually selectable special-function signals. These signals share package pins as follows: P2.0 with TXD, P2.1 with RXD, P2.2 with EXTINT0, P2.3 with BREQ#, P2.4 with EXTINT1, P2.5 with HOLD#, P2.6 with HLDA#, and P2.7 with CLKOUT.
P3.7:0	I/O	Port 3 Port 3 is an 8-bit, bidirectional, standard I/O port. These signals share package pins as follows: P3.0 with CS0#, P3.1 with CS1#, P3.2 with CS2#, P3.3 with CS3#, P3.4 with CS4#, P3.5 with CS5#, P3.6 with EXTINT2, and P3.7 with EXTINT3.
P4.3:0	I/O	Port 4 Port 4 is a 4-bit, bidirectional, standard I/O port with high-current drive capability. These signals share package pins as follows: P4.0 with PWM0, P4.1 with PWM1, and P4.2 with PWM2. P4.3 does not share a package pin with another signal.
PLLEN2:1	I	Phase-locked Loop 1 and 2 Enable These input pins are used to enable the phase-locked loop and select either the doubled or quadrupled clock speed as follows: **PLLEN2** **PLLEN1** **Mode** 0 0 PLL disabled ($f = F_{XTAL1}$) 0 1 PLL in 2x mode ($f = 2F_{XTAL1}$) 1 0 Reserved† 1 1 PLL in 4x mode ($f = 4F_{XTAL1}$) † **CAUTION:** This reserved combination causes the device to enter an unsupported test mode.
PWM2:0	O	Pulse Width Modulator Outputs These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable. PWM2:0 share package pins with P4.2:0.
RD#	O	Read Read-signal output to external memory. RD# is asserted only during external memory reads.
READY	I	Ready Input This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states in addition to the wait states that are generated internally. When READY is high, CPU operation continues in a normal manner with wait states inserted as programmed in the chip configuration registers or the chip-select *x* bus control register. READY is ignored for all internal memory accesses.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
RESET#	I/O	Reset A level-sensitive reset input to, and an open-drain system reset output from, the microcontroller. Either a falling edge on RESET# or an internal reset turns on a pull-down transistor connected to the RESET# pin for 16 state times. In the powerdown, standby, and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. If the phase-locked loop (PLL) clock circuitry is enabled, you must hold RESET# low for at least 2 ms to allow the PLL to stabilize before the internal CPU and peripheral clocks are enabled. After a device reset, the first instruction fetch is from F2080H.
RPD	I	Return from Powerdown Timing pin for the return-from-powerdown circuit. If your application uses an external interrupt input to return to normal operation from powerdown mode, and the phase-locked loop (PLL) circuitry is enabled (see PLLEN2:1 signal description), connect a capacitor between RPD and V_{SS}. The capacitor is used to establish a delay of at least 2 ms to allow the PLL circuitry to stabilize before the internal CPU and peripheral clocks are enabled.(See "Exiting Powerdown Mode" on page 12-8 of the *80296SA Microcontroller User's Manual* for details on selecting the capacitor.) If your application uses powerdown mode, but the phase-locked loop (PLL) circuitry is disabled, the capacitor is not required. If your application does not use powerdown mode, leave this pin unconnected.
RXD	I/O	Receive Serial Data In modes 1, 2, and 3, RXD receives serial port input data. In mode 0, it functions as either an input or an open-drain output for data. RXD shares a package pin with P2.1.
T1CLK	I	Timer 1 External Clock External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode. **and** External clock for the serial I/O baud-rate generator input (program selectable). T1CLK shares a package pin with P1.4.
T2CLK	I	Timer 2 External Clock External clock for timer 2. Timer 2 increments (or decrements) on both rising and falling edges of T2CLK. Also used in conjunction with T2DIR for quadrature counting mode. T2CLK shares a package pin with P1.6.
T1DIR	I	Timer 1 External Direction External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode. T1DIR shares a package pin with P1.5.
T2DIR	I	Timer 2 External Direction External direction (up/down) for timer 2. Timer 2 increments when T2DIR is high and decrements when it is low. Also used in conjunction with T2CLK for quadrature counting mode. T2DIR shares a package pin with P1.7.

Table 6. Signal Descriptions (Continued)

Name	Type	Description
TXD	O	Transmit Serial Data In serial I/O modes 1, 2, and 3, TXD transmits serial port output data. In mode 0, it is the serial clock output. TXD shares a package pin with P2.0.
V_{CC}	PWR	Digital Supply Voltage Connect each V_{CC} pin to the digital supply voltage.
V_{SS}	GND	Digital Circuit Ground Connect each V_{SS} pin to ground through the lowest possible impedance path.
WR#	O	Write† This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes. WR# shares a package pin with WRL#. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
WRH#	O	Write High† During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations. WRH# shares a package pin with BHE#. † The chip configuration register 0 (CCR0) determines whether this pin functions as BHE# or WRH#. CCR0.2 = 1 selects BHE#; CCR0.2 = 0 selects WRH#.
WRL#	O	Write Low† During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations. WRL# shares a package pin with WR#. † The chip configuration register 0 (CCR0) determines whether this pin functions as WR# or WRL#. CCR0.2 = 1 selects WR#; CCR0.2 = 0 selects WRL#.
XTAL1	I	Input Crystal/Resonator or External Clock Input Input to the on-chip oscillator, phase-locked loop circuitry, and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1. The external clock signal must meet the V_{IH} specification for XTAL1.
XTAL2	O	Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses a external clock source instead of the on-chip oscillator.

5.0 ADDRESS MAP

Table 7. 80296SA Address Map

Hex Address	Description (Note 1, Note 2)	Addressing Modes for Data Accesses
FFFFFF FFF800	External device (memory or I/O) in 1-Mbyte mode (CCB1.1=0) A copy of internal code RAM in 64-Kbyte mode (CCB1.1=1)	Extended
FFF7FF FF2080	External program memory (Note 3)	Extended
FF207F FF2000	External special-purpose memory (CCBs and interrupt vectors)	Extended
FF1FFF FF0400	External device (memory or I/O) connected to address/data bus	Extended
FF03FF FF0000	Reserved for in-circuit emulators	—
FEFFFF 0F0000	Overlaid memory (reserved for future devices); locations *x*F0000–*x*F03FFH are reserved for in-circuit emulators	—
0EFFFF 010000	External device (memory or I/O) connected to address/data bus	Extended
00FFFF 00F800	Internal code RAM (code or data); can be windowed by WSR1. In 64-Kbyte mode, code RAM is identically mapped into page FFH.	Indirect, indexed, extended, windowed direct
00F7FF 00F000	External device (memory or I/O) connected to address/data bus; can be windowed by WSR1	Indirect, indexed, extended, windowed direct
00EFFF 002000	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
001FFF 001F00	Internal peripheral special-function registers (SFRs); can be windowed by WSR or WSR1	Indirect, indexed, extended, windowed direct
001EFF 001C00	Reserved (future SFR expansion)	—
001BFF 000400	External device (memory or I/O) connected to address/data bus	Indirect, indexed, extended
0003FF 000200	Reserved (future register file expansion)	—
0001FF 000100	Upper register file (general-purpose register RAM) can be windowed by WSR or WSR1	Indirect, indexed, extended windowed direct
0000FF 00001A	Lower register file (general-purpose register RAM)	Direct, indirect, indexed, extended
000019 000000	Lower register file (stack pointer and CPU SFRs)	Direct

NOTES:
1. Unless otherwise noted, write 0FFH to reserved memory locations and write 0 to reserved SFR bits.
2. The contents or functions of reserved locations may change in future device revisions, in which case a program that relies on one or more of these locations might not function properly.
3. External memory occupies the boot memory partition, FF2080–FF7FFH. After reset, the default chip-select line (CS0#) is active; the first instruction fetch is from FF2080H.

6.0 ELECTRICAL CHARACTERISTICS

NOTICE: This datasheet contains information on products being sampled or in the initial production phase of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature	−60°C to +150°C
Supply Voltage with Respect to V_{SS}	−0.5 V to +7.0 V
Power Dissipation	1.5 W

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias)	0°C to +70°C
V_{CC} (Digital Supply Voltage)	4.5 V to 5.5 V
F_{XTAL1} (Input frequency for V_{CC} = 4.5 V – 5.5 V) (Note 1, 2, 3)	16 MHz to 50 MHz

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. This device is static and should operate below 1 Hz, but has been tested only down to 16 MHz.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. Assumes an external clock. The maximum frequency for an external crystal oscillator is 25 MHz.

6.1 DC Characteristics

Table 8. DC Characteristics Over Specified Operating Conditions

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current		90	150	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V Device in Reset
I_{IDLE}	Idle Mode Current		45	60	mA	XTAL1 = 50 MHz V_{CC} = 5.5 V
I_{PD}	Powerdown Mode Current		20	50	µA	V_{CC} = 5.5 V (Note 2)
I_{STDBY}	Standby Mode		8	15	mA	V_{CC} = 5.5 V
I_{LI}	Input Leakage Current (Standard Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage (all pins)	–0.5		0.8	V	
V_{IL1}	Input Low Voltage XTAL1	–0.5		0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.2 V_{CC} +1		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (output configured as complementary) (Note 3, 4)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OL1}	Output Low Voltage on P4.3:0 (output configured as complementary) (Note 4)			0.45 0.6	V V	I_{OL} = 8 mA I_{OL} = 15 mA
V_{OL2}	Output Low Voltage in Reset on ALE, INST, and NMI			0.45	V	I_{OL} = 3 µA
V_{OL3}	Output Low Voltage in Reset on ONCE pin			0.45	V	I_{OL} = 30 µA

NOTES:

1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

5. For all pins that were weakly pulled high during reset. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
6. Pin capacitance is not tested. This value is based on design simulations.

Table 8. DC Characteristics Over Specified Operating Conditions (Continued)

Symbol	Parameter	Min	Typical (Note 1)	Max	Units	Test Conditions
V_{OL4}	Output Low Voltage on XTAL2			0.3 0.45 1.5	V V V	I_{OL} = 100 µA I_{OL} = 700 µA I_{OL} = 3 mA
V_{OH}	Output High Voltage (output configured as complementary) (Note 4)	V_{CC} – 0.5 V_{CC} – 0.9 V_{CC} – 1.5			V V V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
V_{OH1}	Output High Voltage in Reset (Note 5)	V_{CC} – 0.7			V	I_{OH} = –3 µA
V_{OH2}	Output High Voltage on XTAL2	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = –100 µA I_{OH} = –700 µA I_{OH} = –3 mA
V_{OH3}	Output High Voltage on READY in Reset	V_{CC} –1.1			V	
$V_{TH+} - V_{TH-}$	Hysteresis voltage width on RESET# pin		0.3		V	
C_S	Pin Capacitance (any pin to V_{SS}) (Note 6)			10	pF	
R_{RST}	Reset Pull-up Resistor	50		150	kΩ	V_{CC} = 5.5 V, V_{IN} = 4.0 V

NOTES:

1. Typical values are based on a limited number of samples and are not guaranteed. The values listed are at room temperature with V_{CC} = 5.0 V.
2. For temperatures below 100°C, typical is 10 µA.
3. For all pins except P4.3:0, which have higher drive capability (see V_{OL1}).
4. During normal (non-transient) conditions, the following maximum current limits apply for pin groups and individual pins:

Group	I_{OL} (mA)	I_{OH} (mA)	Individual	I_{OL} (mA)	I_{OH} (mA)
P1.7:3, P4	40	40	P1, P2, P3	10	10
P2	40	40	P4	18	10
P1.2:0, P3	40	40			

5. For all pins that were weakly pulled high during reset. This **excludes** ALE, INST, and NMI, which were weakly pulled low (see V_{OL2}) and ONCE, which was pulled medium low (see V_{OL3}).
6. Pin capacitance is not tested. This value is based on design simulations.

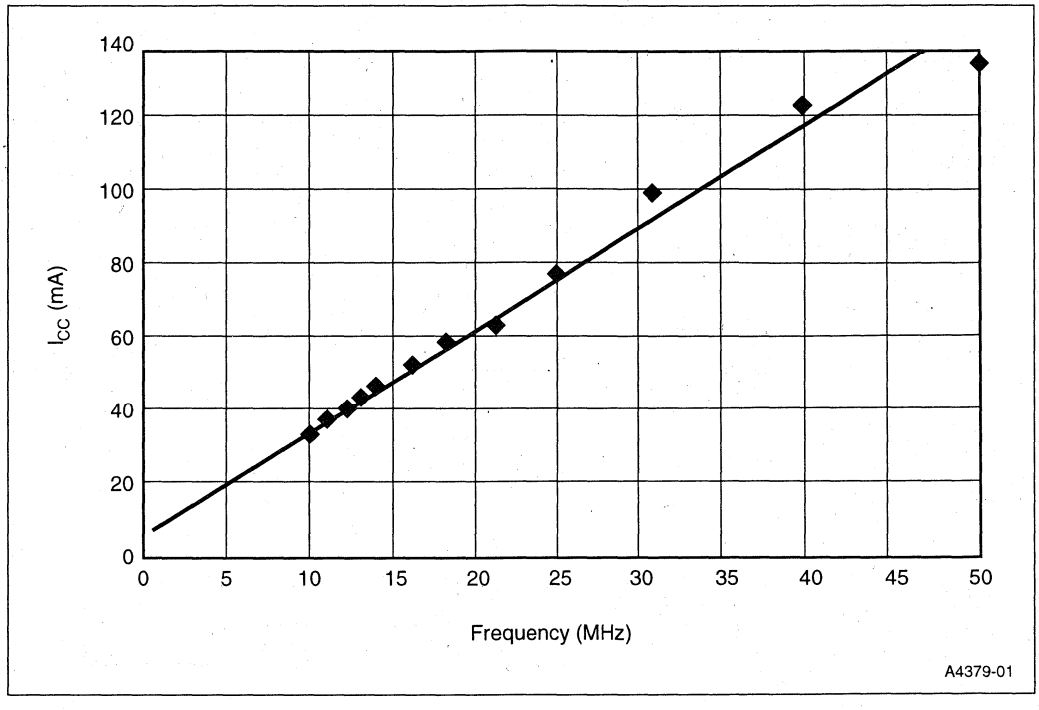


Figure 5. I_{CC} versus Frequency in Reset

6.2 AC Characteristics

6.2.1 RELATIONSHIP OF XTAL1 TO CLKOUT

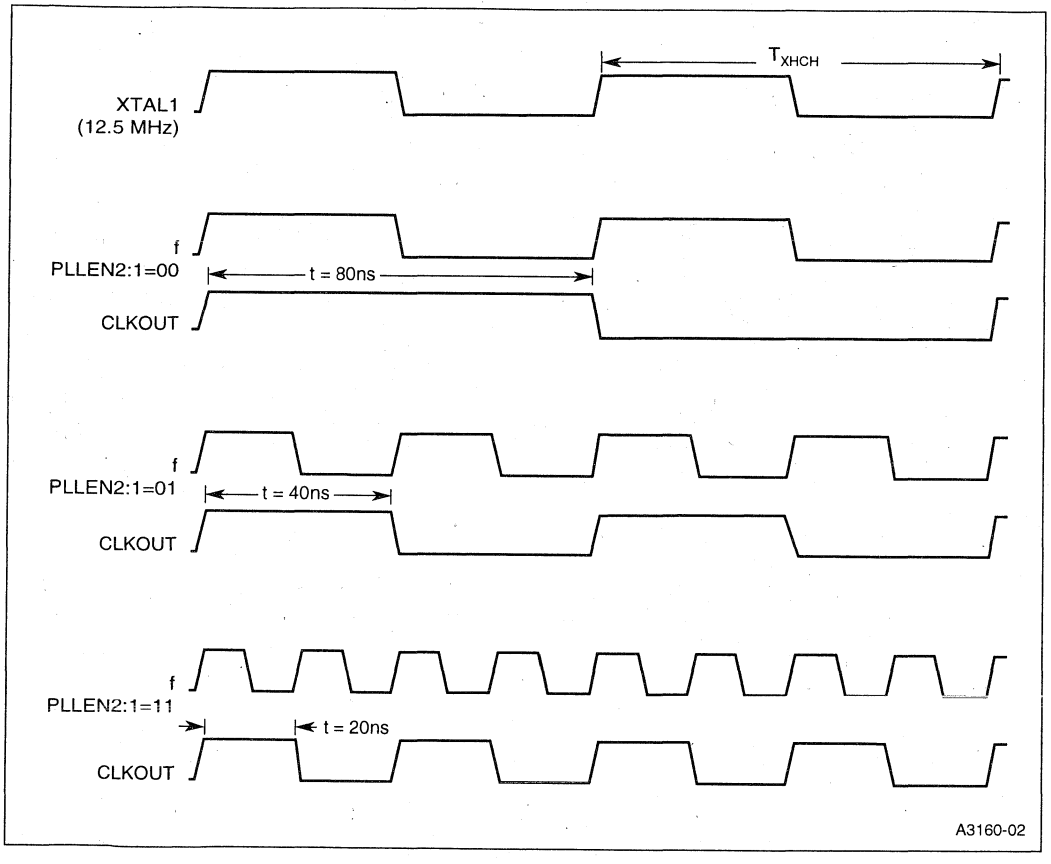


Figure 6. Effect of Clock Mode on CLKOUT

6.2.2 EXPLANATION OF AC SYMBOLS

Each AC timing symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Table 9. AC Timing Symbol Definitions

Character	Signal(s)
A	AD15:0, A19:0
B	BHE#
BR	BREQ#
C	CLKOUT
D	AD15:0, AD7:0, RXD (SIO mode 0 input data)
H	HOLD#
HA	HLDA#
L	ALE
Q	AD15:0, AD7:0, RXD (SIO mode 0 output data)
R	RD#
S	CS*x*#
W	WR#, WRH#,WRL#
X	XTAL1, TXD (SIO clock)
Y	READY

Character	Condition
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating (low impedance)

6.2.3 AC CHARACTERISTICS — MULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 10. AC Characteristics the 80C296SA Will Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{XHCH}	XTAL1 Rising Edge to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{AVWL}	Address Valid to WR# Falling Edge	2t – 25		ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	–13	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	–15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (1)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{AVLL}	Address Valid to ALE Falling Edge	t – 15		ns
T_{LLAX}	Address Hold after ALE Falling Edge	1		ns
T_{LLRL}	ALE Falling Edge to RD# Falling Edge	3		ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	–10	20	ns
T_{RLRH}	RD# Low Period	2t – 25		ns (3)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 5	t + 15	ns (4)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE Falling Edge to WR# Falling Edge	4		ns
T_{QVWH}	Data Stable to WR# Rising Edge	2t – 27		ns (1)
T_{CHWH}	CLKOUT High to WR# Rising Edge	–15	5	ns
T_{WLWH}	WR# Low Period	2t – 25		ns (1)

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 10. AC Characteristics the 80C296SA Will Meet, Multiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WHQX}	Data Hold after WR# Rising Edge	t – 7		ns
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 15	t + 20	ns
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge	0		ns
T_{WHAX}	AD15:8 Hold after WR# Rising Edge	t – 4		ns (5)
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge	0		ns
T_{RHAX}	AD15:8 Hold after RD# Rising Edge	t – 4		ns (5)
T_{WHSH}	A19:16, CS# Hold after WR# Rising Edge	0		ns
T_{RHSH}	A19:16, CS# Hold after RD# Rising Edge	0		ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.

Table 11. AC Characteristics the External Memory System Must Meet, Multiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	AD15:0 Valid to Input Data Valid		3t – 32	ns (1)
T_{RLDV}	RD# Active to Input Data Valid		2t – 40	ns (1)
T_{SLDV}	Chip Select Low to Data Valid		4t – 28	ns (1)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t – 3	ns
T_{RXDX}	Data Hold after RD# Inactive	2		ns
T_{AVYV}	AD15:0 Valid to READY Setup		2t – 42	ns (2,4)
T_{CHYX}	Non-first READY Hold after CLKOUT High	0	2t – 40	ns (3,4,5)
T_{CHYX}	First READY Hold after CLKOUT High	t – 4	2t – 21	ns (3,4,5)
T_{YLYH}	Non-READY Time	No Upper Limit		ns

NOTES:
1. If wait states are used, add $2t \times n$, where n = number of wait states.
2. When forcing wait states using the BUSCON register, add $2t \times n$.
3. Exceeding the maximum specification causes additional wait states.
4. The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
5. If READY is held high after the first CLKOUT high following READY setup, or if more than one wait state is inserted, the hold time specification increases.

6.2.3.1 System Bus Timings, Multiplexed Bus

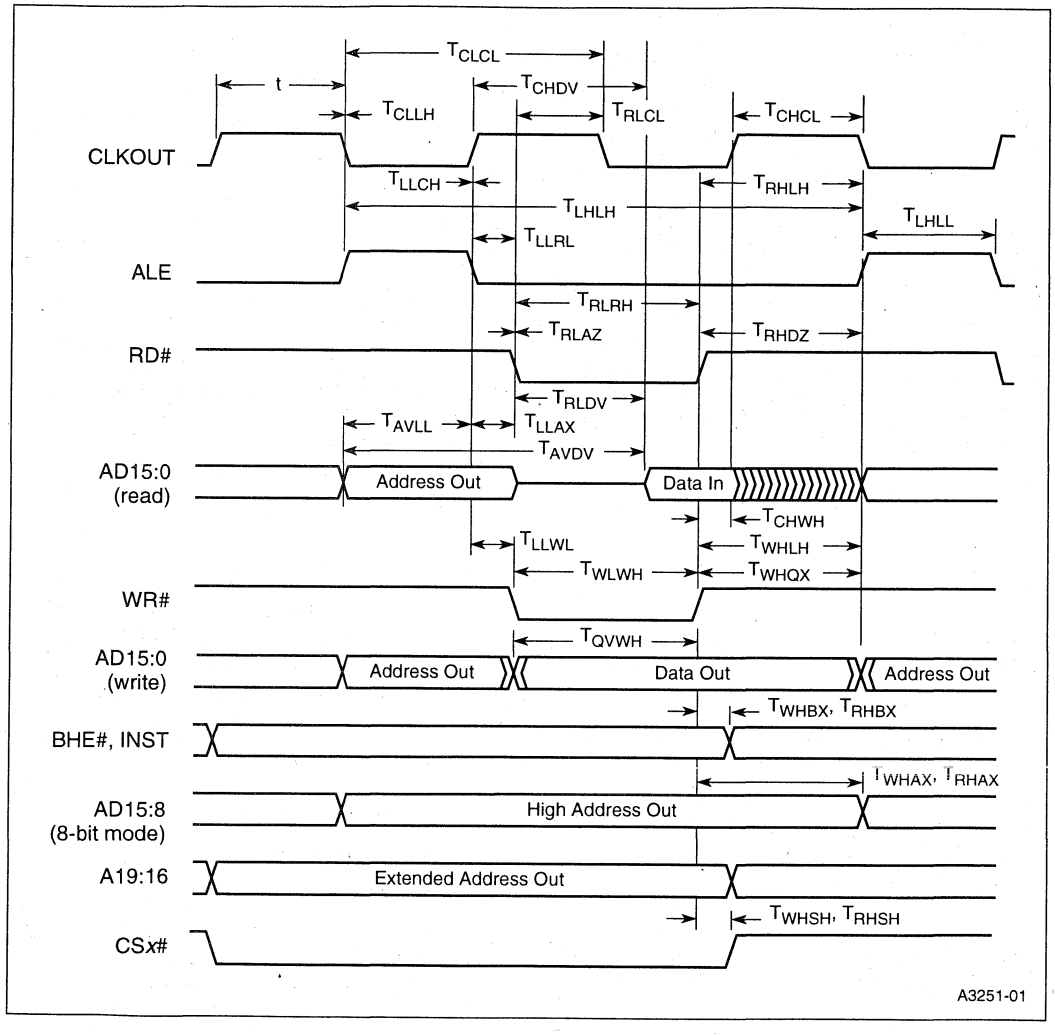


Figure 7. System Bus Timings, Multiplexed Bus Mode

6.2.3.2 READY Timing, Multiplexed Bus

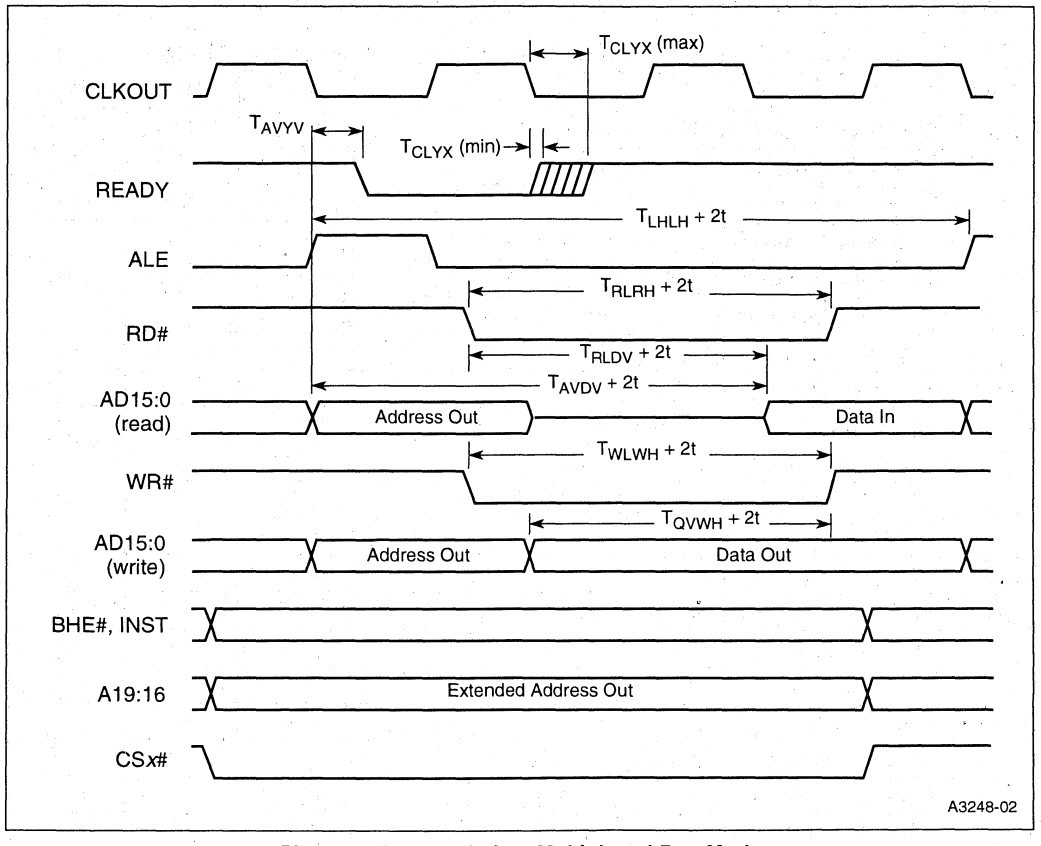


Figure 8. READY Timing, Multiplexed Bus Mode

6.2.4 AC CHARACTERISTICS — DEMULTIPLEXED BUS MODE

Test Conditions: Capacitive load on all pins = 50 pF, Rise and Fall Times = 3 ns.

Table 12. AC Characteristics the 80C296SA Will Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	Frequency on XTAL1, PLL in 1x mode	16	50 (1)	MHz
	Frequency on XTAL1, PLL in 2x mode	8 (2)	25	MHz
	Frequency on XTAL1, PLL in 4x mode	8 (2)	12.5	MHz
f	Operating frequency, f = F_{XTAL1}; PLL in 1x mode	16	50	MHz
	Operating frequency, f = $2F_{XTAL1}$; PLL in 2x mode			
	Operating frequency, f = $4F_{XTAL1}$; PLL in 4x mode			
t	Period, t = 1/f	20	62.5	ns
T_{AVWL}	Address Valid to WR# Falling Edge	t – 10		ns
T_{AVRL}	Address Valid to RD# Falling Edge	t – 10		ns
T_{RHRL}	Read High to Next Read Low	t – 5		ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	3	50	ns
T_{CLCL}	CLKOUT Cycle Time	2t		ns
T_{CHCL}	CLKOUT High Period	t – 10	t + 15	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising Edge	–13	10	ns
T_{LLCH}	ALE Falling Edge to CLKOUT Rising Edge	–15	15	ns
T_{LHLH}	ALE Cycle Time	4t		ns (3,4)
T_{LHLL}	ALE High Period	t – 10	t + 10	ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	–5	11	ns
T_{RLRH}	RD# Low Period	3t – 18		ns (3)
T_{RHLH}	RD# Rising Edge to ALE Rising Edge	t – 4	t + 15	ns (4)
T_{WLCL}	WR# Low to CLKOUT Falling Edge	–8	9	ns
T_{QVWH}	Data Stable to WR# Rising Edge	3t – 10		ns (4)
T_{CHWH}	CLKOUT High to WR# Rising Edge	–11	10	ns
T_{WLWH}	WR# Low Period	3t – 10		ns (3)
T_{WHQX}	Data Hold after WR# Rising Edge	t – 5	t + 20	ns
T_{WHLH}	WR# Rising Edge to ALE Rising Edge	t – 5	t + 10	ns (3)

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.

Table 12. AC Characteristics the 80C296SA Will Meet, Demultiplexed Bus Mode (Continued)

Symbol	Parameter	Min	Max	Units
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge	0		ns
T_{WHAX}	A19:0, CS*x*# Hold after WR# Rising Edge	0		ns
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge	0		ns
T_{RHAX}	A19:0, CS*x*# Hold after RD# Rising Edge	0		ns

NOTES:
1. 25 MHz is the maximum input frequency when using an external crystal oscillator; however, 50 MHz can be applied with an external clock source.
2. When the phase-locked loop (PLL) circuitry is enabled, the minimum input frequency on XTAL1 is 8 MHz. The PLL cannot be run at frequencies lower than 16 MHz.
3. If wait states are used, add $2t \times n$, where n = number of wait states.
4. Assuming back-to-back bus cycles.

Table 13. AC Characteristics the External Memory System Must Meet, Demultiplexed Bus Mode

Symbol	Parameter	Min	Max	Units
T_{AVDV}	A19:0 Valid to Input Data Valid		4t – 28	ns (1)
T_{RLDV}	RD# Active to Input Data Valid		3t – 25	ns (1)
T_{SLDV}	Chip Select Low to Data Valid		4t – 28	ns (1)
T_{CHDV}	CLKOUT High to Input Data Valid		2t – 25	ns
T_{RHDZ}	End of RD# to Input Data Float		t	ns
T_{RXDX}	Data Hold after RD# Inactive	2		ns
T_{AVYV}	A19:0 Valid to READY Setup		3t – 45	ns (2)
T_{CHYX}	Non-first READY Hold after CLKOUT High	0	2t – 40	ns (3,4,5)
T_{CHYX}	First READY Hold after CLKOUT High	t – 4	2t – 21	ns (3,4,5)
T_{YLYH}	Non READY Time	No Upper Limit		ns

NOTES:
1. If wait states are used, add $2t \times n$, where n = number of wait states.
2. When forcing wait states using the BUSCON register, add $2t \times n$.
3. Exceeding the maximum specification causes additional wait states.
4. The first falling edge of READY is not synchronized to a CLKOUT edge; therefore, one programmed wait state is required.
5. If READY is held high after the first CLKOUT high following READY setup, or if more than one wait state is inserted, the hold time specification increases.

6.2.4.1 System Bus Timings, Demultiplexed Bus

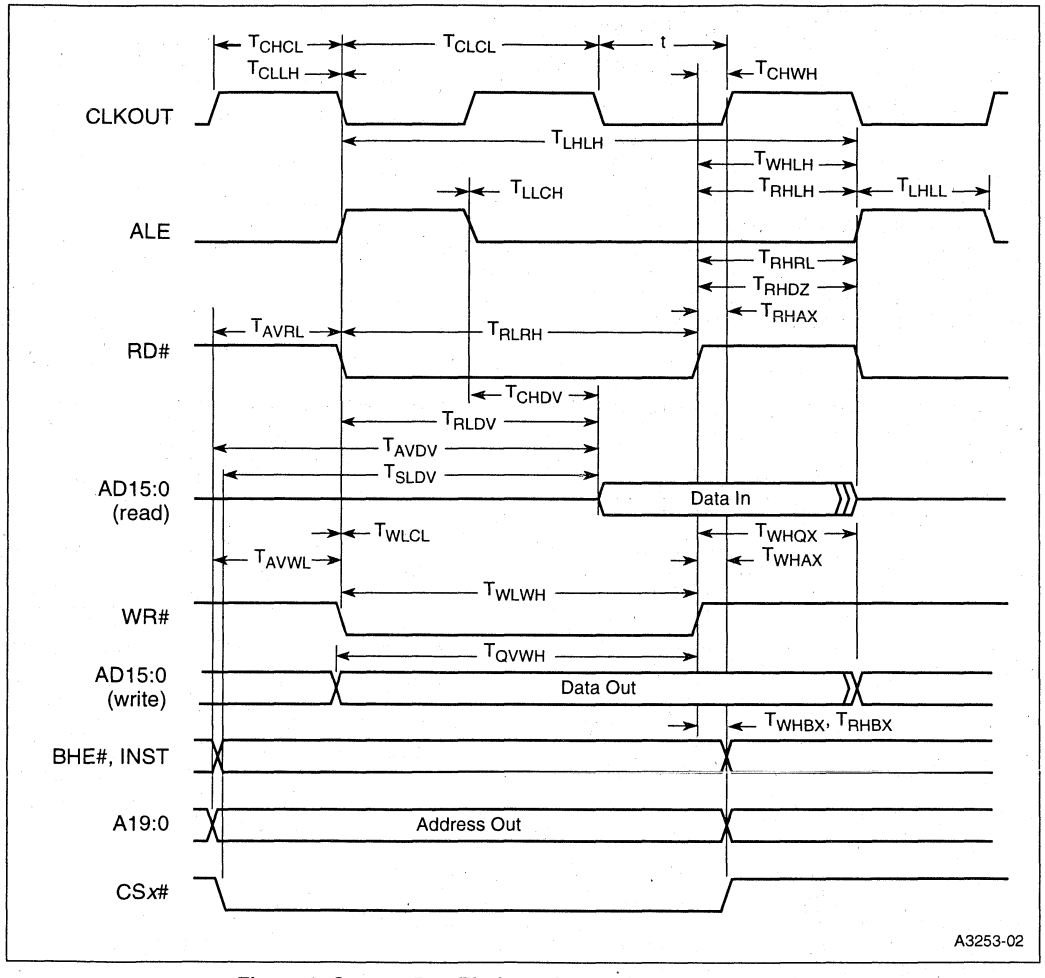


Figure 9. System Bus Timings, Demultiplexed Bus Mode

6.2.4.2 READY Timing, Demultiplexed Bus

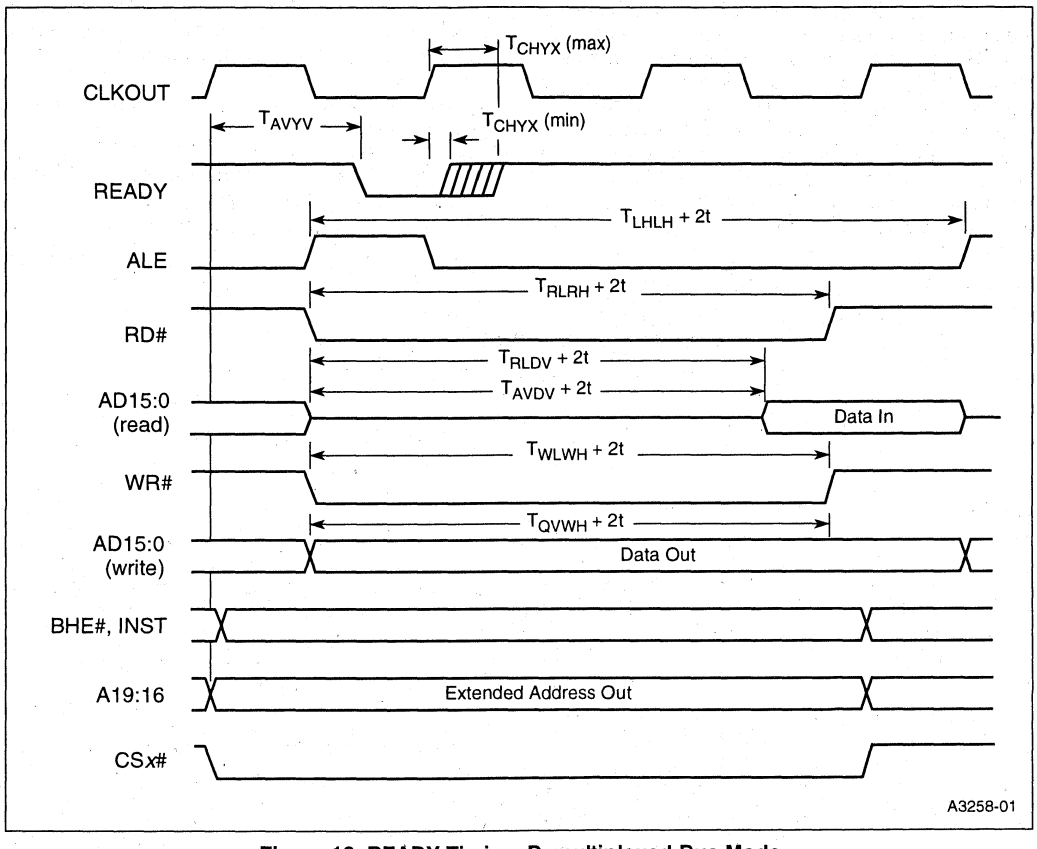


Figure 10. READY Timing, Demultiplexed Bus Mode

6.2.4.3 80296SA Deferred Bus Timing Mode

The deferred bus cycle mode is designed to reduce bus contention when using the 80296SA in demultiplexed mode with slow memory devices. Unlike the 8XC196NU, in which this bus mode has to be enabled through the CCR to take advantage of the feature, the 80296SA automatically invokes this mode whenever the appropriate conditions occur. In the deferred mode, a delay of the WR# signal and the next bus cycle will occur in the first bus cycle following a chip-select change and the first write cycle following a read cycle. This mode will work in parallel with wait states. Refer to Figure 11 to determine which control signals are affected.

Cycle 1 is a normal 4t read cycle. Cycle 2 is a write cycle that follows a read cycle, so a 2t delay of the next bus cycle is inserted. Notice that the chip-select change at the beginning of cycle 2 did not cause a double delay (4t). The chip-select change in cycle 3, a read cycle, causes a 2t delay.

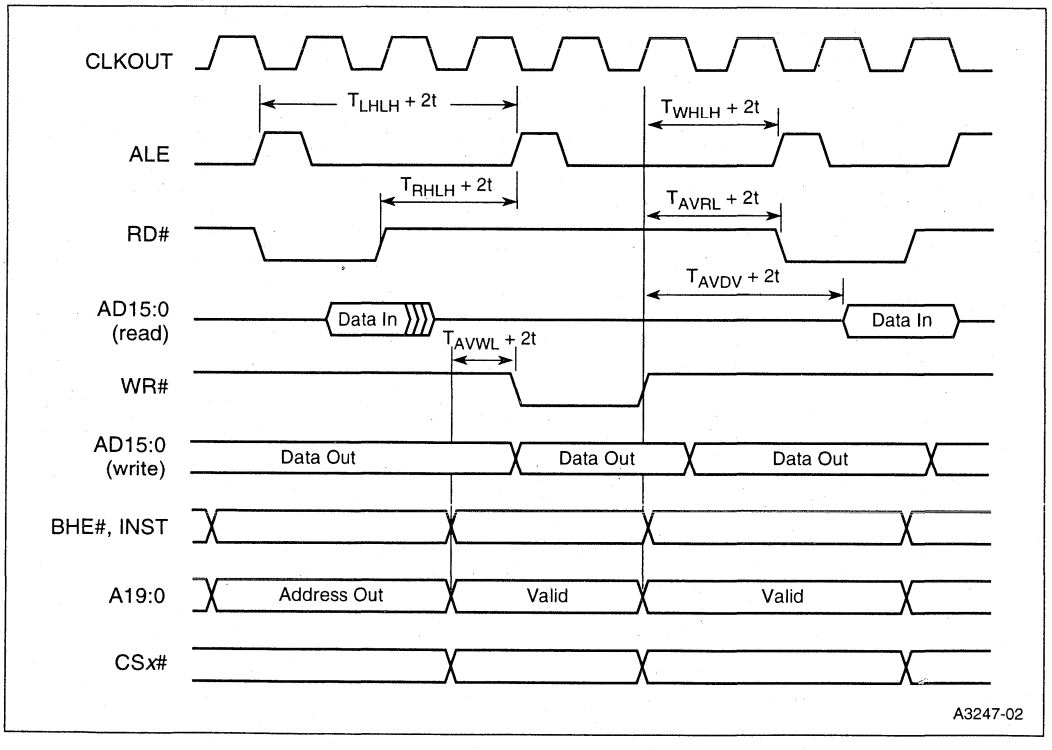


Figure 11. Deferred Bus Mode Timing Diagram

6.2.5 HOLD#, HLDA# TIMINGS

Table 14. HOLD#, HLDA# Timings

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD# Setup time (to guarantee recognition at next clock)	30		ns
T_{CLHAL}	CLKOUT Low to HLDA# Low	–15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	–15	15	ns
T_{HALAZ}	HLDA# Low to Address Float		33	ns
T_{HALBZ}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	–25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	–25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	–20		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	–20		ns

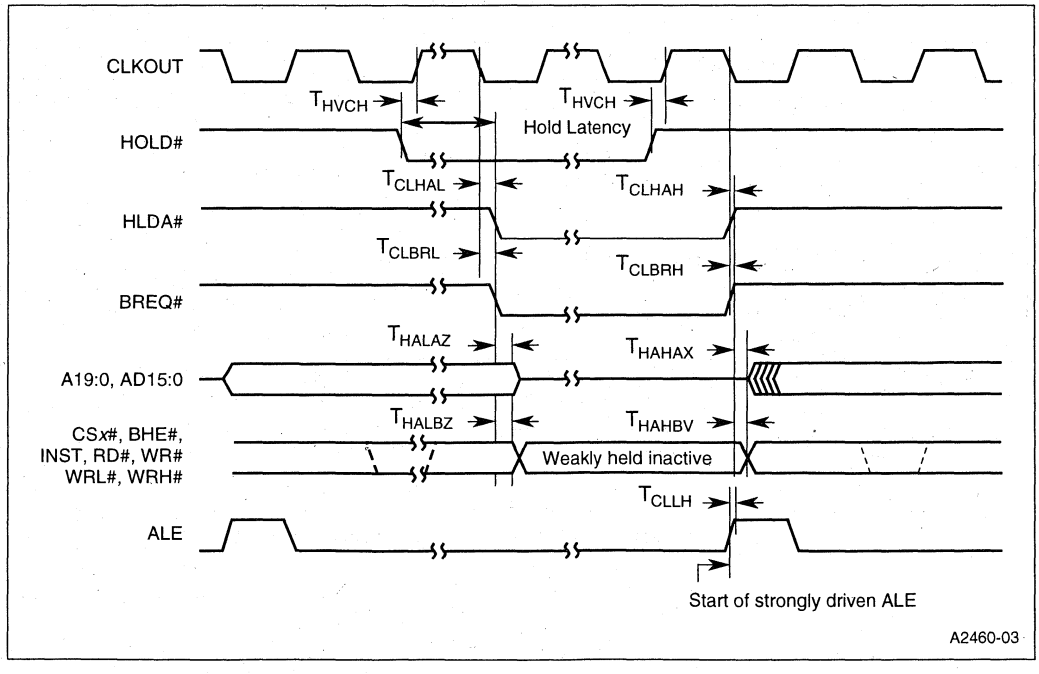


Figure 12. HOLD#, HLDA# Timing Diagram

6.2.6 AC CHARACTERISTICS — SERIAL PORT, SYNCHRONOUS MODE 0

Table 15. Serial Port Timing — Synchronous Mode 0

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock period[†] SP_BAUD ≥ x002H SP_BAUD = x001H	 6t 4t		 ns ns
T_{XLXH}	Serial Port Clock falling edge to rising edge [†] SP_BAUD ≥ x002H SP_BAUD = x001H	 4t – 15 2t – 15	 4t + 15 2t + 15	 ns ns
T_{QVXH}	Output data setup to clock high (see Note) SP_BAUD ≥ x002H SP_BAUD = x001H	 4t – 15 2t – 15	 4t + 15 2t + 15	 ns
T_{XHQX}	Output data hold after clock high	2t – 20		ns
T_{XHQV}	Next output data valid after clock high		2t + 20	ns
T_{DVXH}	Input data setup to clock high (see Note) SP_BAUD ≥ x002H SP_BAUD = x001H	 2t + 10 t + 10		 ns
T_{XHDX}	Input data hold after clock high	0		ns
T_{XHQZ}	Last clock high to output float		2t + 15	ns

[†] The minimum baud-rate (SP_BAUD) register value is x002H for receptions and x001H for transmissions.

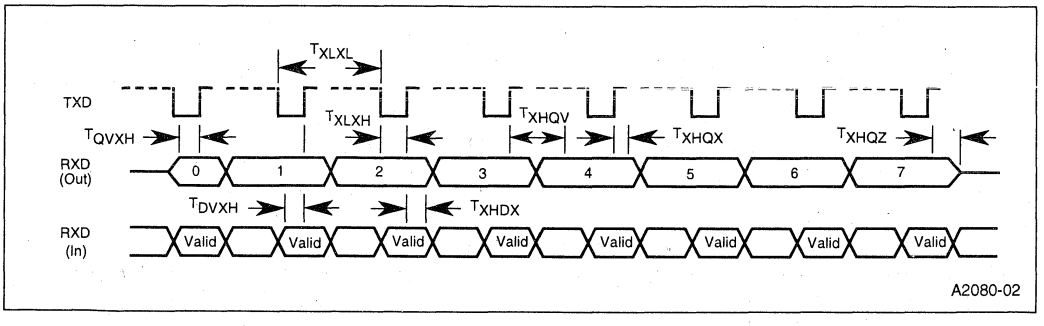


Figure 13. Serial Port Waveform — Synchronous Mode 0

6.2.7 EXTERNAL CLOCK DRIVE

Table 16. External Clock Drive

Symbol	Parameter	Min	Max	Units
F_{XTAL1}	External Input Frequency ($1/T_{XLXL}$), PLL disabled	16	50†	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 2x mode	8	25	MHz
	External Input Frequency ($1/T_{XLXL}$), PLL in 4x mode	8	12.5	MHz
T_{XTAL1}	Oscillator Period (T_{XLXL}), PLL disabled	20	62.5	ns
	Oscillator Period (T_{XLXL}), PLL in 2x mode	40	125	ns
	Oscillator Period (T_{XLXL}), PLL in 4x mode	80	125	ns
T_{XHXX}	High Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXX}	Low Time	$0.35T_{XTAL1}$	$0.65T_{XTAL1}$	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

† Assumes an external clock; the maximum input frequency for an external crystal oscillator is 25 MHz.

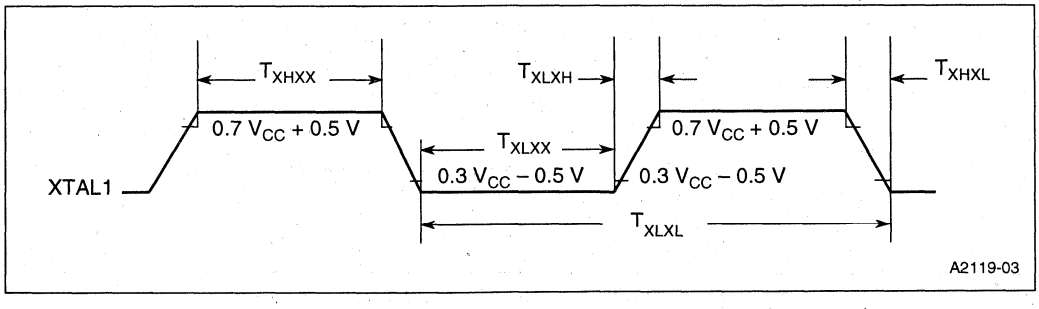
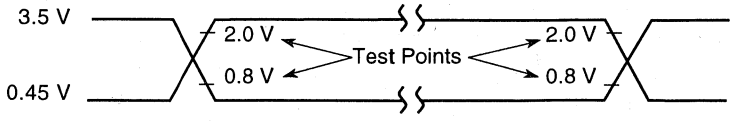


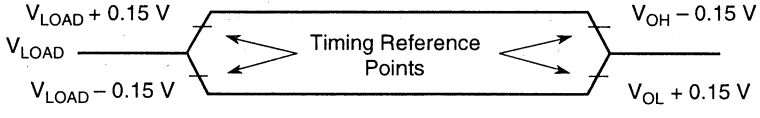
Figure 14. External Clock Drive Waveforms



Note:
AC testing inputs are driven at 3.5 V for a logic " 1" and 0.45 V for a logic " 0" . Timing measurements are made at 2.0 V for a logic " 1" and 0.8 V for a logic " 0".

A2120-04

Figure 15. AC Testing Input and Output Waveforms During 5.0 Volt Testing



Note:
For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A2121-03

Figure 16. Float Waveforms During 5.0 Volt Testing

7.0 THERMAL CHARACTERISTICS

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology. The *Components Quality and Reliability Handbook* (order number 210997) provides quality and reliability information.

Table 17. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
100-pin SQFP	47°C/W	13°C/W
100-pin QFP	50°C/W	16°C/W

8.0 80296SA ERRATA

The 80296SA may contain design defects or errors known as errata. Characterized errata that may cause the 80296SA's behavior to deviate from published specifications are documented in a specification update. Specification updates can be obtained from your local Intel sales office or from the World Wide Web (*www.intel.com*).

9.0 DATASHEET REVISION HISTORY

This datasheet is valid for devices with an "A" at the end of the topside tracking number. Datasheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This is the -002 version of the datasheet. The following changes were made in this version:

1. The "Intel Confidential" designation was removed for publication.
2. A heading was added for Section 1.0, "Product Overview," and the remaining sections were renumbered.
3. The errata list was replaced with a reference to the specification update document.

The following changes were made in the -001 version of the datasheet:

1. Throughout the datasheet, the product name was changed to read "80296SA" instead of "80C296SA."
2. The feature list was clarified.
3. A table of contents was added.
4. The block diagram was changed.
5. Several sections were rearranged and section numbers were assigned. "Thermal Characteristics" was moved to Section 7.0; a section heading was added for "Nomenclature Overview," Section 2.0; a section heading was added for "Address Map" and it was moved to Section 5.0; a section heading was added for "Pinout," and it was moved to Section 3.0; the section heading "Pin Descriptions" was changed to "Signals," Section 4.0. The remaining sections were assigned section numbers: "Electrical Characteristics" is Section 6.0; "Errata" is Section 8.0, and "Datasheet Revision History" is Section 9.0.
6. Table 2 was changed to Table 1 and the "process information" was corrected to show that "no mark" signifies a CHMOS process.
7. Table 3 was changed to Table 7 and several clarifications were made.
8. Figure 3 was changed to correct the product name. Pin assignments did **not** change.
9. Table 4 was changed to Table 2 and pin 3 was changed from "no connection" to "tie to V_{CC}."
10. Figure 4 was changed to correct the product name. Pin assignments did **not** change.
11. Figure 5, "I_{CC} versus Frequency in Reset," was added. Remaining figure numbers were incremented.
12. Table 6 was changed to Table 4 and a note for handling the "no connection" pins was added.
13. Table 8 was changed to Table 6. The descriptions of BREQ#, HLDA#, and HOLD# were changed to reflect their operation during hold. The description of the ONCE signal was changed to reflect the correct states of READY, RESET#, and NMI during ONCE mode. The description of PLLEN2:1 was

changed to show the correct pin states to achieve each phase-locked loop (PLL) clock multiplier mode. The descriptions of RPD and RESET# were changed to reflect system requirements when using the PLL.

14. Two notes were added to clarify the "Operating Conditions" in the "Electrical Characteristics" section.
15. Table 9 was changed to Table 8, the notes were re-ordered, and the following specifications were changed:
    - I_{CC} max was changed to 150 mA (from 120 mA).
    - V_{OH} min was changed to V_{CC}–0.5 V (from V_{CC}–0.3 V) at I_{OH} = –200µA.
    - V_{OH} min was changed to V_{CC}–0.9 V (from V_{CC}–0.7V) at I_{OH} = –3.2 mA.
    - Test condition for V_{OL1} max = 0.45 V was changed to I_{OL} = 8 mA (from I_{OL} = 10 mA).
    - R_{RST} min and max were changed to 50 kΩ and 150 kΩ (from 9 kΩ and 95 kΩ).
    - V_{OH3} min specification was added.
16. Table 10 was divided into two tables: timing specifications that the microcontroller will meet (Table 10) and those that the external memory system must meet (Table 11). Note 7 was deleted and the remaining notes were re-ordered. The following specifications were changed or added in Table 10:
    - F_{XTAL1} min for the PLL in 4x mode was changed to 8 MHz (from 4 MHz); a clarifying note was added.
    - T_{XHCH} min was changed to 3 ns (from TBD).
    - T_{LLAX} min was changed to 1 ns (from TBD).
    - T_{LLRL} min was changed to 3 ns (from TBD)
    - T_{RHAX} min was changed to t – 4 ns (from t).
    - T_{AVWL} min (2t – 25) was added to Table 10.
    - T_{SLDV} min (4t – 28) was added to Table 11.
17. Table 11 was divided into two tables: timing specifications that the microcontroller will meet (Table 12) and those that the external memory system must meet (Table 13). Note 7 was deleted and the remaining notes were re-ordered. The following specifications were changed:
    - F_{XTAL1} min for the PLL in 4x mode was changed to 8 MHz (from 4 MHz); a clarifying note was added.
    - T_{WHQX} min was changed to t – 5 ns (from t – 2 ns).
18. Figure 6 was changed to show the correct PLLEN2:1 values to select the 2x clock multiplier mode.
19. Table 13 was changed to Table 15 and a note was added.
20. Table 14 was changed to Table 16, $1/T_{XLXL}$ specifications for each phase-locked loop (PLL) mode were added, and Note 2 was deleted.

PRELIMINARY

8XC196MC
INDUSTRIAL MOTOR CONTROL MICROCONTROLLER

87C196MC 16 Kbytes of On-Chip OTPROM*
87C196MC, ROM 16 Kbytes of On-Chip Factory-Programmed OTPROM
80C196MC ROMless

- **High-Performance CHMOS 16-Bit CPU**
- **16 Kbytes of On-Chip OTPROM/ Factory-Programmed OTPROM**
- **488 bytes of On-Chip Register RAM**
- **Register to Register Architecture**
- **Up to 53 I/O Lines**
- **Peripheral Transaction Server (PTS) with 11 Prioritized Sources**
- **Event Processor Array (EPA)**
  - **— 4 High Speed Capture/Compare Modules**
  - **— 4 High Speed Compare Modules**
- **Extended Temperature Standard**
- **Two 16-Bit Timers with Quadrature Decoder Input**
- **3-Phase Complementary Waveform Generator**
- **13 Channel 8/10-Bit A/D with Sample/ Hold with Zero Offset Adjustment H/W**
- **14 Prioritized Interrupt Sources**
- **Flexible 8-/16-Bit External Bus**
- **1.75 μs 16 x 16 Multiply**
- **3 μs 32/16 Divide**
- **Idle and Power Down Modes**

The 8XC196MC is a 16-bit microcontroller designed primarily to control 3 phase AC induction and DC brushless motors. The 8XC196MC is based on Intel's MCS® 96 16-bit microcontroller architecture and is manufactured with Intel's CHMOS process.

The 8XC196MC has a three phase waveform generator specifically designed for use in "Inverter" motor control applications. This peripheral allows for pulse width modulation, three phase sine wave generation with minimal CPU intervention. It generates 3 complementary non-overlapping PWM pulses with resolutions of 0.125 μs (edge trigger) or 0.250 μs (centered).

The 8XC196MC has 16 Kbytes on-chip OTPROM/ROM and 488 bytes of on-chip RAM. It is available in three packages; PLCC (84-L), SDIP (64-L) and EIAJ/QFP (80-L).

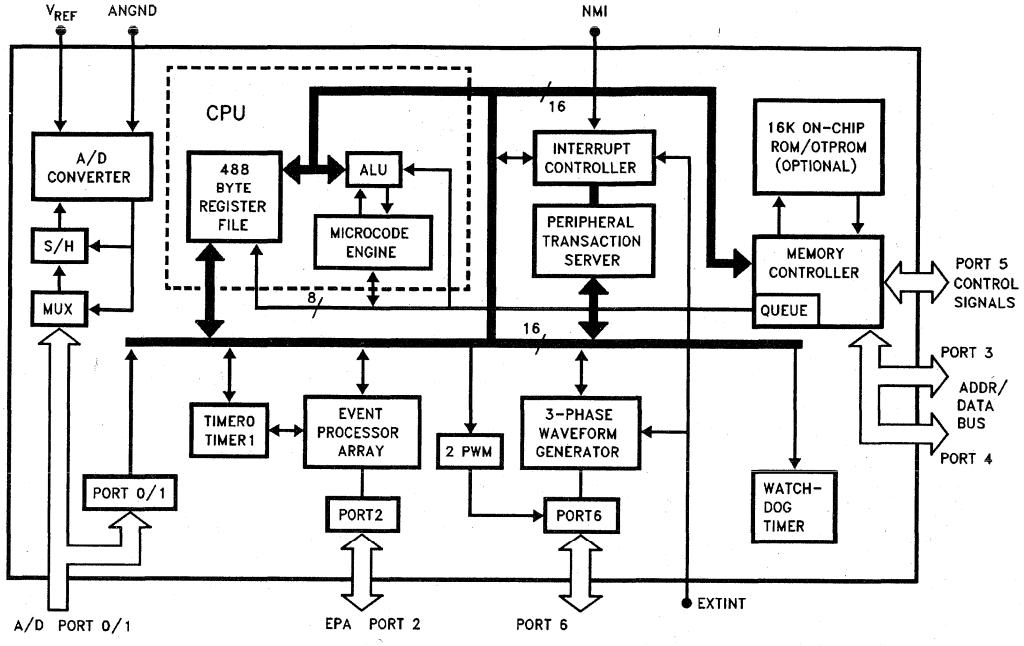
Note that the 64-L SDIP package does not include P1.4, P2.7, P5.1 and the CLKOUT pins.

Operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

The 87C196MC contains 16 Kbytes on-chip OTPROM. The 83C196MC contains 16 Kbytes on-chip ROM. All references to the 80C196MC also refers to the 83C196MC and 87C196MC unless noted.

*OTPROM (One Time Programmable Read Only Memory) is the same as EPROM but it comes in an unwindowed package and cannot be erased. It is user programmable.

April 1994 Order Number: 270946-005

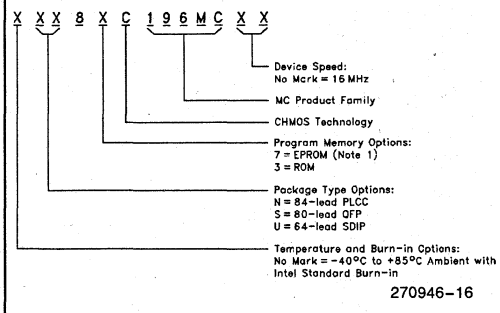


NOTE:
Connections between the standard I/O ports and the bus are not shown.

Figure 1. 87C196MC Block Diagram

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196MC is 84-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
1. EPROMs are available as One Time Programmable (OTPROM) only.

Figure 3. The 8XC196MC Family Nomenclature

Thermal Characteristics

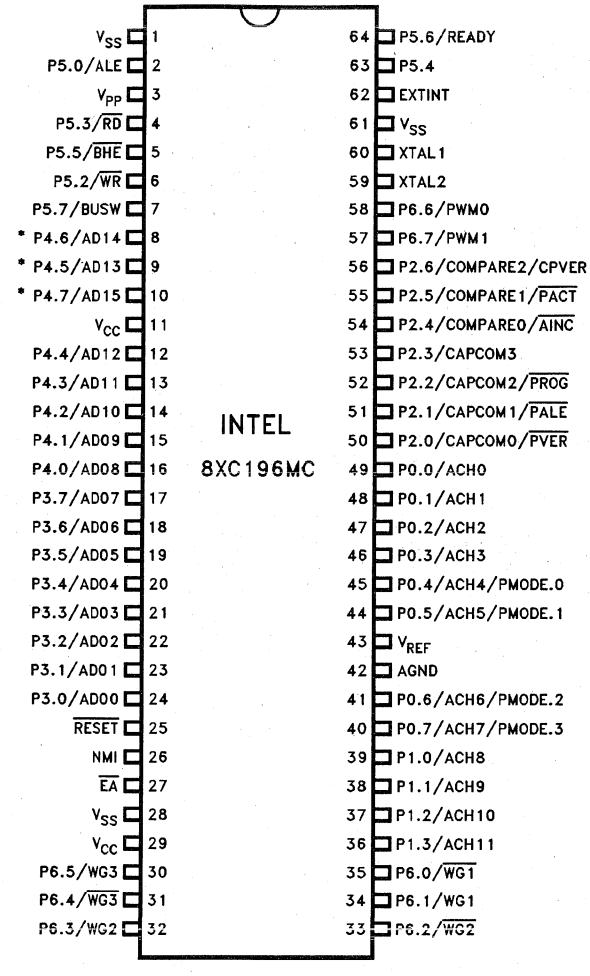
Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W
SDIP	TBD	TBD

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

8XC196MC Memory Map

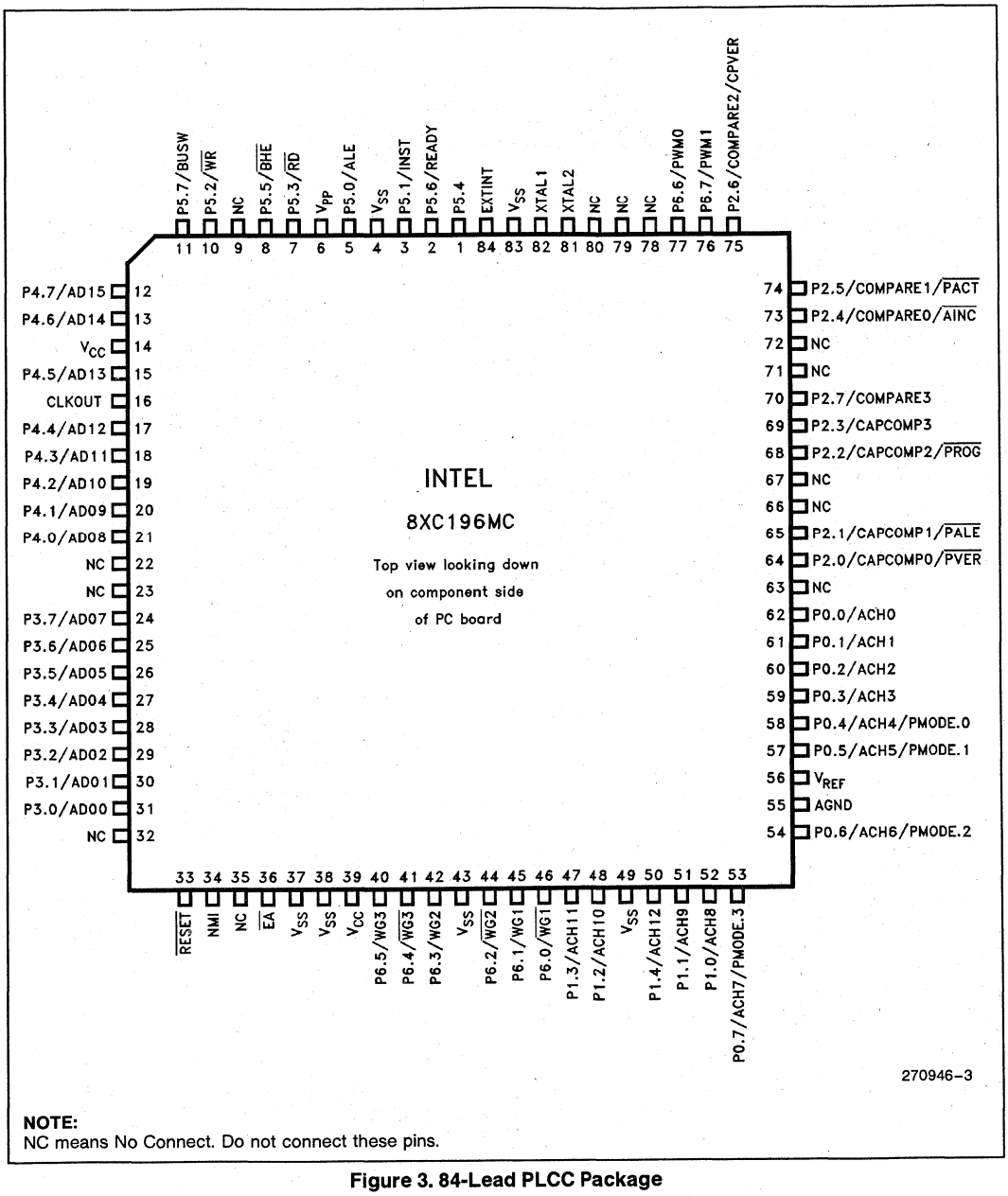
Description	Address
External Memory or I/O	0FFFFH 06000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	5FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201CH
Reserved. Must Contain 20H (Note 5)	201BH
CCB1	201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB0	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
SFR's	1FFFH 1F00H
External Memory	1EFFH 0200H
488 Bytes Register RAM (Note 1)	01FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 03FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196KC for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.



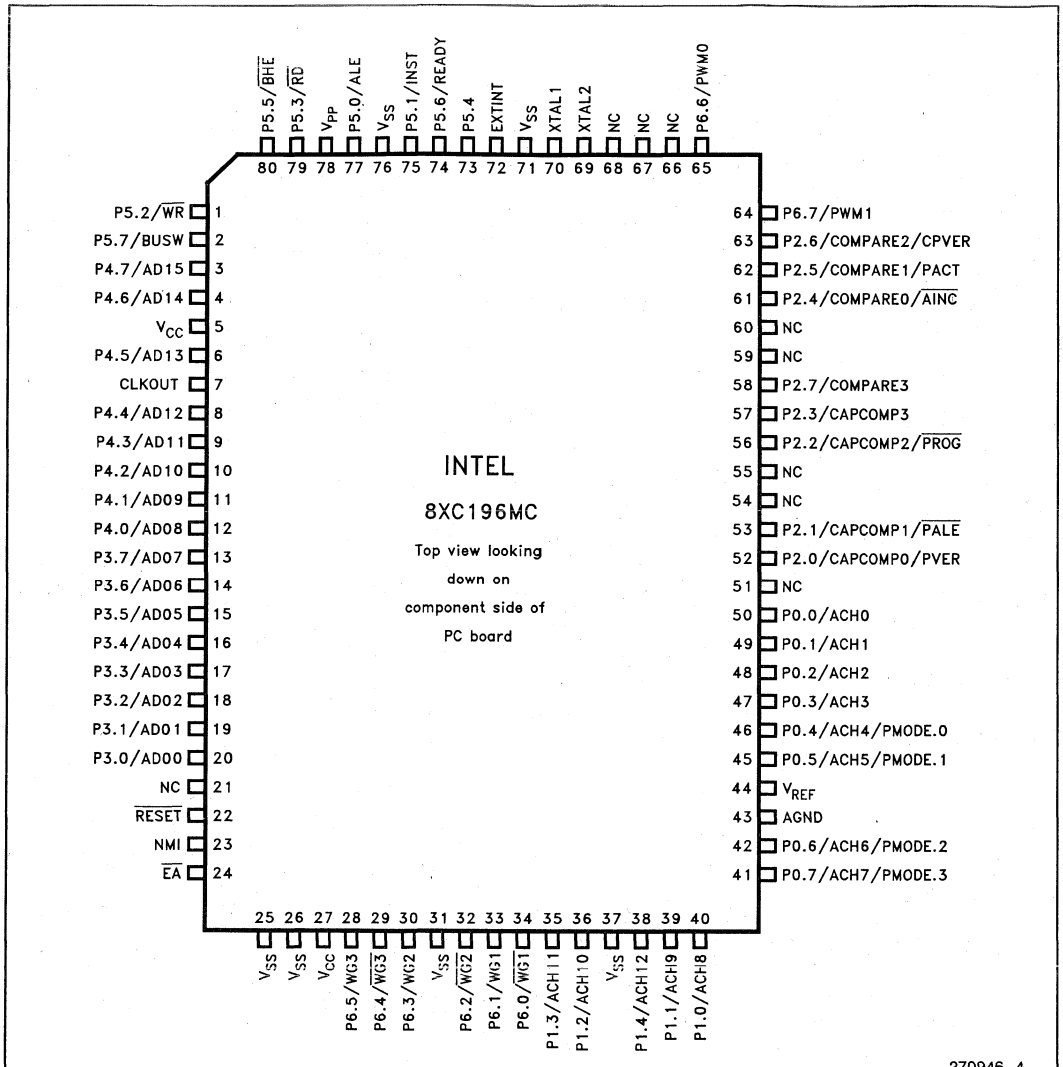
NOTE:
*The pin sequence is correct.
The 64-Lead SDIP package does not include the following pins: P1.4/ACH12, P2.7/COMPARE3, P5.1/INST, CLKOUT.

Figure 2. 64-Lead Shrink DIP (SDIP) Package



NOTE:
NC means No Connect. Do not connect these pins.

Figure 3. 84-Lead PLCC Package



NOTE:
NC means No Connect. Do not connect these pins.

Figure 4. 80-Lead Shrink EIAJQFP (Quad Flat Pack)

PIN DESCRIPTIONS (Alphabetically Ordered)

Symbol	Function
ACH0–ACH12 (P0.0–P0.7, P1.0–P1.4)	Analog inputs to the on-chip A/D converter. ACH0–7 share the input pins with P0.0–7 and ACH8–12 share pins with P1.0–4. If the A/D is not used, the port pins can be used as standard input ports.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ALE/$\overline{ADV}$(P5.0)	Address Latch Enable or Address Valid output, as selected by CCR. Both options allow a latch to demultiplex the address/data bus on the signal's falling edge. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. ALE/$\overline{ADV}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE/ADV.
$\overline{BHE}$/$\overline{WRH}$ (P5.5)	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.
BUSWIDTH (P5.7)	Input for bus width selection. If CCR bits 1 and 2 = 1, this pin dynamically controls the bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If it is high, a 16-bit cycle occurs. This pin can be used as standard I/O when not used as BUSWIDTH.
CAPCOMP0–CAPCOMP3 (P2.0–P2.3)	The EPA Capture/Compare pins. These pins share P2.0–P2.3. If not used for the EPA, they can be configured as standard I/O pins.
CLKOUT	Output of the internal clock generator. The frequency is ½ of the oscillator frequency. It has a 50% duty cycle.
COMPARE0–COMPARE3 (P2.4–P2.7)	The EPA Compare pins. These pins share P2.4–P2.7. If not used for the EPA, they can be configured as standard I/O pins.
$\overline{EA}$	External Access enable pin. $\overline{EA}$ = 0 causes all memory accesses to be external to the chip. $\overline{EA}$ = 1 causes memory accesses from location 2000H to 5FFFH to be from the on-chip OTPROM/QROM. $\overline{EA}$ = 12.5V causes execution to begin in the programming mode. $\overline{EA}$ is latched at reset.
EXTINT	A programmable input on this pin causes a maskable interrupt vector through memory location 203CH. The input may be selected to be a positive/negative edge or a high/low level using WG_PROTECT (1FCEH).
INST (P5.1)	INST is high during the instruction fetch from the external memory and throughout the bus cycle. It is low otherwise. This pin can be configured as standard I/O if not used as INST.
NMI	A positive transition on this pin causes a non-maskable interrupt which vectors to memory location 203EH. If not used, it should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port0 pins should not be left floating. These pins also used to select programming modes in the OTPROM devices.
PORT1	5-bit high impedance input-only port. P1.0–P1.4 are also used as A/D converter inputs. In addition, P1.2 and P1.3 can be used as Timer 1 clock input and direction select respectively.
PORT2	8-bit bidirectional I/O port. All of the Port2 pins are shared with the EPA I/O pins (CAPCOMP0–3 and COMPARE0–3).
PORT3 PORT4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional I/O port. 7 of the pins are shared with bus control signals ($\overline{ALE}$, INST, $\overline{WR}$, $\overline{RD}$, $\overline{BHE}$, READY, BUSWIDTH). Can be used as standard I/O.

PIN DESCRIPTIONS (Alphabetically Ordered) (Continued)

Symbol	Function
PORT6	8-bit output port. P6.6 and P6.7 output PWM, the others are used as the Wave Form Generator outputs. Can be used as standard output ports.
PWM0, PWM1 (P6.6, P6.7)	Programmable duty cycle, Programmable frequency Pulse Width Modulator pins. The duty cycle has a resolution of 256 steps, and the frequency can vary from 122 Hz to 31 KHz (16 MHz input clock). Pins may be configured as standard output if PWM is not used.
$\overline{RD}$ (P5.3)	Read signal output to external memory. $\overline{RD}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{RD}$.
READY (P5.6)	Ready input to lengthen external memory cycles. If READY = 0, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{RESET}$	Reset input to and open-drain output from the chip. Held low for at least 16 state times to reset the chip. Input high for normal operation. $\overline{RESET}$ has an Ohmic internal pullup resistor.
T1CLK (P1.2)	Timer 0 Clock input. This pin has two other alternate functions: ACH10 and P1.2.
T1DIR (P1.3)	Timer 0 Direction input. This pin has two other alternate functions: ACH11 and P1.3.
V_{PP}	The programming voltage is applied to this pin. It is also the timing pin for the return from Power Down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If the Power Down feature is not used, connect the pin to V_{CC}.
WG1–WG3/$\overline{WG1}$–$\overline{WG3}$ (P6.0–P6.5)	3 phase output signals and their complements used in motor control applications. The pins can also be configured as standard output pins.
$\overline{WR}$/$\overline{WRL}$ (P5.2)	Write and Write Low output to external memory. $\overline{WR}$ will go low every external write. $\overline{WRL}$ will go low only for external writes to an even byte. Can be used as standard I/O when not used as $\overline{WR}$/$\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.
PMODE (P0.4–7)	Determines the EPROM programming mode.
$\overline{PACT}$ (P2.5)	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
$\overline{PALE}$ (P2.1)	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{PROG}$ (P2.2)	A falling edge in Slave Programming Mode begins programming. A rising edge ends programming.
PVER (P2.0)	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER (P2.6)	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.
$\overline{AINC}$ (P2.4)	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias ..... −40°C to +85°C

Storage Temperature ..... −65°C to +150°C

Voltage from $\overline{EA}$ or V_{PP}
to V_{SS} or ANGND ..... +13.00V

Voltage on V_{PP} or $\overline{EQ}$
to V_{SS} or ANGND ..... −0.5V to 13.0V

Voltage on Any Other Pin
to V_{SS} or ANGND ..... −0.5V to +7.0V(1)

Power Dissipation ..... 1.5W(2)

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
F_{OSC}	Oscillator Frequency	8	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential. Also V_{SS} and V_{SS1} must be at the same potential.

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage Port 2 and 5, P6.6, P6.7, CLKOUT		0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage on Port 3/4		1.0	V	I_{OL} = 15 mA
V_{OL2}	Output Low Voltage on Port 6.0–6.5		0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 µA I_{OH} = −3.2 mA I_{OH} = −7 mA
$V_{th+} - V_{th-}$	Hysteresis Voltage Width on $\overline{RESET}$	0.2		V	Typical

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Leakage Current on All Input Only Pins			±10	μA	$0V < V_{IN} < V_{CC}-0.3V$ (in RESET)
I_{LI1}	Input Leakage Current on Port0 and Port1			±3	μA	$0V < V_{IN} < V_{REF}$
I_{IL}	Input Low Current on BD Ports (Note 1)			−70	μA	$V_{IN} = 0.3\ V_{CC}$
I_{IL1}	Input Low Current on P5.4 and P2.6 during Reset			−7	mA	$0.2\ V_{CC}$
I_{OH}	Output High Current on P5.4 and P2.6 during Reset	−2			mA	$0.7\ V_{CC}$
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Conversion Reference Current		2	5	mA	
I_{IDL}	Idle Mode Current		15	30	mA	
I_{PD}	Power-Down Mode Current		5	50	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	$\overline{\text{RESET}}$ Pin Pullup Resistor	6k		65k	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:

1. BD (Bidirectional ports) include:
   - P2.0–P2.7, except P2.6
   - P3.0–P3.7
   - P4.0–P4.7
   - P5.0–P5.3
   - P5.5–P5.7
2. During normal (non-transient) conditions, the following total current limits apply:

P6.0–P6.5	I_{OL}: 40 mA	I_{OH}: 28 mA
P3	I_{OL}: 90 mA	I_{OH}: 42 mA
P4	I_{OL}: 90 mA	I_{OH}: 42 mA
P5, CLKOUT	I_{OL}: 35 mA	I_{OH}: 35 mA
P2, P6.6, P6.7	I_{OL}: 63 mA	I_{OH}: 63 mA

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H — High
L — Low
V — Valid
X — No Longer Valid
Z — Floating

Signals:

A — Address
B — $\overline{BHE}$
C — CLKOUT
D — DATA
G — Buswidth
H — $\overline{HOLD}$
HA — $\overline{HLDA}$
L — ALE/$\overline{ADV}$
BR — $\overline{BREQ}$
R — $\overline{RD}$
W — $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X — XTAL1
Y — READY
Q — Data Out

AC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The system must meet the following specifications to work with the 87C196MC:

Symbol	Parameter	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1	8	16	MHz	3
T_{OSC}	$1/F_{XTAL}$	62.5	125	ns	
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns	4
T_{YLYH}	Not READY Time	No Upper Limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	1
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	1
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns	4
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	2
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 22$	ns	2
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2T_{OSC} * N$, where N = number of wait states.
3. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
4. These timings are included for compatibility with older −90 and BH products. They should not be used for newer high-speed designs.

AC ELECTRICAL CHARACTERISTICS (Continued)

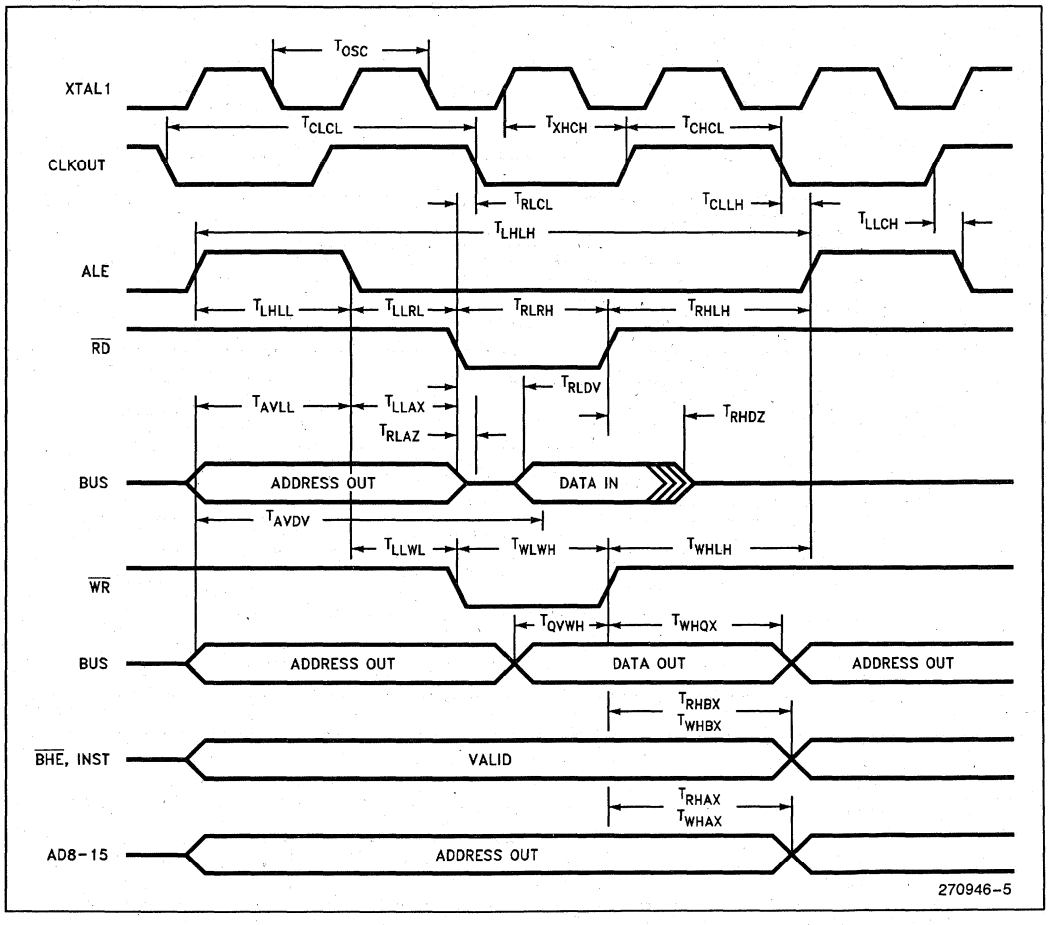
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The 87C196MC will meet the following timing specifications:

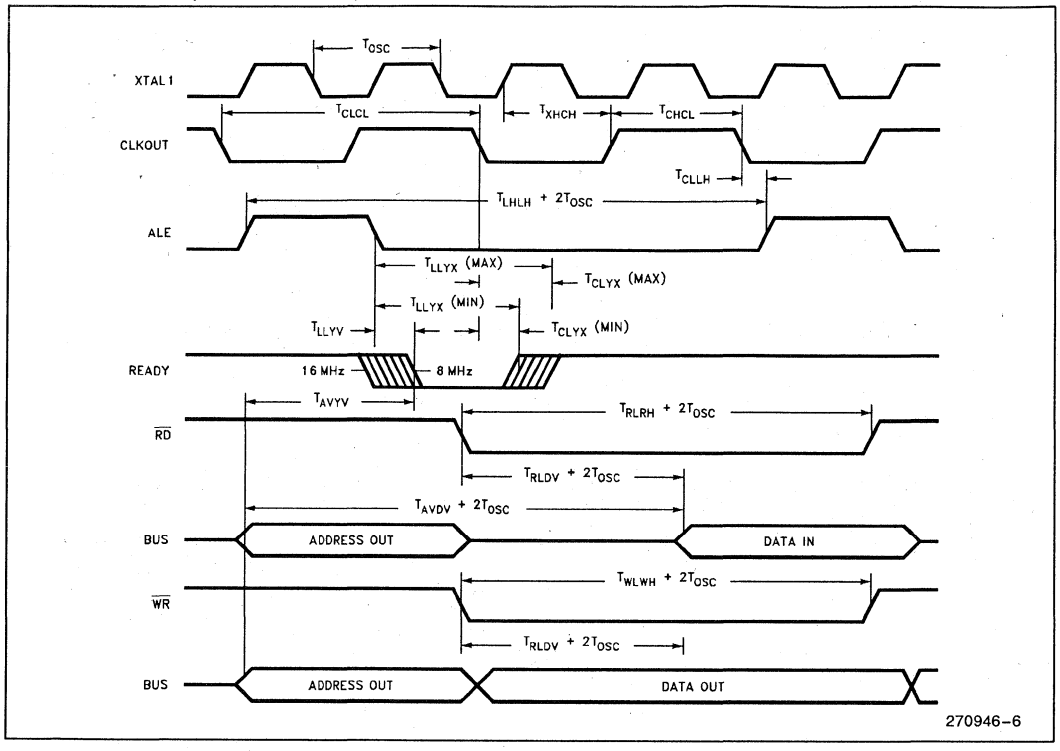
Symbol	Parameter	Min	Max	Units	Notes
T_{XHCH}	XTAL1 to CLKOUT High or Low	30	110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	3
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15		ns	
T_{LLAX}	Address Hold after ALE Falling	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	3
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	1
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns	3
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	1
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising	T_{OSC} − 30		ns	2
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising	T_{OSC} − 30		ns	2

NOTES:
1. Assuming back to back cycles.
2. 8-bit bus only.
3. If wait states are used, add 2 T_{OSC}*N, where N = number of wait states.

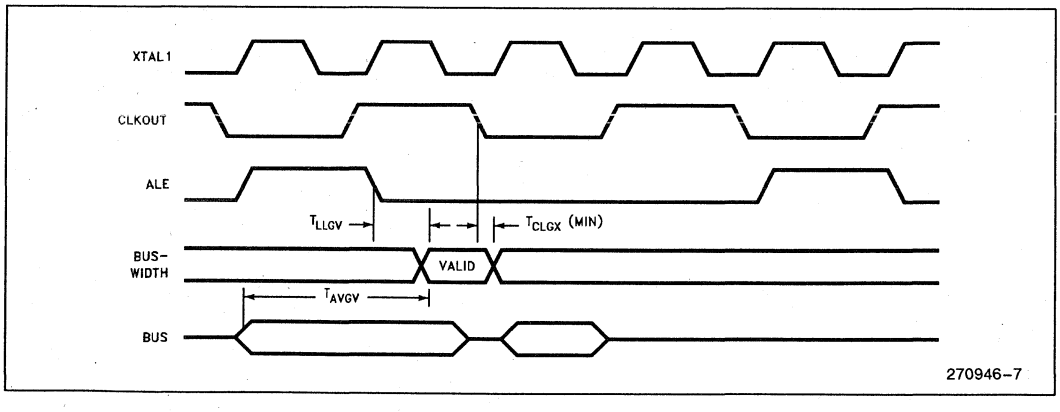
SYSTEM BUS TIMINGS



READY TIMINGS (One Wait State)



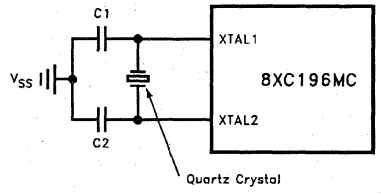
BUSWIDTH TIMINGS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	22		ns
T_{XLXX}	Low Time	22		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

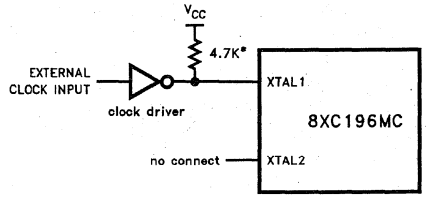
EXTERNAL CRYSTAL CONNECTIONS



270946-14

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

EXTERNAL CLOCK CONNECTIONS



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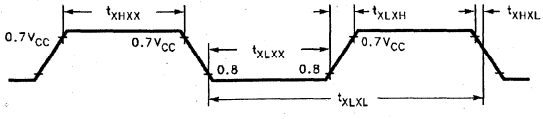
* Required if TTL driver used.
Not needed if CMOS driver is used.

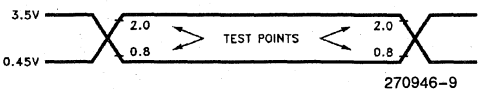
EXTERNAL CLOCK DRIVE WAVEFORMS



270946-8

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

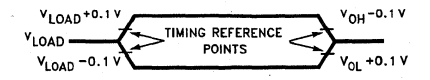
AC TESTING INPUT, OUTPUT WAVEFORMS



270946-9

AC Testing inputs are driven at 3.5V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



270946-10

For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \leq \pm 15$ mA.

A TO D CHARACTERISTICS

The sample and conversion time of the A/D converter in the 8-bit or 10-bit modes is programmed by loading a byte into the AD_TIME Special Function Register. This allows optimizing the A/D operation for specific applications. The AD_TIME register is functional for all possible values, but the accuracy of the A/D converter is only guaranteed for the times specificed in the operating conditions table.

The value loaded into AD_TIME bits 5, 6, 7 determines the sample time, T_{SAM}, and is calculated using the following formula:

$$SAM = \frac{(T_{SAM} \times F_{OSC}) - 2}{8}$$

T_{SAM} = Sample time, μs
F_{OSC} = Processor frequency, MHz
SAM = Value loaded into AD_TIME bits 5, 6, 7

SAM must be in the range 1 through 7.

The value loaded into AD_TIME bits 0–5 determines the conversion time, T_{CONV}, and is calculated using the following formula:

$$CONV = \frac{(T_{CONV} \times F_{OSC}) - 3}{2B} - 1$$

T_{CONV} = Conversion time, μs
F_{OSC} = Processor frequency, MHz
B = 8 for 8-bit conversion
B = 10 for 10-bit conversion
CONV = Value loaded into AD_TIME bits 0–5

CONV must be in the range 2 through 31.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the analog portion of the converter and input port pins. There is also an AD_TEST SFR that allows for conversion on ANGND and V_{REF} as well as adjusting the zero offset. The absolute error listed is WITHOUT doing any adjustments.

A/D CONVERTER SPECIFICATION

The specifications given assume adherence to the operating conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V and 16.0 MHz operating frequency. After a conversion is started, the device is placed in the IDLE mode until the conversion is complete.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	10.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Levels Bits
Absolute Error		0	±4	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±4	LSBs
Differential Non-Linearity		>−1	+2	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB", as used here has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	7.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD__TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over the Above Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1	LSBs
Differential Non-Linearity		>−1	+1	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25			LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB" as used here, has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
T_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	PROG High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

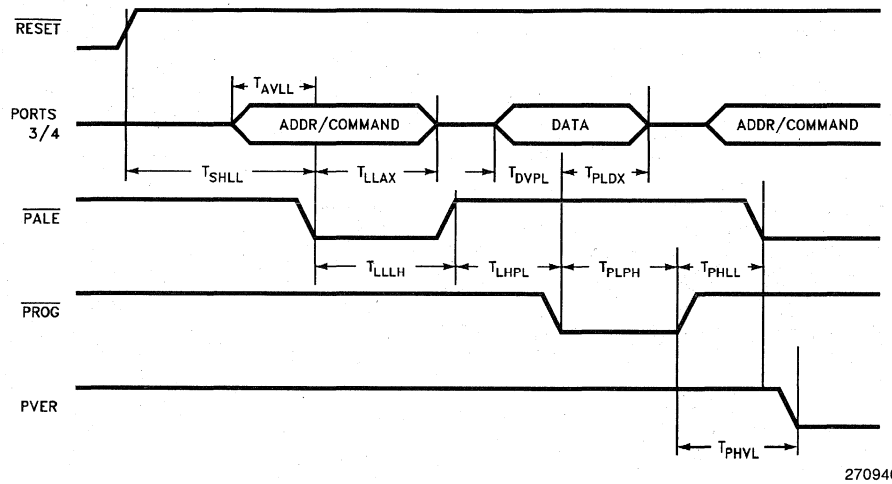
NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

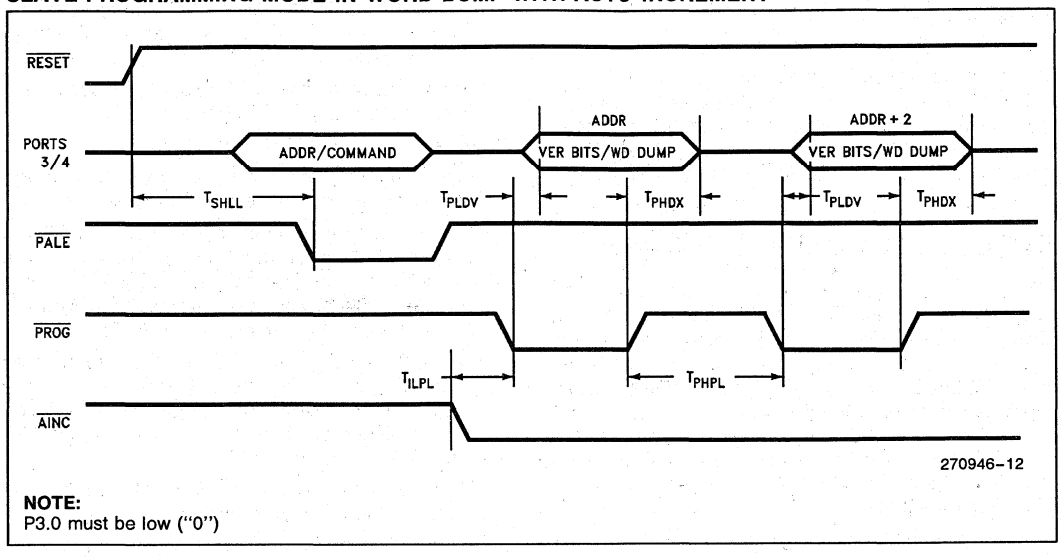
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



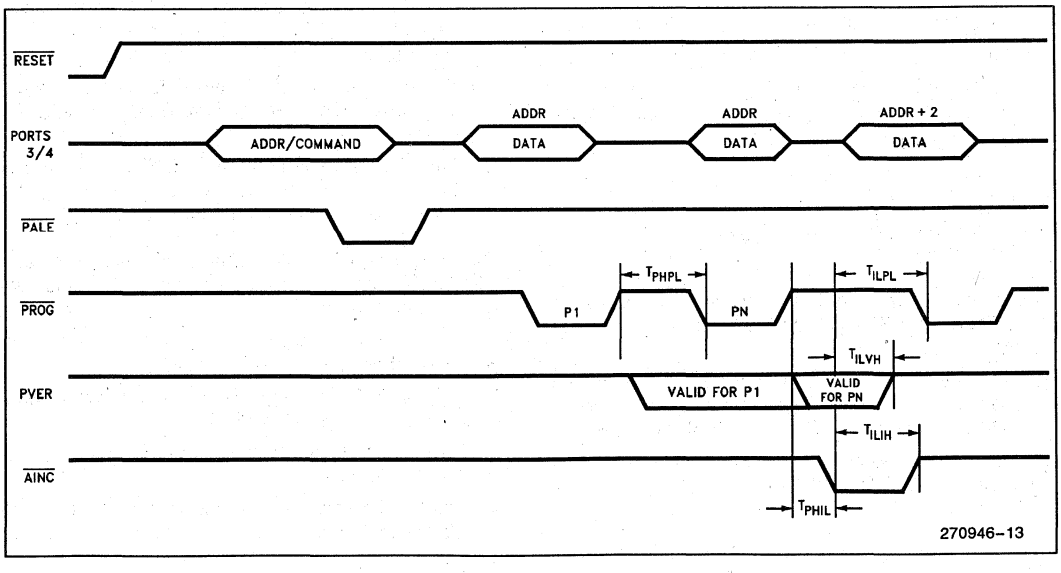
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



87C196MC DESIGN CONSIDERATIONS

When an indirect shift during divide occurs the upper 3 bits of the shift count are not masked completely. If the shift count register has the value 32*n where n = 1, 3, 5 or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

DATA SHEET REVISION HISTORY

This data sheet (270946-004) is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following important differences exist between this data sheet (270946-002) and the previous version (270946-003):

1. The data sheet was reorganized to standard format.
2. Added 83C196MC device.
3. Added package thermal characteristics.
4. Added note on missing pins on SDIP package.
5. Removed SFR maps (now in user's manual).
6. Added note on T_{LLYV} and T_{LLGV} specifications.
7. Changed 10-bit mode T_{CONV} (MIN) to 10.0 μs from 15.0 μs.
8. Changed 10-bit mode T_{CONV} (MAX) to 20.0 μs from 18.0 μs.
9. Changed VREF (MIN) in 8- and 10-bit mode to 4.0V from 4.5V.

The following important differences exist between data sheet 270946-003 and the previous version (270946-002):

1. The data sheet title was changed to better reflect the purpose of the 87C196MC as an AC Inverter/DC Brushless Motor Control Microcontroller.
2. The standard temperature range for this part now covers $-40°C$ to $+85°C$.
3. EXTINT function description now includes WG_PROTECT (1FCEH) as the name and address of the register used to select positive/negative or high/low detection for EXTINT.
4. The memory range 01F00H–01FBFH was added to the SFR map as RESERVED.
5. I_{IL} changed from -60 μA to -70 μA.
6. I_{REF} changed from 5 mA to 2 mA maximum and the typical specification was removed.
7. The READY description of the READY TIMINGS (One Wait State) graphic was modified to denote the shifting of the leading edge of READY versus frequency. At 16 MHz the falling edge of READY occurs before the falling edge of ALE.
8. AC Testing Input, Output Waveform was changed to reflect inputs driven at 3.5V for a Logic "1" and .45V for a Logic "0" and timing measurements made at 2.0V for a Logic "1" and 0.8V for a Logic "0".
9. Float Waveform was changed from $I_{OL}/I_{OH} = \pm 15$ mA to $I_{OL}/I_{OH} \leq \pm 15$ mA
10. AD_TIME register for 10-bit conversions was changed from 0C7H to 0D8H. The number of sample time states was changed from 24 to 25 states, the conversion time states was changed from 80 to 240 states, and the total conversion time for AD_TIME = D8H replaced the total conversion time for AD_TIME = C7H.
11. The number of sample time states for an 8-bit conversion was changed from 20 states to 21 states.
12. There is a single entry in the ERRATA section of this version of the data sheet concerning the results of an indirect shift during divide.

The following important differences exist between this data sheet (270946-002) and the previous version (270946-001):

1. T_A Ambient Temperature Under Bias Min changed from $-20°C$ to $-40°C$.
2. I_{REF} A/D Conversion Reference Current Max changed from 5 mA to 2 mA.
3. Testing levels changed from TTL values to CMOS values.
4. A/D Input Series Resistance Max changed from 1.2 KΩ to 2 KΩ.

8XC196MD
INDUSTRIAL MOTOR CONTROL MICROCONTROLLER

87C196MD 16 Kbytes of On-Chip OTPROM*
87C196MD, ROM 16 Kbytes of On-Chip Factory-Programmed OTPROM
80C196MD ROMless

- High-Performance CHMOS 16-Bit CPU
- 16 Kbytes of On-Chip OTPROM/ Factory-Programmed OTPROM
- 488 bytes of On-Chip Register RAM
- Register to Register Architecture
- Up to 64 I/O Lines
- Peripheral Transaction Server (PTS) with 17 Prioritized Sources
- Event Processor Array (EPA)
  - 6 High Speed Capture/Compare Modules
  - 6 High Speed Compare Modules
- Extended Temperature Standard
- Programmable Frequency Generator
- Two 16-Bit Timers with Quadrature Counting Input
- 3-Phase Complementary Waveform Generator
- 14 Channel 8/10-Bit A/D with Sample/ Hold with Zero Offset Adjustment H/W
- 18 Prioritized Interrupt Sources
- Flexible 8-/16-Bit External Bus
- 1.75 μs 16 x 16 Multiply
- 3 μs 32/16 Divide
- Idle and Power Down Modes

The 8XC196MD is a 16-bit microcontroller designed primarily to control 3 phase AC induction and DC brushless motors. The 8XC196MD is based on Intel's MCS® 96 16-bit microcontroller architecture and is manufactured with Intel's CHMOS process.

The 8XC196MD has a three phase waveform generator specifically designed for use in "Inverter" motor control applications. This peripheral allows for pulse width modulation, three phase sine wave generation with minimal CPU intervention. It generates 3 complementary non-overlapping PWM pulses with resolutions of 0.125 μs (edge trigger) or 0.250 μs (centered).

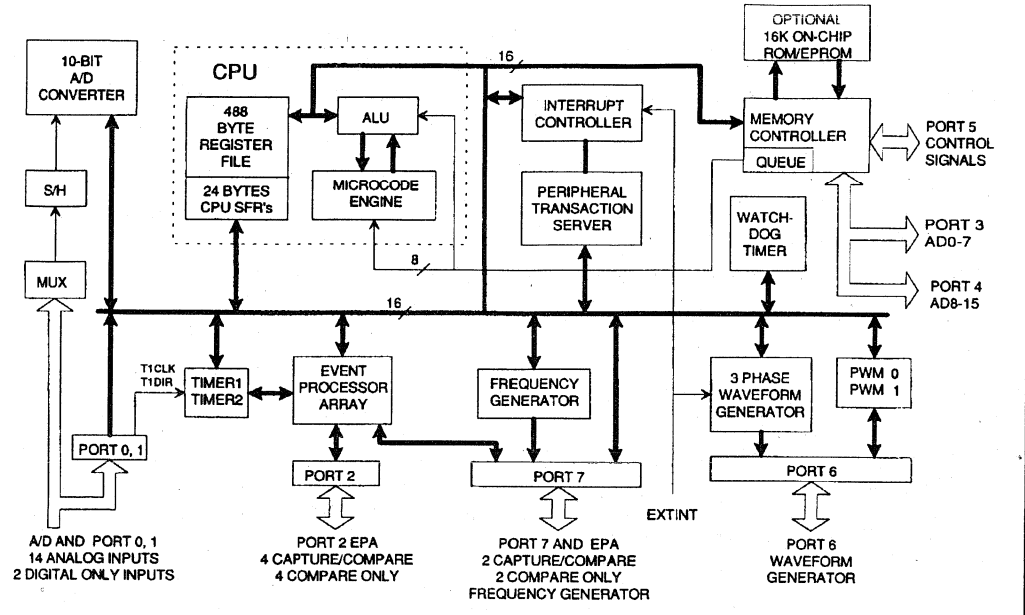
The 8XC196MD has 16 Kbytes on-chip OTPROM/ROM and 488 bytes of on-chip RAM. It is available in two packages; PLCC (84-L) and EIAJ/QFP (80-L).

Operational characteristics are guaranteed over the temperature range of −40°C to +85°C.

The 87C196MD contains 16 Kbytes on-chip OTPROM. The 83C196MD contains 16 Kbytes on-chip ROM. All references to the 80C196MD also refers to the 83C196MD and 87C196MD unless noted.

*OTPROM (One Time Programmable Read Only Memory) is the same as EPROM but it comes in an unwindowed package and cannot be erased. It is user programmable.

April 1994 Order Number: 272323-002

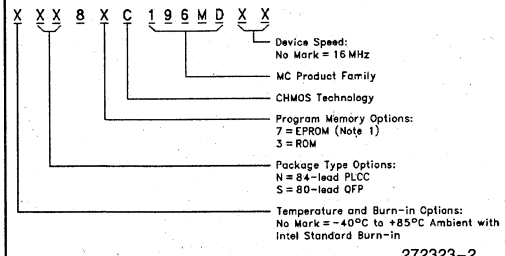


NOTE:
Connections between the standard I/O ports and the bus are not shown.

Figure 1. 87C196MD Block Diagram

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS III-E process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.



EXAMPLE: N87C196MD is 84-Lead PLCC OTPROM, 16 MHz.
For complete package dimensional data, refer to the Intel Packaging Handbook (Order Number 240800).

NOTE:
EPROMs are available as One Time Programmable (OTPROM) only.

Figure 2. The 8XC196MD Family Nomenclature

Table 1. Thermal Characteristics

Package Type	θ_{ja}	θ_{jc}
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

Table 2. 8XC196MD Memory Map

Description	Address
External Memory or I/O	0FFFFH 06000H
Internal ROM/EPROM or External Memory (Determined by $\overline{EA}$)	5FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/EPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201CH
Reserved. Must Contain 20H (Note 5)	201BH
CCB1	201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB0	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
SFR's	1FFFH 1F00H
External Memory	1EFFH 0200H
488 Bytes Register RAM (Note 1)	01FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

NOTES:
1. Code executed in locations 0000H to 01FFH will be forced external.
2. Reserved memory locations must contain 0FFH unless noted.
3. Reserved SFR bit locations must contain 0.
4. Refer to 8XC196MC for SFR descriptions.
5. **WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

8XC196MC AND 8XC196MD DIFFERENCES

INT_MASK1/INT_PEND1 Registers

There are some differences between the 8XC196MC and 8XC196MD INT_MASK1/INT_PEND1 registers. The 8XC196MD interrupt mask and pending registers are shown below. Notice that the CAPCOM5, COMP4, and CAPCOM4 bits are reserved bits on the 8XC196MC. The PI bit of the INT_PEND1 register will be set when a Waveform Generator or Compare Module 5 event occurs and the corresponding bit in the PI_MASK register is set. The PI interrupt vector can be taken when the PI bit in the INT_MASK1 register is set. The 8XC196MC User's Manual should be referenced for details about the interrupts.

INT_MASK1 (0031H) and INT_PEND1 (0012H)

7	6	5	4	3	2	1	0
RSV	EXTINT	PI	CAPCOM5*	COMP4*	CAPCOM4*	COMP3	CAPCOM3

RSV = RESERVED BIT. MUST WRITE AS 0
* = THIS BIT RESERVED ON 8XC196MC.

Figure 3. Interrupt Mask and Status Registers

PTSSRV and PTSSEL Register

Similarly, there are differences between 8XC196MC and 8XC196MD PTS registers. The 8XC196MD PTS registers are shown below. Notice the CAPCOM5, COMP4, and CAPCOM4 bits are reserved bits on the 8XC196MC. The PI bit in the PTSSRV will be set when a Waveform Generator or Compare Module 5 end of PTS interrupt occurs and the corresponding bit in the PI_MASK register is set. The PI PTS vector can be used when the PI bit in the PTSSEL register is set. The 8XC196MC User's Manual should be referenced for details about the PTS.

PTSSEL (0004H) and PTSSRV (0006H)

15	14	13	12	11	10	9	8
RSV	EXTINT	PI	CAPCOM5*	COMP4*	CAPCOM4*	COMP3	CAPCOM3

7	6	5	4	3	2	1	0
COMP2	CAPCOM2	COMP1	CAPCOM1	COMP0	CAPCOM0	AD_DONE	TOVF

RSV = RESERVED BIT. MUST WRITE AS 0
* = THIS BIT RESERVED ON 8XC196MC.

Figure 4. PTS Select and Service Registers

PI_MASK and PI_PEND Registers

The PI_MASK/PI_PEND registers contain the bits for the Compare Module 5 (COMP5) Waveform Generator (WG), Timer 1 Overflow (TFI), and Timer 2 Overflow (TF2) mask/status flag. The diagram below shows the registers. Notice that the COMP5 bit is a reserved bit on the 8XC196MC. The 8XC196MC User's Manual should be referenced for details about the Waveform Generator, Compare Modules, and Timers.

PI_MASK (1FBEH) and PI_PEND (1FBCH, Read Only)

7	6	5	4	3	2	1	0
RSV	COMP5*	RSV	WG	RSV	TF2	RSV	TF1

RSV = RESERVED BIT. MUST WRITE AS 0, READ AS 1.
* = THIS BIT RESERVED ON 8XC196MC.

Figure 5. Peripheral Interrupt Mask and Status Registers

The PI bit in the INT_PEND1 register is set if a Waveform Generator event or Compare Module 5 event occurs and the corresponding PI_MASK bit is set. For either of these events to cause an interrupt, the PI bit in the INT_MASK1 register and the corresponding event bit in the PI_MASK register must be set.

Similarly, the TOVF bit in the INT_PEND register is set if Timer 1 or Timer 2 overflow and the corresponding bit in the PI_MASK register is set. For either of these two events to cause an interrupt, the TOVF bit in the INT_MASK register and the corresponding event bit in the PI_MASK must be set.

Upon a PI and/or a TOVF interrupt, it may be necessary to check if the Compare Module 5, the Waveform Generator, Timer 1, or Timer 2 event caused the interrupt. The PI_PEND will give this information. However, it should be noted that reading the PI_PEND register will clear the register. So the individual bits in the PI_PEND register must be read by loading PI_PEND into another "shadow" register, then checking the "shadow" register to see what event occurred.

Table 3. Interrupt Sources, Vectors and Priorities

		Interrupt Service			PTS Service		
Interrupt Source	**Symbol**	**Name**	**Vector**	**Priority**	**Name**	**Vector**	**Priority**
Capture/Compare5	CAPCOMP5	INT12	2038H	12	PTS12	2058H	27
Compare4	COMP4	INT11	2036H	11	PTS11	2056H	26
Capture/Compare4	CAPCOMP4	INT10	2034H	10	PTS10	2054H	25

Interrupt and PTS Vectors

The 8XC196MD has three new interrupt and PTS vectors which are Capture/Compare5, Compare 4, and Capture/Compare4. Table 3 shows these interrupt vectors and priorities. These are shown as reserved vectors in the 8XC196MC User's Manual.

Frequency Generator

The Frequency Generator (FG) Peripheral which was not available on the 8XC196MC device, is available on the 8XC196MD device. The FG outputs a programmable-frequency 50% duty cycle waveform on the FREQOUT pin (P7.7). There are two 8-bit registers which control the FG peripheral:

— Frequency Generator Control Register (FG_CON) at 1FB8h

— Frequency Generator Period Count Register (FG_COUNT) at 1FBAh.

The FG_CON can be read or written. This register is loaded with a value which determines the number of counts necessary for toggling the output. The following equation should be used to calculate the FG_CON value:

$$\text{FG\_CON value} = \frac{F_{XTAL}}{16 * (\text{FG Frequency})} - 1$$

where FG Frequency is from 4 kHz to 1 MHz.

The FG_COUNT is loaded with the FG_CON register value. The FG_COUNT register is decremented every eighth state time. When it reaches 00h, the FG_COUNT register will send a signal to toggle the output pin and reload the FG_COUNT register with the value in the FG_CON register. The FG_COUNT can only be read, not written.

The FREQOUT pin (P7.7) must be configured for a special function to use it for the Frequency Generator feature.

Port 7

Port 7 is an additional bidirectional port that was not available on the 8XC196MC device. Port 7 can be used as I/O or some of the pins have special functions. The pins are listed below followed by their special functions.

Table 4. Port 7 Special Function Pins

Pin	Special Function
P7.0	CAPCOMP4
P7.1	CAPCOMP5
P7.2	CAPCOMP4
P7.3	CAPCOMP5
P7.4	
P7.5	
P7.6	
P7.7	FREQOUT

The special functions of the pins are selected in the Port 7 SFRs. The Port 2 I/O Port section of the 8XC196MC User's Manual can be referenced when setting up the Port 7 SFRs. Port 7 SFRs are located in the following locations:

Table 5. Port 7 Special Function Registers

SFR	Address
P7_MODE	1FD1h
P7_DIR	1FD3h
P7_REG	1FD5h
P7_PIN	1FD7h

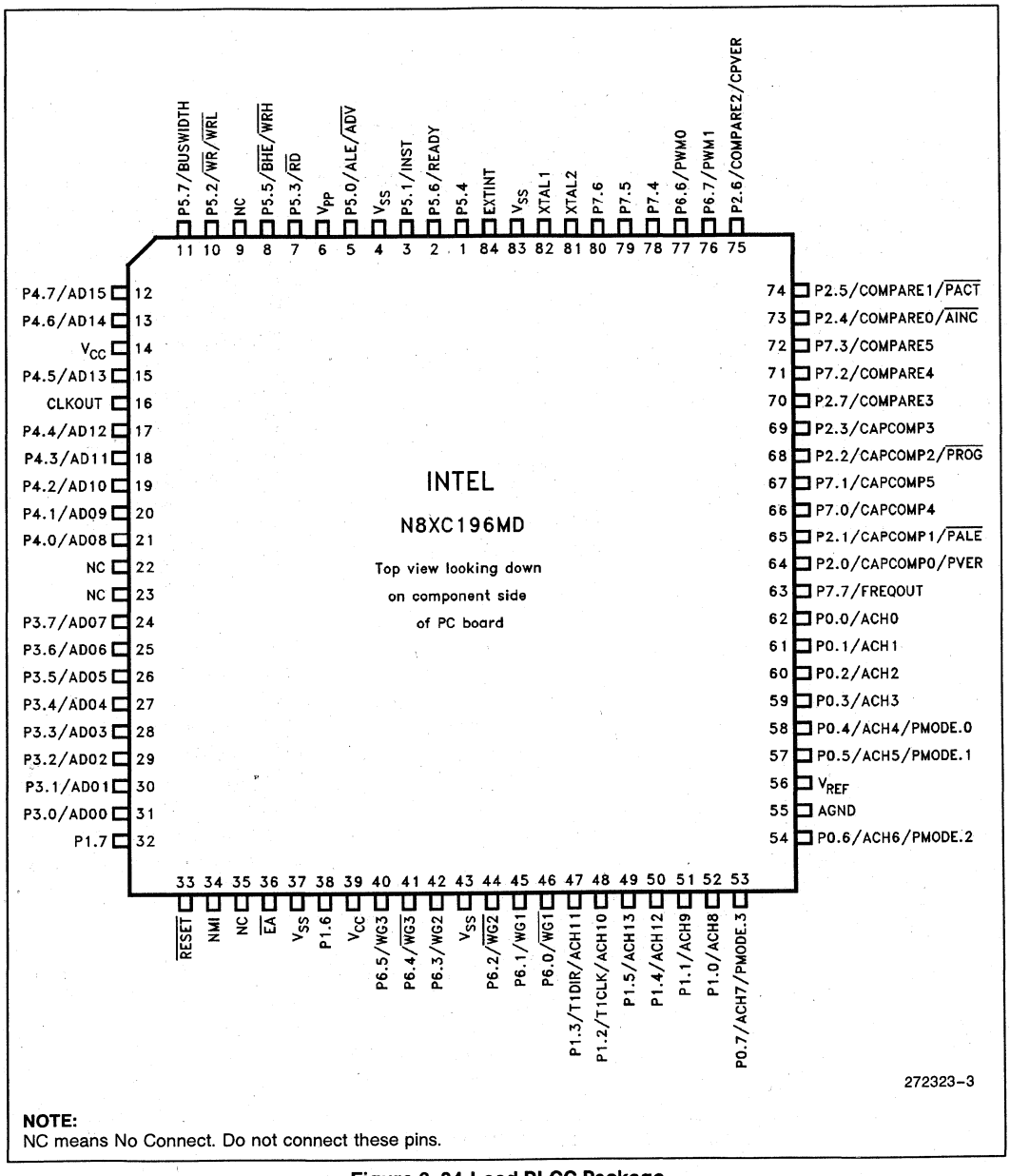
Port 1

There are three additional Port 1 input pins (P1.5–P1.7) that were not available on the 8XC196MC. These pins are listed below followed by their function:

Table 6. New 8XC196MD Port 1 Pins

Pin	Description
P1.5	Digital or Analog Input
P1.6	Digital Input
P1.7	Digital Input

NOTE:
P1.5 was a V_{SS} pin on the 8XC196MC device. If P1.5 and P1.6 are not being used these pins can remain connected to V_{SS}.



NOTE:
NC means No Connect. Do not connect these pins.

Figure 6. 84-Lead PLCC Package

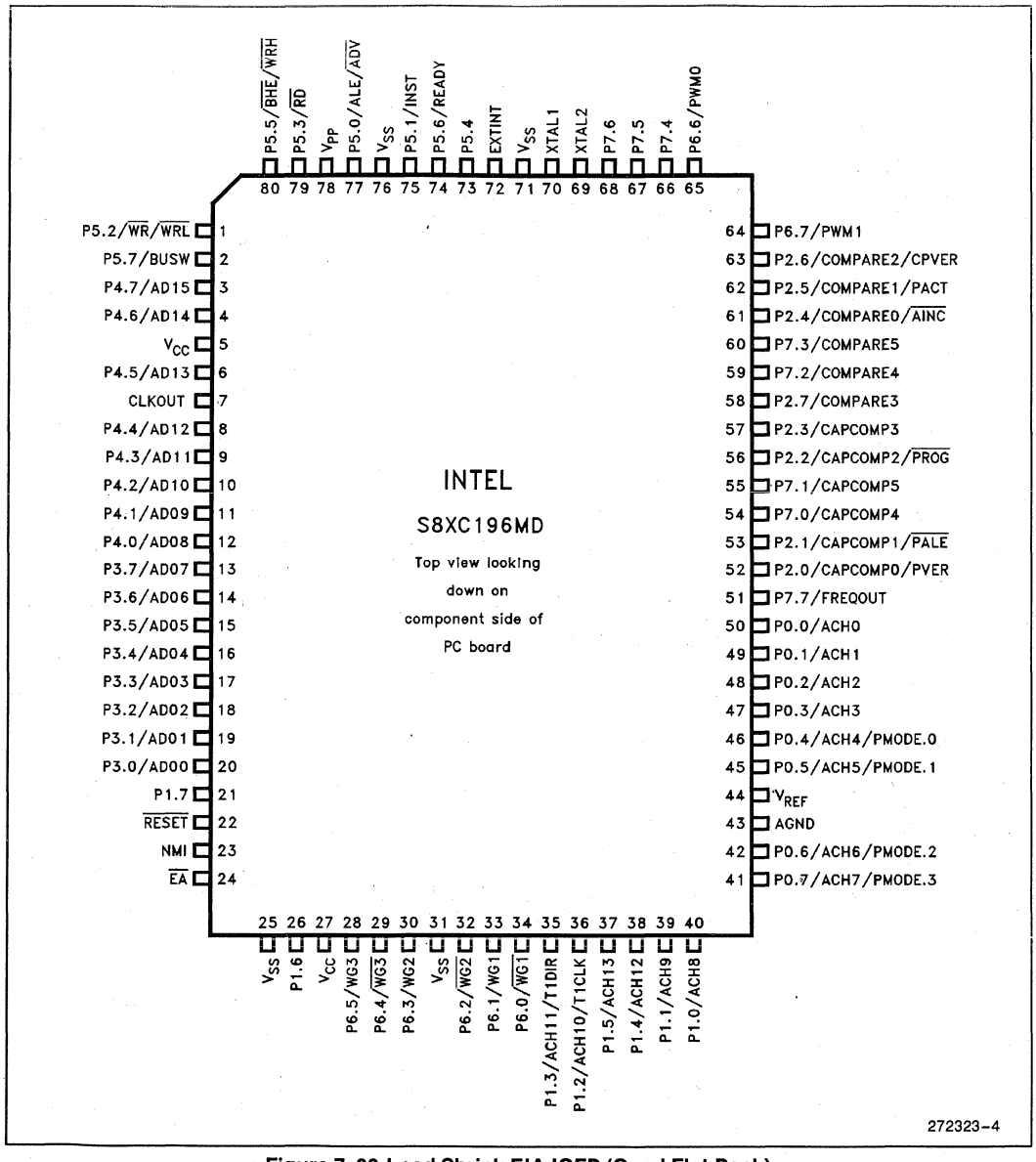


Figure 7. 80-Lead Shrink EIAJQFP (Quad Flat Pack)

PIN DESCRIPTIONS (Alphabetically Ordered)

Symbol	Function
ACH0–ACH13 (P0.0–P0.7, P1.0–P1.5)	Analog inputs to the on-chip A/D converter. ACH0–7 share the input pins with P0.0–7 and ACH8–13 share pins with P1.0–5. If the A/D is not used, the port pins can be used as standard input ports.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
ALE/$\overline{ADV}$(P5.0)	Address Latch Enable or Address Valid output, as selected by CCR. Both options allow a latch to demultiplex the address/data bus on the signal's falling edge. When the pin is $\overline{ADV}$, it goes inactive (high) at the end of the bus cycle. ALE/$\overline{ADV}$ is active only during external memory accesses. Can be used as standard I/O when not used as ALE/ADV.
$\overline{BHE}$/$\overline{WRH}$ (P5.5)	Byte High Enable or Write High output, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.
BUSWIDTH (P5.7)	Input for bus width selection. If CCR bits 1 and 2 = 1, this pin dynamically controls the bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If it is high, a 16-bit cycle occurs. This pin can be used as standard I/O when not used as BUSWIDTH.
CAPCOMP0–CAPCOMP5 (P2.0–P2.3, P7.0–P7.1)	The EPA Capture/Compare pins. CAPCOMP0–3 share the pins with P2.0–P2.3. CAPCOMP4–5 share the pins with P7.0–P7.1. If not used for the EPA, they can be configured as standard I/O pins.
CLKOUT	Output of the internal clock generator. The frequency is ½ of the oscillator frequency. It has a 50% duty cycle.
COMPARE0–COMPARE5 (P2.4–P2.7, P7.2–P7.3)	The EPA Compare pins. COMPARE0–3 share the pins with P2.4–P2.7. COMPARE4–5 share the pins with P7.2–P7.3. If not used for the EPA, they can be configured as standard I/O pins.
$\overline{EA}$	External Access enable pin. $\overline{EA}$ = 0 causes all memory accesses to be external to the chip. $\overline{EA}$ = 1 causes memory accesses from location 2000H to 5FFFH to be from the on-chip OTPROM/ROM. $\overline{EA}$ = 12.5V causes execution to begin in the programming mode. $\overline{EA}$ is latched at reset.
EXTINT	A programmable input on this pin causes a maskable interrupt vector through memory location 203CH. The input may be selected to be a positive/negative edge or a high/low level using WG_PROTECT (1FCEH).
FREQOUT	Programmable frequency output pin. The frequency can vary from 4 KHz to 1 MHz (16 MHz input clock). It has a 50% duty cycle. Pin may be configured as standard I/O if FREQOUT is not used.
INST (P5.1)	INST is high during the instruction fetch from the external memory and throughout the bus cycle. It is low otherwise. This pin can be configured as standard I/O if not used as INST.
NMI	A positive transition on this pin causes a non-maskable interrupt which vectors to memory location 203EH. If not used, it should be tied to V_{SS}. May be used by Intel Evaluation boards.
PORT0	8-bit high impedance input-only port. Also used as A/D converter inputs. Port0 pins should not be left floating. These pins also used to select programming modes in the OTPROM devices.
PORT1	8-bit high impedance input-only port. P1.0–P1.5 are also used as A/D converter inputs. In addition, P1.2 and P1.3 can be used as Timer 1 clock input and direction select respectively. P1.6–P1.7 can be used as input-only pins.

PIN DESCRIPTIONS (Alphabetically Ordered) (Continued)

Symbol	Function
PORT2	8-bit bidirectional I/O port. All of the Port2 pins are shared with the EPA I/O pins (CAPCOMP0–3 and COMPARE0–3).
PORT3 PORT4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which uses strong internal pullups.
PORT5	8-bit bidirectional I/O port. 7 of the pins are shared with bus control signals ($\overline{ALE}$, INST, $\overline{WR}$, $\overline{RD}$, $\overline{BHE}$, READY, BUSWIDTH). Can be used as standard I/O.
PORT6	8-bit output port. P6.6 and P6.7 output PWM, the others are used as the Wave Form Generator outputs. Can be used as standard output ports.
PORT7	8-bit bidirectional I/O port. P7.0–P7.3 can be used as EPA I/O pins (CAPCOMP4–5 and COMPARE4–5). P7.7 can be used as FREQOUT output pin. P7.4–P7.6 are standard I/O pins.
PWM0, PWM1 (P6.6, P6.7)	Programmable duty cycle, Programmable frequency Pulse Width Modulator pins. The duty cycle has a resolution of 256 steps, and the frequency can vary from 122 Hz to 31 KHz (16 MHz input clock). Pins may be configured as standard output if PWM is not used.
$\overline{RD}$ (P5.3)	Read signal output to external memory. $\overline{RD}$ is low only during external memory reads. Can be used as standard I/O when not used as $\overline{RD}$.
READY (P5.6)	Ready input to lengthen external memory cycles. If READY = 0, the memory controller inserts wait states until the next positive transition of CLKOUT occurs with READY = 1. Can be used as standard I/O when not used as READY.
$\overline{RESET}$	Reset input to and open-drain output from the chip. Held low for at least 16 state times to reset the chip. Input high for normal operation. $\overline{RESET}$ has an Ohmic internal pullup resistor.
T1CLK (P1.2)	Timer 1 Clock input. This pin has two other alternate functions: ACH10 and P1.2.
T1DIR (P1.3)	Timer 1 Direction input. This pin has two other alternate functions: ACH11 and P1.3.
V_{PP}	The programming voltage is applied to this pin. It is also the timing pin for the return from Power Down circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If the Power Down feature is not used, connect the pin to V_{CC}.
WG1–WG3/$\overline{WG1}$–$\overline{WG3}$ (P6.0–P6.5)	3 phase output signals and their complements used in motor control applications. The pins can also be configured as standard output pins.
$\overline{WR}$/$\overline{WRL}$ (P5.2)	Write and Write Low output to external memory. $\overline{WR}$ will go low every external write. $\overline{WRL}$ will go low only for external writes to an even byte. Can be used as standard I/O when not used as $\overline{WR}$/$\overline{WRL}$.
XTAL1	Input of the oscillator inverter and the internal clock generator. This pin should be used when using an external clock source.
XTAL2	Output of the oscillator inverter.
PMODE (P0.4–7)	Determines the EPROM programming mode.
$\overline{PACT}$ (P2.5)	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.

PIN DESCRIPTIONS (Alphabetically Ordered) (Continued)

Symbol	Function
$\overline{\text{PALE}}$ (P2.1)	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$ (P2.2)	A falling edge in Slave Programming Mode begins programming. A rising edge ends programming.
PVER (P2.0)	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER (P2.6)	Cumulative Program Verification. Pin is high if all locations since entering a programming mode have programmed correctly.
$\overline{\text{AINC}}$ (P2.4)	Auto Increment. Active low input enables the auto increment mode. Auto increment will allow reading or writing of sequential EPROM locations without address transactions across the PBUS for each read or write.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage from $\overline{EA}$ or V_{PP}
to V_{SS} or ANGND ..... −0.5V to +13.00V
Voltage on Any Other Pin
to V_{SS} or ANGND ..... −0.5V to +7.0V(1)
Power Dissipation ..... 1.5W(2)

NOTES:
1. This includes V_{PP} and $\overline{EA}$ on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature Under Bias	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V
F_{OSC}	Oscillator Frequency	8	16	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential. Also V_{SS} and V_{SS1} must be at the same potential.

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage Port 2, 5, and 7, P6.6, P6.7, CLKOUT		0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage on Port 3/4		1.0	V	I_{OL} = 15 mA
V_{OL2}	Output Low Voltage on Port 6.0–6.5		0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5		V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
$V_{th+} - V_{th-}$	Hysteresis Voltage Width on $\overline{RESET}$	0.2		V	Typical

DC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Leakage Current on All Input Only Pins			±10	μA	$0V < V_{IN} < V_{CC}-0.3V$ (in RESET)
I_{LI1}	Input Leakage Current on Port0 and Port1			±3	μA	$0V < V_{IN} < V_{REF}$
I_{IL}	Input Low Current on BD Ports (Note 1)			−70	μA	$V_{IN} = 0.3\ V_{CC}$
I_{IL1}	Input Low Current on P5.4 and P2.6 during Reset (Note 3)			−10	mA	$0.2\ V_{CC}$
I_{OH}	Output High Current on P5.4 and P2.6 during Reset (Note 4)	−2			mA	$0.7\ V_{CC}$
I_{CC}	Active Mode Current in Reset		50	70	mA	XTAL1 = 16 MHz, $V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{REF}	A/D Conversion Reference Current		2	5	mA	
I_{IDL}	Idle Mode Current		15	30	mA	
I_{PD}	Power-Down Mode Current		5	50	μA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	$\overline{\text{RESET}}$ Pin Pullup Resistor	6k		65k	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:

1. BD (Bidirectional ports) include:
   - P2.0–P2.7, except P2.6
   - P3.0–P3.7
   - P4.0–P4.7
   - P5.0–P5.3
   - P5.5–P5.7
   - P7.0–P7.7
2. During normal (non-transient) conditions, the following total current limits apply:
   - P6.0–P6.5: I_{OL}: 40 mA I_{OH}: 28 mA
   - P3: I_{OL}: 90 mA I_{OH}: 42 mA
   - P4: I_{OL}: 90 mA I_{OH}: 42 mA
   - P5, CLKOUT: I_{OL}: 35 mA I_{OH}: 35 mA
   - P2, P6.6, P6.7, P7: I_{OL}: 63 mA I_{OH}: 63 mA
3. Maximum current that must be sunk by external device to ensure test mode entry.
4. Do not exceed minimum current or device may enter test mode.

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H — High
L — Low
V — Valid
X — No Longer Valid
Z — Floating

Signals:

A — Address
B — $\overline{BHE}$
C — CLKOUT
D — DATA
G — Buswidth
H — $\overline{HOLD}$
HA — $\overline{HLDA}$
L — ALE/$\overline{ADV}$
BR — $\overline{BREQ}$
R — $\overline{RD}$
W — $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X — XTAL1
Y — READY
Q — Data Out

AC ELECTRICAL CHARACTERISTICS (Over Specified Operating Conditions)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The system must meet the following specifications to work with the 87C196MD:

Symbol	Parameter	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1	8	16	MHz	3
T_{OSC}	$1/F_{XTAL}$	62.5	125	ns	
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 70$	ns	4
T_{YLYH}	Not READY Time	No Upper Limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	1
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	1
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns	4
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	2
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 22$	ns	2
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add $2T_{OSC}$ * N, where N = number of wait states.
3. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
4. These timings are included for compatibility with older −90 and BH products. They should not be used for newer high-speed designs.

AC ELECTRICAL CHARACTERISTICS (Continued)

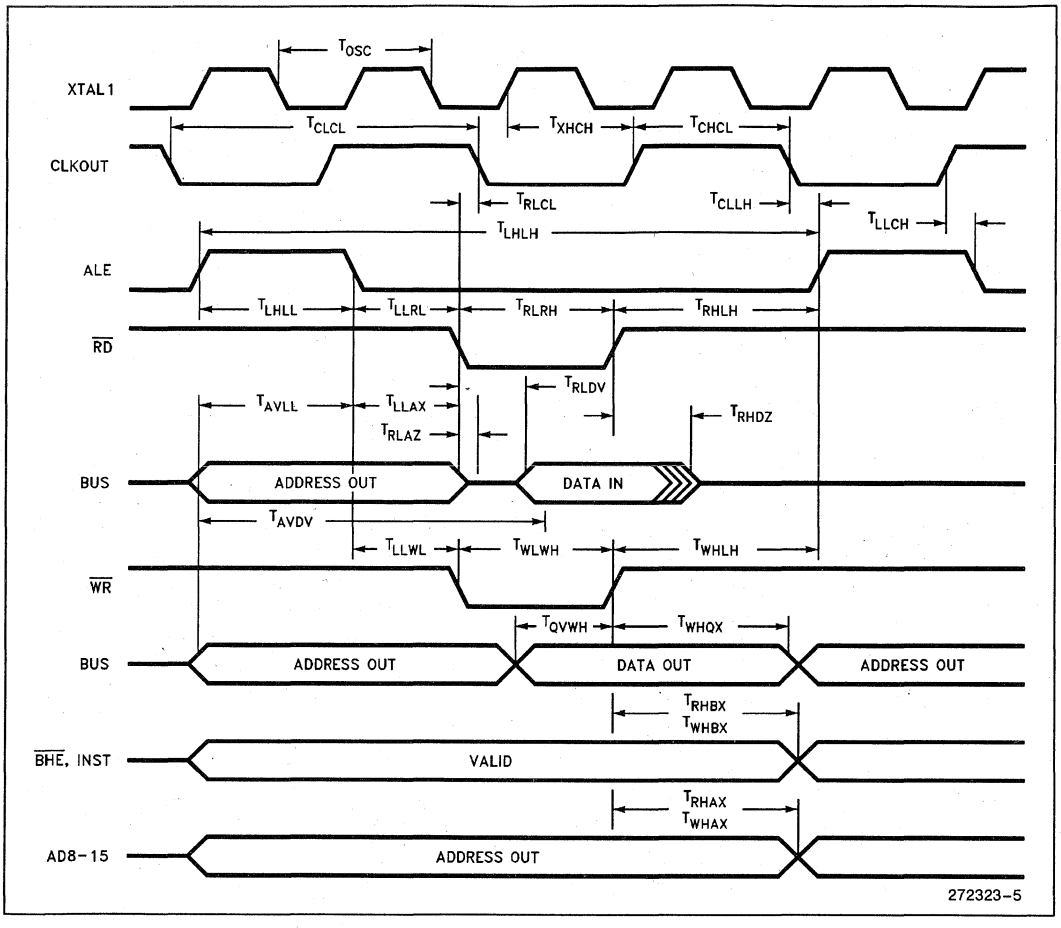
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

The 87C196MD will meet the following timing specifications:

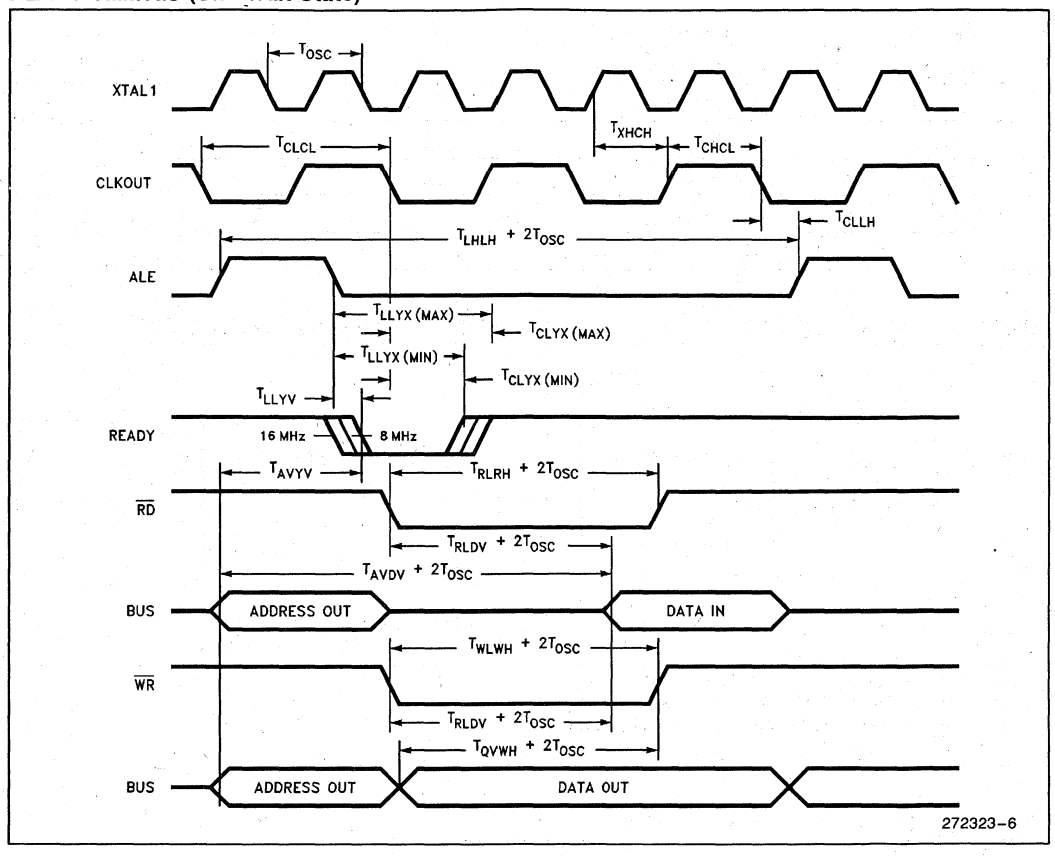
Symbol	Parameter	Min	Max	Units	Notes
T_{XHCH}	XTAL1 to CLKOUT High or Low	30	110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 15	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−20	15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	3
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15		ns	
T_{LLAX}	Address Hold after ALE Falling	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling	T_{OSC} − 30		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	3
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	1
T_{RLAZ}	$\overline{RD}$ Low to Address Float		5	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns	3
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 25		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	1
T_{WHBX}	$\overline{BHE}$, INST Hold after $\overline{WR}$ Rising	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising	T_{OSC} − 30		ns	2
T_{RHBX}	$\overline{BHE}$, INST Hold after $\overline{RD}$ Rising	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising	T_{OSC} − 30		ns	2

NOTES:
1. Assuming back to back cycles.
2. 8-bit bus only.
3. If wait states are used, add 2 T_{OSC}*N, where N = number of wait states.

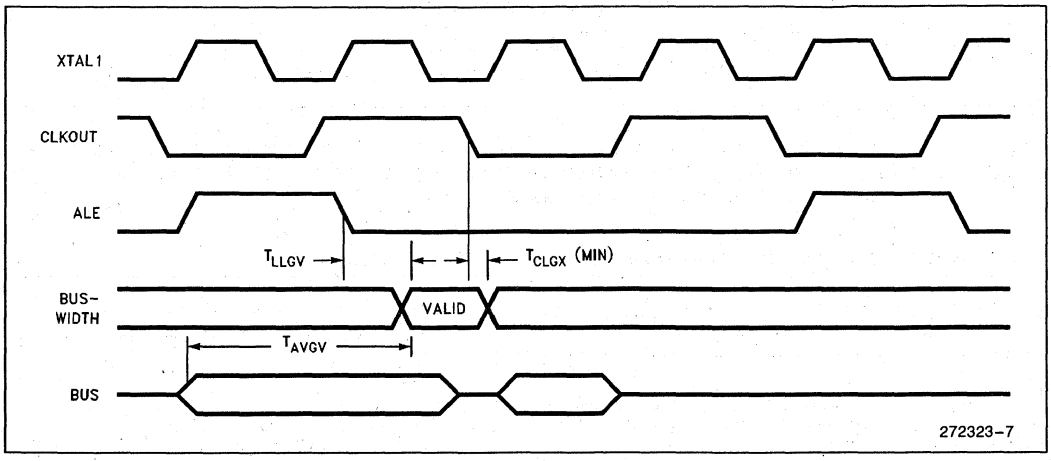
SYSTEM BUS TIMINGS



READY TIMINGS (One Wait State)



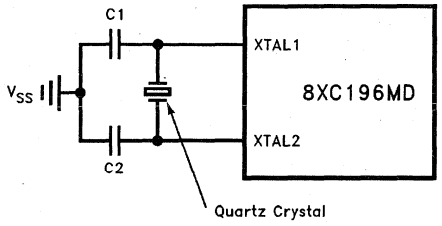
BUSWIDTH TIMINGS



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16.0	MHz
T_{XLXL}	Oscillator Period	62.5	125	ns
T_{XHXX}	High Time	22		ns
T_{XLXX}	Low Time	22		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

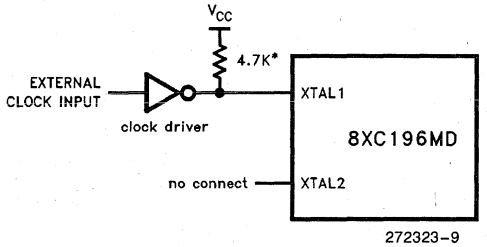
EXTERNAL CRYSTAL CONNECTIONS



272323-8

NOTE:
Keep oscillator components close to chip and use short, direct traces to XTAL1, XTAL2 and V_{SS}. When using crystals, C1 = 20 pF, C2 = 20 pF. When using ceramic resonators, consult manufacturer for recommended circuitry.

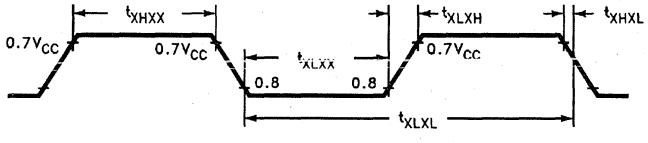
EXTERNAL CLOCK CONNECTIONS



272323-9

* Required if TTL driver used.
Not needed if CMOS driver is used.

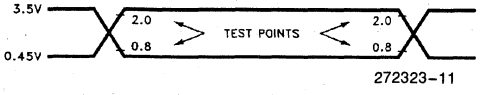
EXTERNAL CLOCK DRIVE WAVEFORMS



272323-10

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

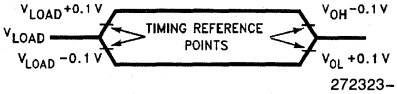
AC TESTING INPUT, OUTPUT WAVEFORMS



272323-11

AC Testing inputs are driven at 3.5V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT WAVEFORMS



272323-12

For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

A TO D CHARACTERISTICS

The sample and conversion time of the A/D converter in the 8-bit or 10-bit modes is programmed by loading a byte into the AD_TIME Special Function Register. This allows optimizing the A/D operation for specific applications. The AD_TIME register is functional for all possible values, but the accuracy of the A/D converter is only guaranteed for the times specificed in the operating conditions table.

The value loaded into AD_TIME bits 5, 6, 7 determines the sample time, T_{SAM}, and is calculated using the following formula:

$$SAM = \frac{(T_{SAM} \times F_{OSC}) - 2}{8}$$

T_{SAM} = Sample time, μs
F_{OSC} = Processor frequency, MHz
SAM = Value loaded into AD_TIME bits 5, 6, 7

SAM must be in the range 1 through 7.

The value loaded into AD_TIME bits 0–5 determines the conversion time, T_{CONV}, and is calculated using the following formula:

$$CONV = \frac{(T_{CONV} \times F_{OSC}) - 3}{2B} - 1$$

T_{CONV} = Conversion time, μs
F_{OSC} = Processor frequency, MHz
B = 8 for 8-bit conversion
B = 10 for 10-bit conversion
CONV = Value loaded into AD_TIME bits 0–5

CONV must be in the range 2 through 31.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the analog portion of the converter and input port pins. There is also an AD_TEST SFR that allows for conversion on ANGND and V_{REF} as well as adjusting the zero offset. The absolute error listed is WITHOUT doing any adjustments.

A/D CONVERTER SPECIFICATION

The specifications given assume adherence to the operating conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V and 16.0 MHz operating frequency. After a conversion is started, the device is placed in the IDLE mode until the conversion is complete.

10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	10.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		1024 10	1024 10	Levels Bits
Absolute Error		0	±4	LSBs
Full Scale Error	0.25 ±0.5			LSBs
Zero Offset Error	0.25 ±0.5			LSBs
Non-Linearity	1.0 ±2.0		±4	LSBs
Differential Non-Linearity		> −1	+2	LSBs
Channel-to-Channel Matching	±0.1	0	±1.0	LSBs
Repeatability	±0.25	0		LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		ANGND − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB", as used here has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

8-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.00	5.50	V(1)
T_{SAM}	Sample Time	1.0		μs(2)
T_{CONV}	Conversion Time	7.0	20.0	μs(2)
F_{OSC}	Oscillator Frequency	8.0	16.0	MHz

NOTES:
ANGND and V_{SS} should nominally be at the same potential.
1. V_{REF} must be within 0.5V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

8-BIT MODE A/D CHARACTERISTICS (Over the Above Operating Conditions)

Parameter	Typical(1)	Min	Max	Units*
Resolution		256 8	256 8	Level Bits
Absolute Error		0	±1	LSBs
Full Scale Error	±0.5			LSBs
Zero Offset Error	±0.5			LSBs
Non-Linearity		0	±1	LSBs
Differential Non-Linearity		>−1	+1	LSBs
Channel-to-Channel Matching		0	±1.0	LSBs
Repeatability	±0.25			LSBs
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/C LSB/C LSB/C
Off Isolation		−60		dB(2, 3)
Feedthrough	−60			dB(2)
V_{CC} Power Supply Rejection	−60			dB(2)
Input Series Resistance		750	2K	Ω(4)
Voltage on Analog Input Pin		V_{SS} − 0.5	V_{REF} + 0.5	V(5, 6)
Sampling Capacitor	3			pF
DC Input Leakage	±1	0	±3.0	μA

NOTES:
*An "LSB" as used here, has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).
1. These values are expected for most parts at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make is guaranteed.
4. Resistance from device pin, through internal MUX, to sample capacitor.
5. These values may be exceeded if the pin current is limited to ±2 mA.
6. Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
7. All conversions performed with processor in IDLE mode.

EPROM SPECIFICATIONS

OPERATING CONDITIONS DURING PROGRAMMING

Symbol	Description	Min	Max	Units
T_A	Ambient Temperature during Programming	20	30	°C
V_{CC}	Supply Voltage during Programming	4.5	5.5	V(1)
V_{REF}	Reference Supply Voltage during Programming	4.5	5.5	V(1)
V_{PP}	Programming Voltage	12.25	12.75	V(2)
V_{EA}	EA Pin Voltage	12.25	12.75	V(2)
F_{OSC}	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
T_{OSC}	Oscillator Frequency during Run-Time Programming	6.0	12.0	MHz

NOTES:
1. V_{CC} and V_{REF} should nominally be at the same voltage during programming.
2. V_{PP} and V_{EA} must never exceed the maximum specification, or the device may be damaged.
3. V_{SS} and ANGND should nominally be at the same potential (0V).
4. Load capacitance during Auto and Slave Mode programming = 150 pF.

AC EPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Parameter	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(1)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	PROG High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to PVER Valid		220	T_{OSC}

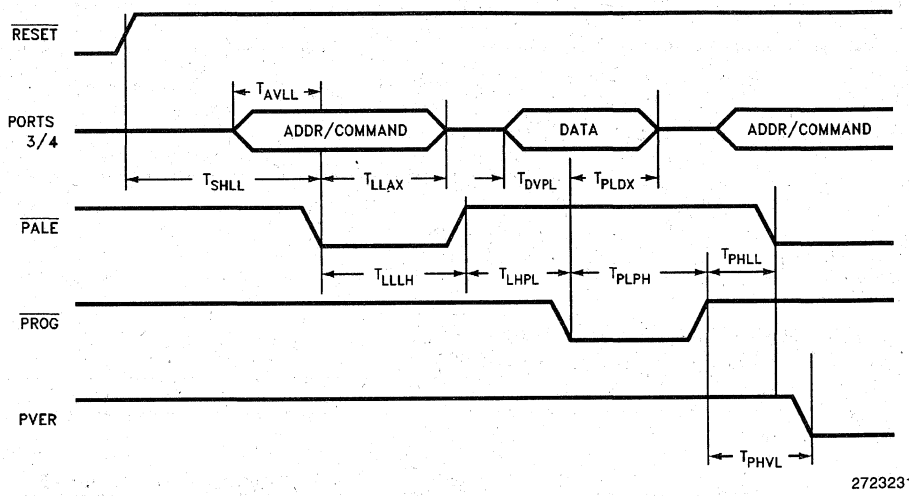
NOTE:
1. This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

DC EPROM PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

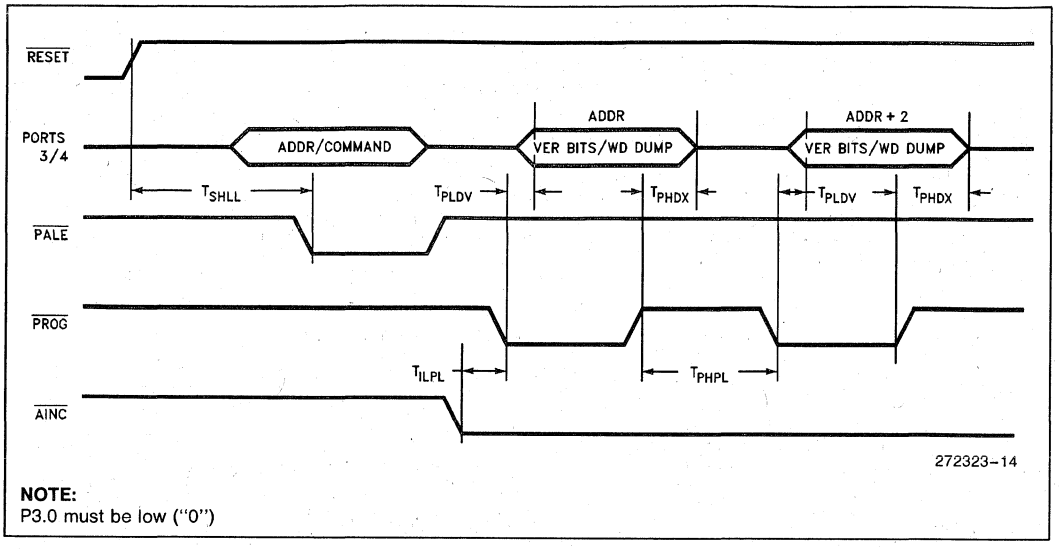
NOTE:
Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



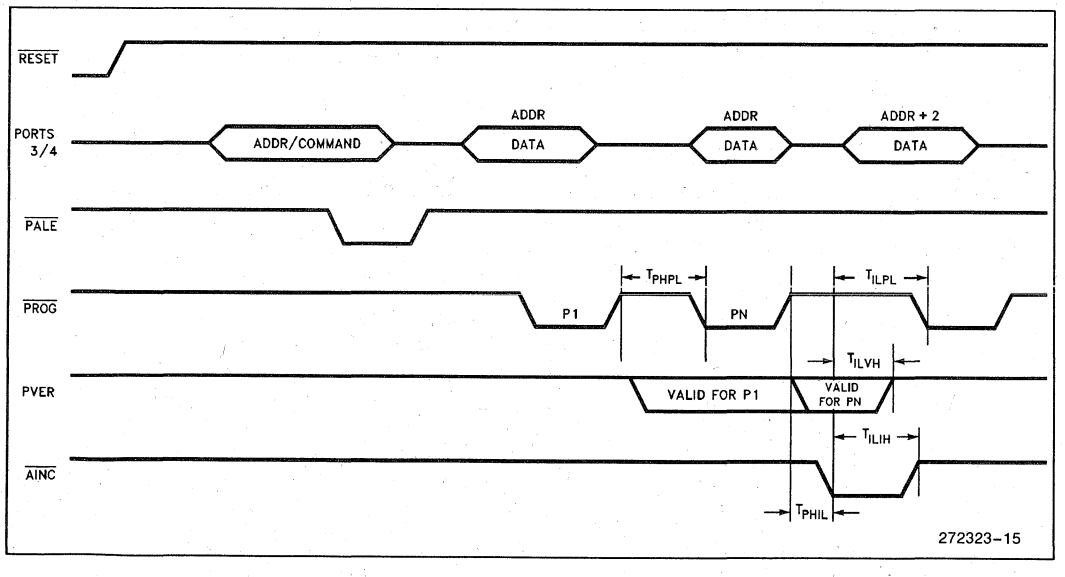
NOTE:
P3.0 must be high ("1")

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT



NOTE:
P3.0 must be low ("0")

SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT



87C196MD DESIGN CONSIDERATIONS

When an indirect shift during divide occurs the upper 3 bits of the shift count are not masked completely. If the shift count register has the value 32 * n where n = 1, 3, 5 or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

8XC196MC to 8XC196MD Design Considerations

8XC196MC and 8XC196MD are pin compatible. However, there were several pins that were not connected (NC) on the 8XC196MC that are I/O pins on the 8XC196MD. Port 7 is a bidirectional port added to the 8XC196MD. Port 1 has one additional analog or digital input that was connected to V_{SS} on the 8XC196MC. Port 1 also has two additional digital inputs. See 8XC196MC and 8XC196MD Differences Section of this data sheet.

DATA SHEET REVISION HISTORY

This is the initial data sheet (272323-001). It is valid for devices with a "B" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

PRELIMINARY

8XC196MH INDUSTRIAL MOTOR CONTROL CHMOS MICROCONTROLLER

- High Performance CHMOS 16-bit CPU
- 16 MHz Operating Frequency
- 32 Kbytes of On-chip OTPROM/ROM
- 744 Bytes of On-chip Register RAM
- Register-to-register Architecture
- 16 Prioritized Interrupt Sources
- Peripheral Transaction Server (PTS) with 15 Prioritized Sources
- Up to 52 I/O Lines
- 3-phase Complementary Waveform Generator
- 8-channel 8- or 10-bit A/D with Sample and Hold
- 2-channel UART
- Event Processor Array (EPA) with 2 High-speed Capture/Compare Modules and 4 High-speed Compare-only Modules
- Two Programmable 16-bit Timers with Quadrature Counting Inputs
- Two Pulse-width Modulator (PWM) Outputs with High Drive Capability
- Flexible 8- or 16-bit External Bus
- 1.75 µs 16 × 16 Multiply
- 3 µs 32/16 Divide
- Extended Temperature Available
- Idle and Powerdown Modes
- Watchdog Timer

The 8XC196MH is a member of Intel's family of 16-bit MCS® 96 microcontrollers. It is designed primarily to control three-phase AC induction and DC brushless motors. It features an enhanced three-phase waveform generator specifically designed for use in "inverter" motor-control applications. This peripheral provides pulse-width modulation and three-phase sine wave generation with minimal CPU intervention. It generates three complementary non-overlapping PWM pulses with resolutions of 0.125 µs (edge triggered) or 0.250 µs (centered).

The 8XC196MH has two dedicated serial port peripherals, allowing less software overhead. The watchdog timer can be programmed with one of four time options.

The 8XC196MH is available without internal memory (80C196MH), with 32 Kbytes of factory programmed OTPROM* (83C196MH), or with 32 Kbytes of user programmable OTPROM* (87C196MH). It is available in three packages: 84-lead PLCC, 80-lead Shrink EIAJ/QFP, and 64-lead SDIP. The 64-lead package does not contain pins for the P5.1/INST and P6.7/PWM1 signals.

Operational characteristics are guaranteed over the temperature range of – 40°C to + 85°C.

*One-Time Programmable Read-Only Memory (OTPROM) is similar to EPROM but comes in an unwindowed package and cannot be erased. It is user programmable.

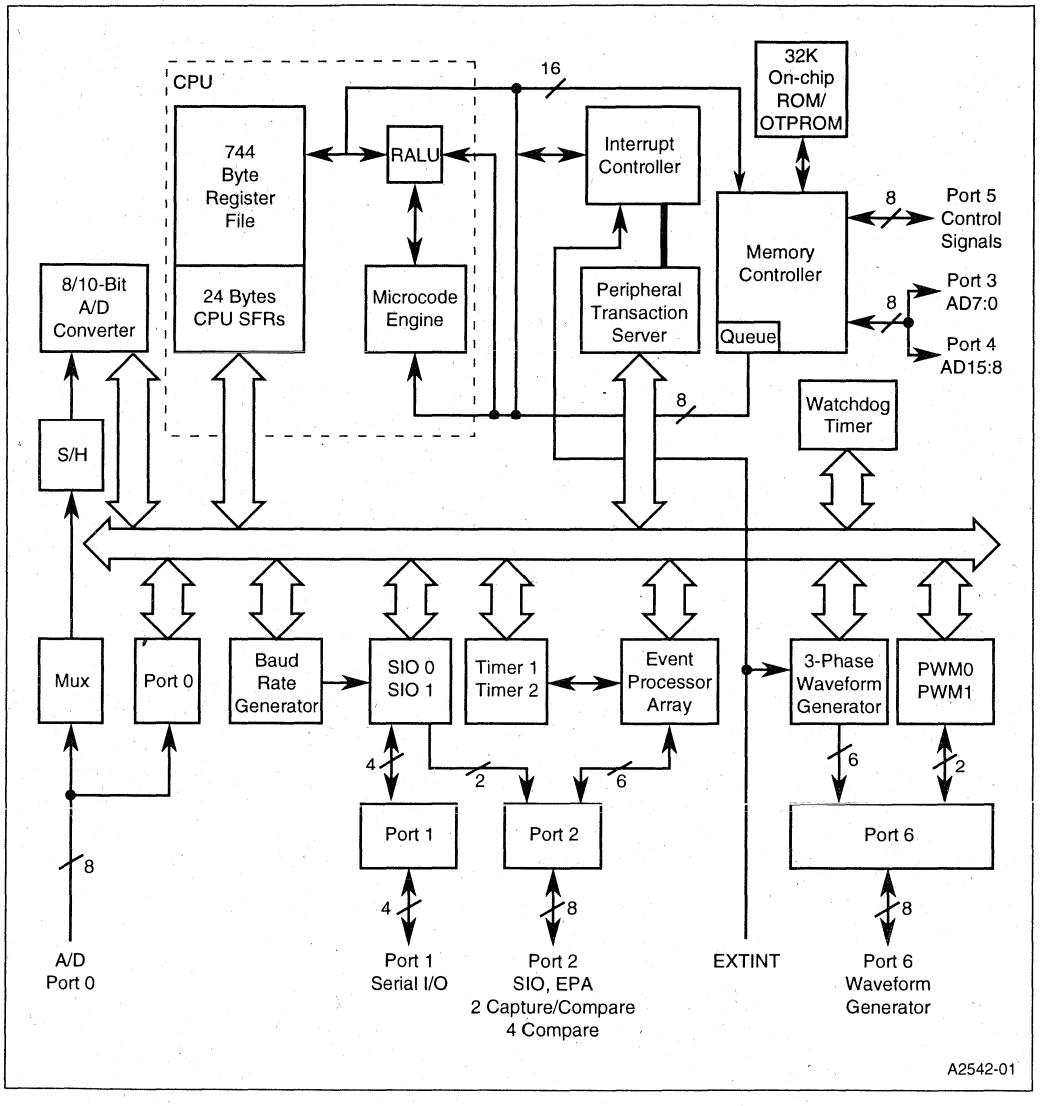


Figure 1. 8XC196MH Block Diagram

PROCESS INFORMATION

This device is manufactured on PX29.5, a CHMOS IV process. Additional process and reliability information is available in Intel's *Components Quality and Reliability* Handbook (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values will change depending on operating conditions and the application. The Intel *Packaging* Handbook (order number 240800) describes Intel's thermal impedance test methodology.

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
84-lead PLCC	33°C/W	11°C/W
80-lead QFP	56°C/W	12°C/W
64-lead SDIP	56°C/W	N/A

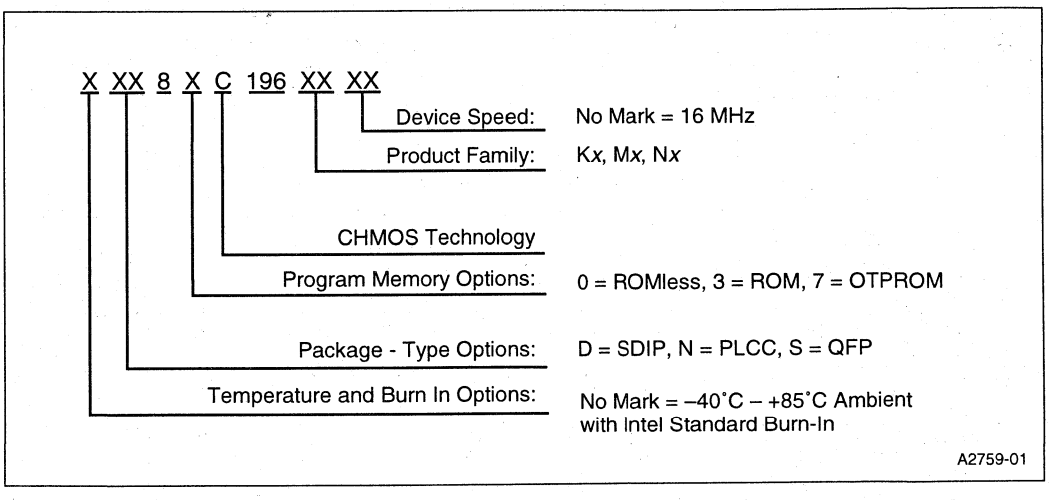


Figure 2. The 8XC196MH Family Nomenclature

Table 2. 8XC196MH Memory Map

Address (1)	Description	Notes
0FFFFH 0A000H	External Memory	
09FFFH 02080H	Internal ROM/OTPROM or External Memory	
0207FH 0205EH	Reserved	1, 2
0205DH 02040H	PTS Vectors	
0203FH 02030H	Interrupt Vectors (upper)	
0202FH 02020H	ROM/OTPROM Security Key	
0201FH 0201CH	Reserved	1, 2
0201BH	Reserved (must contain 20H)	
0201AH	CCB1	
02019H	Reserved (must contain 20H)	
02018H	CCB0	
02017H 02014H	Reserved	
02013H 02000H	Interrupt Vectors (lower)	
01FFFH 01F00H	Internal SFRs	1
1EFFH 300H	External Memory	
2FFH 18H	Register RAM	3
17H 00H	CPU SFRs	1

NOTES:
1. Unless otherwise noted, write 0FFH to reserved memory locations and write 0 to reserved SFR bits.
2. **WARNING:** The contents and/or function of reserved locations may change with future revisions of the device.
3. Code executed in locations 0000H to 02FFH will be forced external.

Table 3. Signals Arranged by Functional Categories

Address & Data
AD15:0

Bus Control & Status
ALE/ADV#
BHE#/WRH#
BUSWIDTH
INST
READY
RD#
WR#/WRL#

Power & Ground
ANGND
V_{CC}
V_{PP}
V_{REF}
V_{SS}

Programming Control
AINC#
CPVER
PACT#
PALE#
PBUS15:0
PMODE.3:0
PROG#
PVER

Processor Control
EA#
EXTINT
NMI
ONCE#
RESET#
XTAL1
XTAL2

Input/Output
P0.0/ACH0
P0.1/ACH1
P0.2/ACH2
P0.3/ACH3
P0.4/ACH4
P0.5/ACH5
P0.6/ACH6/T1CLK
P0.7/ACH7/T1DIR
P1.0/TXD0
P1.1/RXD0
P1.2/TXD1
P1.3/RXD1
P2.0/EPA0
P2.1/SCLK0#/BCLK0
P2.2/EPA1
P2.3/COMP3
P2.4/COMP0

Input/Output (Cont'd)
P2.5/COMP1
P2.6/COMP2
P2.7/SCLK1#/BCLK1
P3.7:0
P4.7:0
P5.7:0
P6.0/WG1#
P6.1/WG1
P6.2/WG2#
P6.3/WG2
P6.4/WG3#
P6.5/WG3
P6.6/PWM0
P6.7/PWM1

NOTE: The following signals are not available in the 64-pin package: P5.1, P6.7, INST, and PWM1.

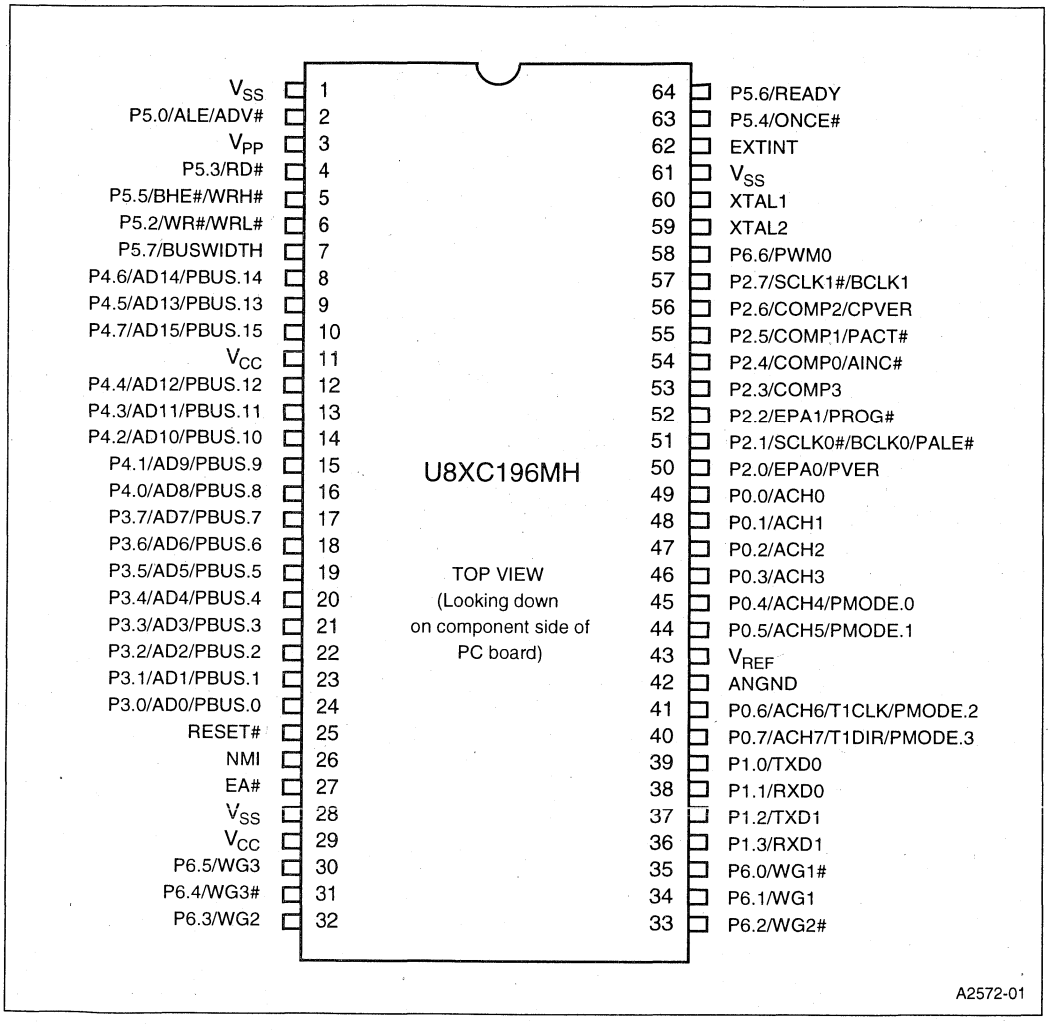


Figure 3. 8XC196MH 64-lead Shrink DIP (SDIP) Package

Table 4. 64-lead Shrink DIP (SDIP) Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	17	P3.7/AD7 /PBUS.7	33	P6.2/WG2#	49	P0.0/ACH0
2	P5.0/ALE/ADV#	18	P3.6/AD6 /PBUS.6	34	P6.1/WG1	50	P2.0/EPA0/PVER
3	V_{PP}	19	P3.5/AD5 /PBUS.5	35	P6.0/WG1#	51	P2.1/SCLK0# /BCLK0/PALE#
4	P5.3/RD#	20	P3.4/AD4 /PBUS.4	36	P1.3/RXD1	52	P2.2/EPA1 /PROG#
5	P5.5/BHE#/WRH#	21	P3.3/AD3 /PBUS.3	37	P1.2/TXD1	53	P2.3/COMP3
6	P5.2/WR#/WRL#	22	P3.2/AD2 /PBUS.2	38	P1.1/RXD0	54	P2.4/COMP0 /AINC#
7	P5.7/BUSWIDTH	23	P3.1/AD1 /PBUS.1	39	P1.0/TXD0	55	P2.5/COMP1 /PACT#
8	P4.6/AD14 /PBUS.14	24	P3.0/AD0 /PBUS.0	40	P0.7/ACH7/T1DIR /PMODE.3	56	P2.6/COMP2 /CPVER
9	P4.5/AD13 /PBUS.13	25	RESET#	41	P0.6/ACH6 /T1CLK/PMODE.2	57	P2.7/SCLK1# /BCLK1
10	P4.7/AD15 /PBUS.15	26	NMI	42	ANGND	58	P6.6/PWM0
11	V_{CC}	27	EA#	43	V_{REF}	59	XTAL2
12	P4.4/AD12 /PBUS.12	28	V_{SS}	44	P0.5/ACH5 /PMODE.1	60	XTAL1
13	P4.3/AD11 /PBUS.11	29	V_{CC}	45	P0.4/ACH4 /PMODE.0	61	V_{SS}
14	P4.2/AD10 /PBUS.10	30	P6.5/WG3	46	P0.3/ACH3	62	EXTINT
15	P4.1/AD9/PBUS.9	31	P6.4/WG3#	47	P0.2/ACH2	63	P5.4/ONCE#
16	P4.0/AD8/PBUS.8	32	P6.3/WG2	48	P0.1/ACH1	64	P5.6/READY

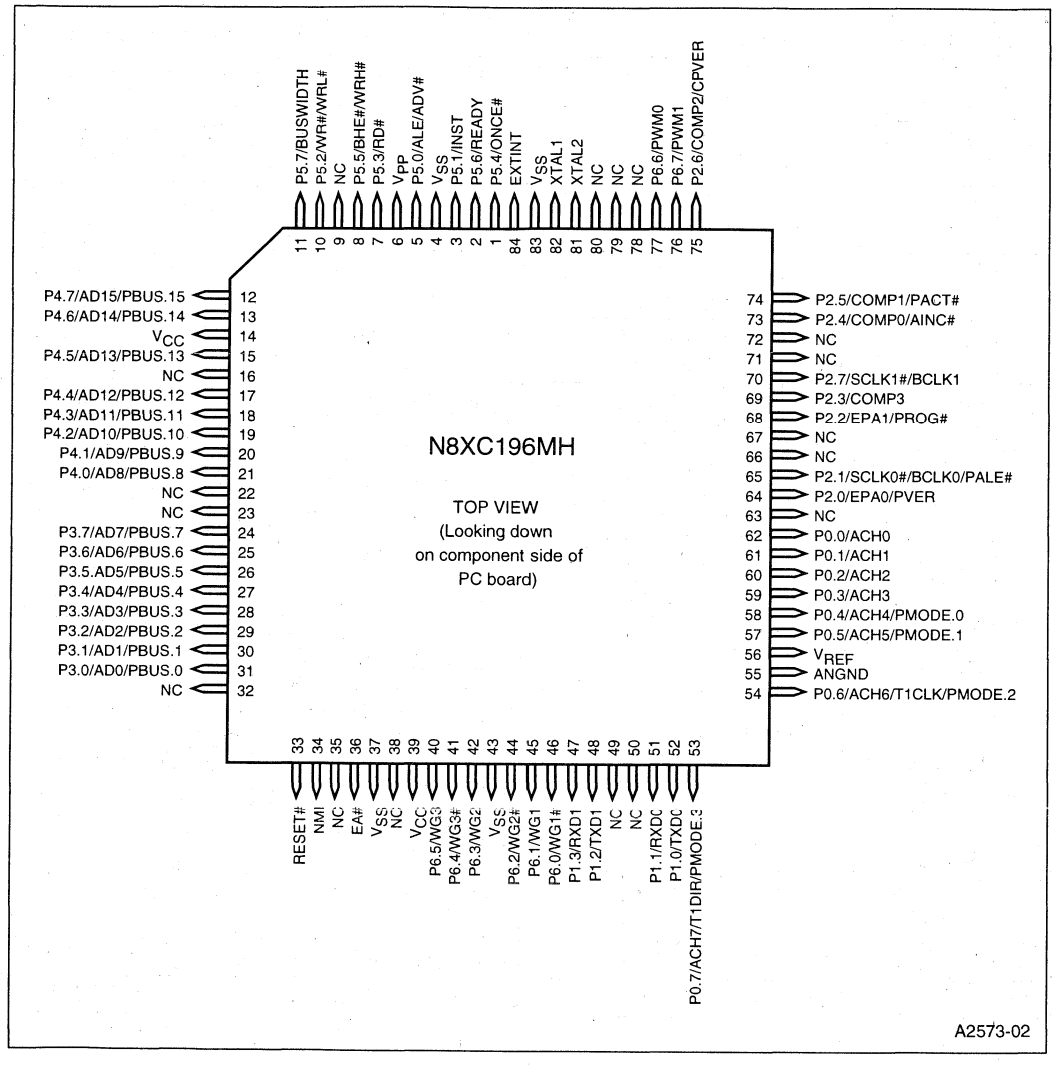


Figure 4. 8XC196MH 84-lead PLCC Package

Table 5. 84-lead PLCC Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	P5.4/ONCE#	22	NC	43	V_{SS}	64	P2.0/EPA0/PVER
2	P5.6/READY	23	NC	44	P6.2/WG2#	65	P2.1/SCLK0# /BCLK0/PALE#
3	P5.1/INST	24	P3.7/AD7 /PBUS.7	45	P6.1/WG1	66	NC
4	V_{SS}	25	P3.6/AD6 /PBUS.6	46	P6.0/WG1#	67	NC
5	P5.0/ALE/ADV#	26	P3.5/AD5 /PBUS.5	47	P1.3/RXD1	68	P2.2/EPA1 /PROG#
6	V_{PP}	27	P3.4/AD4 /PBUS.4	48	P1.2/TXD1	69	P2.3/COMP3
7	P5.3/RD#	28	P3.3/AD3 /PBUS.3	49	NC	70	P2.7/SCLK1# /BCLK1
8	P5.5/BHE#/WRH#	29	P3.2/AD2 /PBUS.2	50	NC	71	NC
9	NC	30	P3.1/AD1 /PBUS.1	51	P1.1/RXD0	72	NC
10	P5.2/WR#/WRL#	31	P3.0/AD0 /PBUS.0	52	P1.0/TXD0	73	P2.4/COMP0 /AINC#
11	P5.7/BUSWIDTH	32	NC	53	P0.7/ACH7 /T1DIR/PMODE.3	74	P2.5/COMP1 /PACT#
12	P4.7/AD15 /PBUS.15	33	RESET#	54	P0.6/ACH6 /T1CLK/PMODE.2	75	P2.6/COMP2 /CPVER
13	P4.6/AD14 /PBUS.14	34	NMI	55	ANGND	76	P6.7/PWM1
14	V_{CC}	35	NC	56	V_{REF}	77	P6.6/PWM0
15	P4.5/AD13 /PBUS.13	36	EA#	57	P0.5/ACH5 /PMODE.1	78	NC
16	NC	37	V_{SS}	58	P0.4/ACH4 /PMODE.0	79	NC
17	P4.4/AD12 /PBUS.12	38	NC	59	P0.3/ACH3	80	NC
18	P4.3/AD11 /PBUS.11	39	V_{CC}	60	P0.2/ACH2	81	XTAL2
19	P4.2/AD10 /PBUS.10	40	P6.5/WG3	61	P0.1/ACH1	82	XTAL1
20	P4.1/AD9/PBUS.9	41	P6.4/WG3#	62	P0.0/ACH0	83	V_{SS}
21	P4.0/AD8/PBUS.8	42	P6.3/WG2	63	NC	84	EXTINT

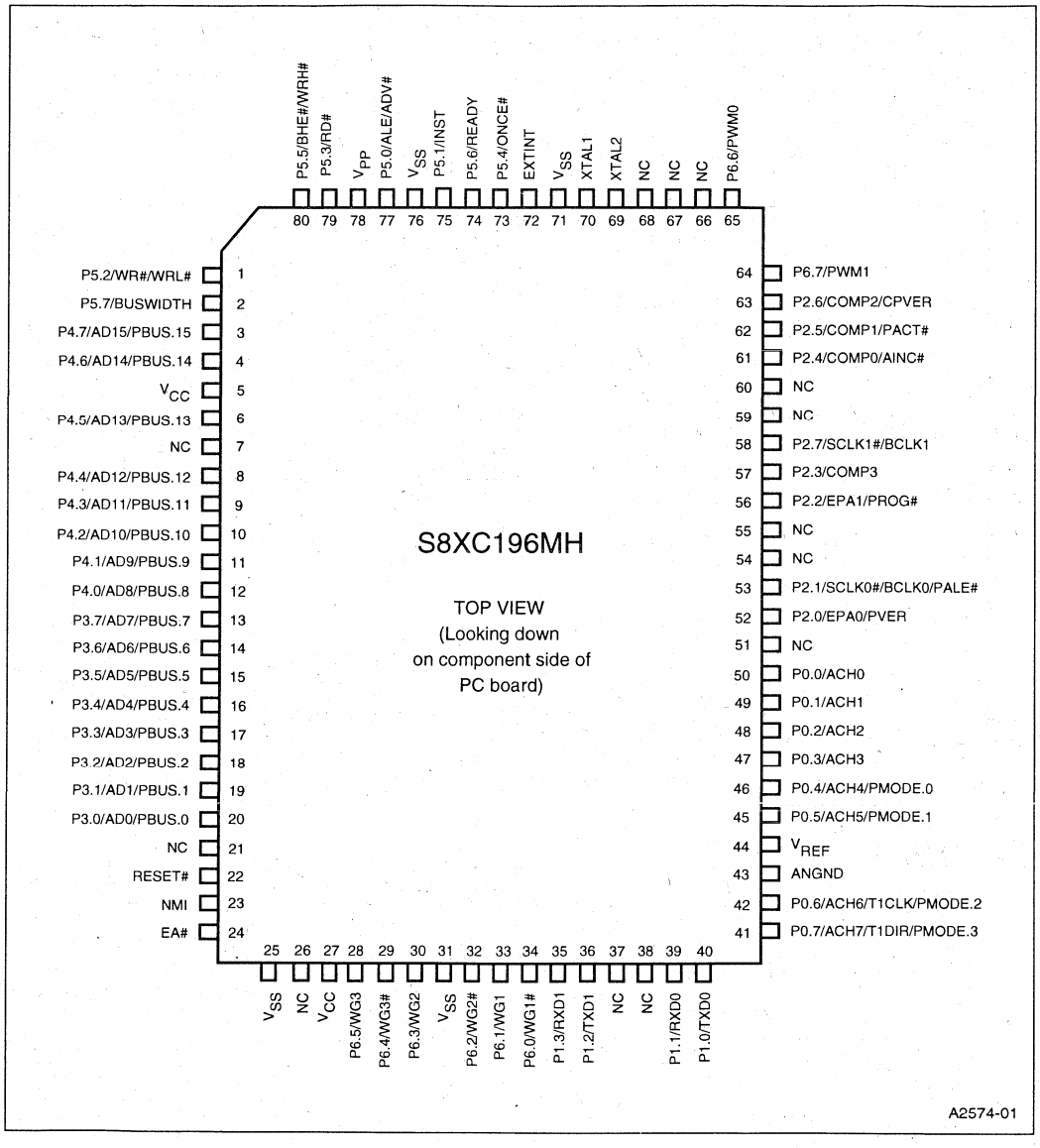


Figure 5. 8XC196MH 80-lead Shrink EIAJ/QFP Package

Table 6. 80-lead Shrink EIAJ/QFP Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	P5.2/WR#/WRL#	21	NC	41	P0.7/ACH7/T1DIR /PMODE.3	61	P2.4/COMP0 /AINC#
2	P5.7/BUSWIDTH	22	RESET#	42	P0.6/ACH6 /T1CLK/PMODE.2	62	P2.5/COMP1 /PACT#
3	P4.7/AD15 /PBUS.15	23	NMI	43	ANGND	63	P2.6/COMP2 /CPVER
4	P4.6/AD14 /PBUS.14	24	EA#	44	V_{REF}	64	P6.7/PWM1
5	V_{CC}	25	V_{SS}	45	P0.5/ACH5 /PMODE.1	65	P6.6/PWM0
6	P4.5/AD13 /PBUS.13	26	NC	46	P0.4/ACH4 /PMODE.0	66	NC
7	NC	27	V_{CC}	47	P0.3/ACH3	67	NC
8	P4.4/AD12 /PBUS.12	28	P6.5/WG3	48	P0.2/ACH2	68	NC
9	P4.3/AD11 /PBUS.11	29	P6.4/WG3#	49	P0.1/ACH1	69	XTAL2
10	P4.2/AD10 /PBUS.10	30	P6.3/WG2	50	P0.0/ACH0	70	XTAL1
11	P4.1/AD9/PBUS.9	31	V_{SS}	51	NC	71	V_{SS}
12	P4.0/AD8/PBUS.8	32	P6.2/WG2#	52	P2.0/EPA0/PVER	72	EXTINT
13	P3.7/AD7/PBUS.7	33	P6.1/WG1	53	P2.1/SCLK0# /BCLK0/PALE#	73	P5.4/ONCE#
14	P3.6/AD6/PBUS.6	34	P6.0/WG1#	54	NC	74	P5.6/READY
15	P3.5/AD5/PBUS.5	35	P1.3/RXD1	55	NC	75	P5.1/INST
16	P3.4/AD4/PBUS.4	36	P1.2/TXD1	56	P2.2/EPA1 /PROG#	76	V_{SS}
17	P3.3/AD3/PBUS.3	37	NC	57	P2.3/COMP3	77	P5.0/ALE/ADV#
18	P3.2/AD2/PBUS.2	38	NC	58	P2.7/SCLK1# /BCLK1	78	V_{PP}
19	P3.1/AD1/PBUS.1	39	P1.1/RXD0	59	NC	79	P5.3/RD#
20	P3.0/AD0/PBUS.0	40	P1.0/TXD0	60	NC	80	P5.5/BHE#/WRH#

PIN DESCRIPTIONS

Table 7. Signal Descriptions

Signal Name	Type	Description	Multiplexed With
ACH7 ACH6 ACH5 ACH4 ACH3:0	I	**Analog Channels**. These pins are analog inputs to the A/D converter. These pins are multiplexed with the port 0 pins. While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading the port while a conversion is in process can produce unreliable conversion results. The ANGND and V_{REF} pins must be connected for the A/D converter and the multiplexed port pins to function.	P0.7/T1DIR/PMODE.3 P0.6/T1CLK/PMODE.2 P0.5/PMODE.1 P0.4/PMODE.0 P0.3:0
AD15:8 AD7:0	I/O	**Address/Data Lines**. These pins provide a multiplexed address and data bus. During the address phase of the bus cycle, address bits 0–15 are presented on the bus and can be latched using ALE or ADV#. During the data phase, 8- or 16-bit data is transferred.	P4.7:0/PBUS.15:8 P3.7:0/PBUS.7:0
ADV#	O	**Address Valid**. This active-low output signal is asserted only during external memory accesses. ADV# indicates that valid address information is available on the system address/data bus. The signal remains low while a valid bus cycle is in progress and is returned high as soon as the bus cycle completes. An external latch can use the ADV# signal to demultiplex the address from the address/data bus. Used with a decoder, ADV# can generate chip-selects for external memory.	P5.0/ALE
AINC#	I	**Auto Increment**. In slave programming mode, this active-low input signal enables the autoincrement mode. Auto increment allows reading from or writing to sequential OTPROM locations without requiring address transactions across the programming bus for each read or write.	P2.4/COMP0
ALE	O	**Address Latch Enable**. This active-high output signal is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus. ALE differs from ADV# in that it is not returned high until a new bus cycle is to begin. An external latch can use ALE to demultiplex the address from the address/data bus.	P5.0/ADV#
ANGND	GND	**Analog Ground**. Reference ground for the A/D converter and the logic used to read port 0. ANGND must be held at nominally the same potential as V_{SS}.	—
BCLK1 BCLK0	I	**Serial Communications Baud Clock 0 and 1**. BCLK0 and 1 are alternate clock sources for the serial ports. The maximum input frequency is $F_{OSC}/4$.	P2.7/SCLK1# P2.1/SCLK0#/PALE#

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
BHE#	O	**Byte High Enable.** During 16-bit bus cycles, this active-low output signal is asserted for word reads and writes and for high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system address/data bus. BHE#, in conjunction with A0, selects the memory byte to be accessed: **BHE# A0 Byte(s) Accessed** 0 0 both bytes 0 1 high byte only 1 0 low byte only	P5.5/WRH#
BUSWIDTH	I	**Bus Width.** When enabled in the chip configuration register, this active-high input signal dynamically selects the bus width of the bus cycle in progress. When BUSWIDTH is high, a 16-bit bus cycle occurs; when BUSWIDTH is low, an 8-bit bus cycle occurs. BUSWIDTH is active during a CCR fetch.	P5.7
COMP3 COMP2 COMP1 COMP0	O	**Event Processor Array (EPA) Compare Pins.** These signals are the output of the EPA compare modules. These pins are multiplexed with other signals and may be configured as standard I/O.	P2.3 P2.6/CPVER P2.5/PACT# P2.4/AINC#
CPVER	O	**Cumulative Program Verification.** This active-high output signal indicates whether any verify errors have occurred since the device entered programming mode. CPVER remains high until a verify error occurs, at which time it is driven low. Once an error occurs, CPVER remains low until the device exits programming mode. When high, CPVER indicates that all locations have programmed correctly since the device entered programming mode.	P2.6/COMP2
EA#	I	**External Access.** This active-low input signal directs memory accesses to on-chip or off-chip memory. If EA# is low, the memory access is off-chip. If EA# is high and the memory address is within 2000H–2FFFH, the access is to on-chip ROM or OTPROM. Otherwise, an access with EA# high is to off-chip memory. EA# is sampled **only** on the rising edge of RESET#. If EA# = V_{EA} on the rising edge of RESET#, the device enters the programming mode selected by PMODE.3:0. For devices without ROM, EA# must be tied low.	—
EPA1 EPA0	I/O	**Event Processor Array (EPA) Input/Output pins.** These are the high-speed input/output pins for the EPA capture/compare modules. These pins are multiplexed with other signals and may be configured as standard I/O.	P2.2/PROG# P2.0/PVER

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
EXTINT	I	**External Interrupt**. This programmable interrupt is controlled by the WG_PROTECT register. This register controls whether the interrupt is edge triggered or sampled and whether a rising edge/high level or falling edge/low level activates the interrupt. This interrupt vectors through memory location 203CH. If the chip is in idle mode and if EXTINT is enabled, a valid EXTINT interrupt brings the chip back to normal operation, where the first action is to execute the EXTINT service routine. After completion of the service routine, execution resumes at the instruction following the one that put the chip into idle mode. In powerdown mode, a valid EXTINT interrupt causes the chip to return to normal operating mode. If EXTINT is enabled, the EXTINT service routine is executed. Otherwise, execution continues at the instruction following the IDLPD instruction that put the chip into powerdown mode.	—
INST	O	**Instruction Fetch**. This active-high output signal is valid only during external memory bus cycles. When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch. INST is low for data accesses, including interrupt vector fetches and chip configuration byte reads. INST is low during internal memory fetches.	P5.1
NMI	I	**Nonmaskable Interrupt**. In normal operating mode, a rising edge on NMI causes a vector through the NMI interrupt at location 203EH. NMI must be asserted for greater than one state time to guarantee that it is recognized. In idle mode, a rising edge on NMI brings the chip back to normal operation, where the first action is to execute the NMI service routine. After completion of the service routine, execution resumes at the instruction following the one that put the chip into idle mode. In powerdown mode, NMI causes a return to normal operating mode only if it is tied to EXTINT.	—
ONCE#	I	**On-circuit Emulation**. Holding this pin low while the RESET# signal transitions from a low to a high places the device into on-circuit emulation (ONCE) mode. ONCE mode isolates the device from other components in the system to allow the use of a clip-on emulator for system debugging. This mode puts all pins except XTAL1 and XTAL2 into a high-impedance state. To exit ONCE mode, reset the device by pulling the RESET# signal low.	P5.4

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
P0.7 P0.6 P0.5 P0.4 P0.3:0	I	**Port 0**. This is a high-impedance, input-only port. Port 0 pins should **not** be left floating. These pins may individually be used as analog inputs (ACH*x*) or digital inputs (P0.*x*). While it is possible for the pins to function simultaneously as analog and digital inputs, this is not recommended because reading port 0 while a conversion is in process can produce unreliable conversion results. ANGND and V_{REF} must be connected for port 0 and the A/D converter to function.	ACH7/T1DIR/PMODE.3 ACH6/T1CLK/PMODE.2 ACH5/PMODE.1 ACH4/PMODE.0 ACH3:0
P1.3 P1.2 P1.1 P1.0	I	**Port 1**. This is a 4-bit, bidirectional, standard I/O port that is multiplexed with individually selectable special-function signals. (Used as PBUS.15:12 in Auto-programming Mode.)	RXD1 TXD1 RXD0 TXD0
P2.7 P2.6 P2.5 P2.4 P2.3 P2.2 P2.1 P2.0	I/O	**Port 2**. This is an 8-bit, bidirectional, standard I/O port that is multiplexed with individually selectable special-function signals. P2.6 is multiplexed with a special test mode function. To prevent accidental entry into test modes, always configure P2.6 as an output.	SCLK1#/BCLK1 COMP2/CPVER COMP1/PACT# COMP0/AINC# COMP3 EPA1/PROG# SCLK0#/BCLK0/PALE# EPA0/PVER
P3.7:0	I/O	**Port 3**. This is an 8-bit, bidirectional, memory-mapped I/O port with open-drain outputs. The pins are shared with the multiplexed address/data bus, which has complementary drivers. In programming modes, port 3 serves as the low byte of the programming bus (PBUS).	AD7:0/PBUS.7:0
P4.7:0	I/O	**Port 4**. This is an 8-bit, bidirectional, memory-mapped I/O port with open-drain outputs. The pins are shared with the multiplexed address/data bus, which has complementary drivers. In programming modes, port 4 serves as the high byte of the programming bus (PBUS).	AD15:8/PBUS.15:8
P5.7 P5.6 P5.5 P5.4 P5.3 P5.2 P5.1 P5.0	I/O	**Port 5**. This is an 8-bit, bidirectional, standard I/O port that is multiplexed with individually selectable control signals. Because P5.4 is multiplexed with the ONCE# function, always configure it as an output to prevent accidental entry into ONCE mode.	BUSWIDTH READY BHE#/WRH# ONCE# RD# WR#/WRL# INST ALE/ADV#

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
P6.7 P6.6 P6.5 P6.4 P6.3 P6.2 P6.1 P6.0	O	**Port 6.** This is an 8-bit output port that is multiplexed with the special functions of the waveform generator and PWM peripherals. The WG_OUT register configures the pins, establishes the output polarity, and controls whether changes to the outputs are synchronized with an event or take effect immediately.	PWM1 PWM0 WG3 WG3# WG2 WG2# WG1 WG1#
PACT#	O	**Programming Active.** In auto-programming mode, PACT# low indicates that programming activity is occurring.	P2.5/COMP1
PALE#	I	**Programming ALE.** In slave programming mode, this active-low input indicates that ports 3 and 4 contain a command/address. When PALE# is asserted, data and commands on ports 3 and 4 are read into the device.	P2.1/SCLK0#/BCLK0
PBUS.15:8 PBUS.7:0	I/O	**Programming Bus.** In programming modes, used as a bidirectional port with open-drain outputs to pass commands, addresses, and data to or from the device. Used as a regular system bus to access external memory during auto-programming mode. When using slave programming mode, the PBUS is used in open-drain I/O port mode (not as a system bus). In slave programming mode, you must add external pull-up resistors to read data from the device during the dump word routine.	P4.7:0/AD15:8 P3.7:0/AD7:0
PMODE.3 PMODE.2 PMODE.1 PMODE.0	I	**Programming Mode Select.** Determines the OTPROM programming algorithm that is to be performed. PMODE is sampled after a device reset when EA# = V_{EA} and must be stable while the device is operating.	P0.7/ACH7/T1DIR P0.6/ACH6/T1CLK P0.5/ACH5 P0.4/ACH4
PROG#	I	**Programming Start.** This active-low input is valid only in slave programming mode. The rising edge of PROG# latches data on the PBUS and begins programming. The falling edge of PROG# ends programming.	P2.2/EPA1
PVER	O	**Program Verification.** In programming modes, this active-high output signal is asserted to indicate that the word has programmed correctly. (PVER low after the rising edge of PROG# indicates an error.)	P2.0/EPA0
PWM1:0	O	**Pulse Width Modulator Outputs.** These are PWM output pins with high-current drive capability. The duty cycle and frequency-pulse-widths are programmable.	P6.7:6
RD#	O	**Read.** Read-signal output to external memory. RD# is asserted only during external memory reads.	P5.3

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
READY	I	**Ready Input.** This active-high input signal is used to lengthen external memory cycles for slow memory by generating wait states. When READY is high, CPU operation continues in a normal manner. If READY is low, the memory controller inserts wait states until the READY signal goes high or until the number of wait states is equal to the number programmed into the chip configuration register. READY is ignored for all internal memory accesses.	P5.6
RESET#	I/O	**Reset.** Reset input to and open-drain output from the chip. A falling edge on RESET# initiates the reset process. When RESET# is first asserted, the chip turns on a pull-down transistor connected to the RESET pin for 16 state times. This function can also be activated by execution of the RST instruction. In the powerdown and idle modes, asserting RESET# causes the chip to reset and return to normal operating mode. RESET# is a level-sensitive input.	—
RXD1 RXD0	I/O	**Receive Serial Data 0 and 1.** In modes 1, 2, and 3, RXD0 and 1 are used to receive serial port data. In mode 0, they function as either inputs or open-drain outputs for data.	P1.3 P1.1
SCLK1# SCLK0#	I/O	**Synchronous Clock Pin 0 and 1.** In mode 4, these are the bidirectional, shift clock signals that synchronize the serial data transfer. Data is transferred 8 bits at a time with the LSB first. The DIR bit (SP_CON*x*.7) controls the direction of SCLK*x* signal. DIR = 0 The internal shift clock is output on SCLK*x*. DIR = 1 An external shift clock is input on SCLK*x*.	P2.7/BCLK1 P2.1/BCLK0
T1CLK	I	**External Clock.** External clock for timer 1. Timer 1 increments (or decrements) on both rising and falling edges of T1CLK. Also used in conjunction with T1DIR for quadrature counting mode.	P0.6/ACH6/PMODE.2
T1DIR	I	**Timer 1 External Direction.** External direction (up/down) for timer 1. Timer 1 increments when T1DIR is high and decrements when it is low. Also used in conjunction with T1CLK for quadrature counting mode.	P0.7/ACH7/PMODE.3
TXD1 TXD0	O	**Transmit Serial Data 0 and 1.** In serial I/O modes 1, 2, and 3, TXD0 and 1 are used to transmit serial port data. In mode 0, they are used as the serial clock output.	P1.2 P1.0
V_{CC}	PWR	**Digital Supply Voltage.** Connect each V_{CC} pin to the digital supply voltage.	—
V_{PP}	PWR	**Programming Voltage.** Set to 12.5 V when programming the on-chip OTPROM. Also the timing pin for the "return from power-down" circuit.	—

Table 7. Signal Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
V_{REF}	PWR	**Reference Voltage for the A/D Converter.** V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. V_{REF} must be connected for the A/D and port 0 to function.	—
V_{SS}	GND	**Digital Circuit Ground** (0 volts). Connect each V_{SS} pin to ground.	—
WG3 WG2 WG1	O	**Waveform Generator Phase 1–3 Positive Outputs.** 3-phase output signals used in motion-control applications.	P6.5 P6.3 P6.1
WG3# WG2# WG1#	O	**Waveform Generator Phase 1–3 Negative Outputs.** Complementary 3-phase output signals used in motion-control applications.	P6.4 P6.2 P6.0
WR#	O	**Write.** This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes.	P5.2/WRL#
WRH#	O	**Write High.** During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory. During 8-bit bus cycles, WRH# is asserted for all write operations.	P5.5/BHE#
WRL#	O	**Write Low.** During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes. During 8-bit bus cycles, WRL# is asserted for all write operations.	P5.2/WR#
XTAL1	I	**Clock/Oscillator Input.** Input to the on-chip oscillator inverter and the internal clock generator. Also provides the clock input for the serial I/O baud-rate generator, timers, and PWM unit. If an external oscillator is used, connect the external clock input signal to XTAL1 and ensure that the XTAL1 V_{IH} specification is met.	—
XTAL2	O	**Oscillator Output.** Output of the on-chip oscillator inverter. When using the on-chip oscillator, connect XTAL2 to an external crystal or resonator. When using an external clock source, let XTAL2 float.	—

ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... – 65°C to + 150°C
Ambient Temperature
under Bias..... – 40°C to + 85°C
Voltage from V_{PP} or EA# to
V_{SS} or ANGND (Note 1) ..... – 0.5 V to + 13.0 V
Voltage with respect to
V_{SS} or ANGND (Note 1) ..... – 0.5 V to + 7.0 V
(This includes V_{PP} on ROM and CPU devices.)
Power Dissipation ..... 1.5 W
(based on package heat transfer limitations, not device power consumption)

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

OPERATING CONDITIONS*

T_A (Ambient Temperature Under Bias) .....– 40°C to + 85°C
V_{CC} (Digital Supply Voltage) ..... 4.50 V to 5.50 V
V_{REF} (Analog Supply Voltage) ..... 4.50 V to 5.50 V
F_{OSC} (Oscillator Frequency) (Note 2) ..... 8 MHz to 16 MHz

NOTES:
1. ANGND and V_{SS} should be at nominally the same potential.
2. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.

DC CHARACTERISTICS

Table 8. DC Characteristics over Specified Operating Conditions

Symbol	Parameter	Min	Typ (4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (standard inputs (1))	– 0.5		0.3 V_{CC}	V	
V_{IL1}	Input Low Voltage (RESET#, ports 3, 4, and 5)	– 0.5		0.8	V	
V_{IH}	Input High Voltage (standard inputs (1))	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (RESET#, ports 3, 4, and 5)	0.2 V_{CC} + 1.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (RESET#, ports 1, 2, 5, P6.6, P6.7, and XTAL2)			0.3 0.45 1.5	V V V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OL1}	Output Low Voltage (ports 3, 4)			1.0	V	I_{OL} = 7 mA
V_{OL2}	Output Low Voltage (P6.5:0)			0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (output pins and I/O configured as push/pull outputs)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V V V	I_{OH} = – 200 µA I_{OH} = – 3.2 mA I_{OH} = – 7.0 mA
$V_{TH+} - V_{TH-}$	Hysteresis voltage width on RESET# pin	0.2			V	
I_{LI}	Input Leakage Current (standard inputs (1))			± 10	µA	$V_{SS} < V_{IN} < V_{CC}$ – 0.3V
I_{LI1}	Input Leakage Current (port 0 – A/D inputs)			± 3	µA	$V_{SS} < V_{IN} < V_{REF}$
I_{IH}	Input High Current (NMI)			300	µA	V_{IN} = 0.7 V_{CC}
I_{IL}	Input Low Current (port 2, except P2.6)			– 70	µA	V_{IN} = 0.3 V_{CC}

NOTES:
1. Standard input pins include XTAL1, EA#, and Ports 1 and 2 when configured as inputs.
2. Maximum current that an external device must sink to ensure test mode entry.
3. Violating these specifications during reset may cause the device to enter test modes.
4. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC} = 5.5$ V.
5. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
6. All voltages are referenced relative to V_{SS}. When used, V_{SS} refers to the device pin.
7. Table 9 lists the total current limits during normal (non-transient conditions). The total current listed is the sum of the pins listed for each specification value.

Table 8. DC Characteristics over Specified Operating Conditions (Continued)

Symbol	Parameter	Min	Typ (4)	Max	Units	Test Conditions
I_{IL1}	Input Low Current (P5.4 and P2.6 during reset) (2)			– 10	mA	V_{IN} = 0.8 V
I_{IL2}	Input Low Current (ports 3, 4, and 5, except P5.4)			– 300	µA	V_{IN} = 0.8 V
I_{IL3}	Input Low Current (port 1)			– 300	µA	V_{IN} = 0.3 V_{CC}
I_{OH}	Output High Current (P5.4 and P2.6 during reset) (3)	– 0.2			mA	0.7 V_{CC}
I_{OH1}	Output High Current (P6.5:0 during reset)	– 6		– 40	µA	0.7 V_{CC}
I_{CC}	V_{CC} Supply Current		50	70	mA	XTAL1 = 16 MHz V_{CC} = 5.5 V V_{PP} = 5.5 V V_{REF} = 5.5 V
I_{REF}	A/D Reference Supply Current		2	5	mA	
I_{IDLE}	Idle Mode Current		15	30	mA	
I_{PD}	Powerdown Mode Current (4)		5	50	µA	
R_{RST}	Reset Pull-up Resistor	6		65	kΩ	
C_S	Pin Capacitance (any pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz

NOTES:
1. Standard input pins include XTAL1, EA#, and Ports 1 and 2 when configured as inputs.
2. Maximum current that an external device must sink to ensure test mode entry.
3. Violating these specifications during reset may cause the device to enter test modes.
4. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC} = 5.5$ V.
5. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
6. All voltages are referenced relative to V_{SS}. When used, V_{SS} refers to the device pin.
7. Table 9 lists the total current limits during normal (non-transient conditions). The total current listed is the sum of the pins listed for each specification value.

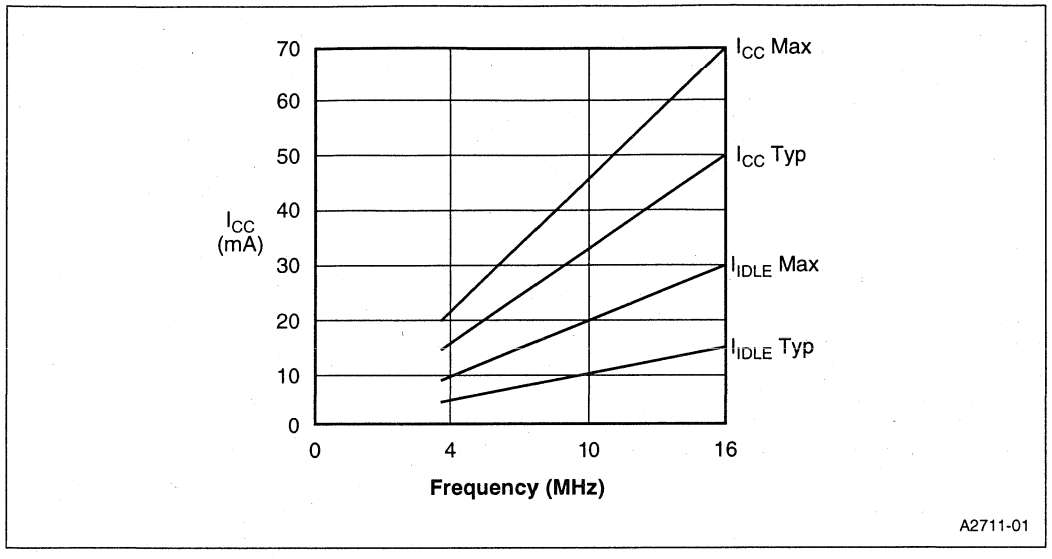


Table 9. Total Current Limits During Normal (Non-transient) Conditions

Signal Names	Maximum I_{OL} Limits	Maximum I_{OH} Limits
Port 1	25 mA	– 25 mA
Port 2, P6.6, P6.7	40 mA	– 40 mA
Port 3	40 mA	– 30 mA
Port 4	40 mA	– 30 mA
Port 5	40 mA	– 30 mA
P6.5:0	40 mA	– 30 mA

Figure 6. I_{CC}, I_{IDLE} versus Frequency

EXPLANATION OF AC SYMBOLS

Each symbol consists of two pairs of letters prefixed by "T" (for time). The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points. For example, T_{RHDZ} is the time between signal R (RD#) condition H (high) and signal D (Input Data) condition Z (floating). Table 10 defines the signal and condition codes.

Table 10. AC Timing Symbol Definitions

Signals				Conditions	
A	Address	P	PROG#	H	High
B	BHE#	Q	Data Out	L	Low
D	Data In	R	RD#	V	Valid
G	BUSWIDTH	V	PVER	X	No Longer Valid
I	T1DIR/AINC#	W	WR#/WRH#/WRL#	Z	Floating
K	T1CLK	X	XTAL1		
L	ALE/ADV#/PALE#	Y	READY		

AC CHARACTERISTICS (OVER SPECIFIED OPERATION CONDITIONS)

Table 11 defines the AC timing specifications that the external memory system must meet and those that the 8XC196MH will provide.

Table 11. AC Timing Definitions (1)

Symbol	Parameter	Min	Max	Units	Notes
F_{OSC}	Frequency on XTAL1	8	16	MHz	4
T_{OSC}	$1/F_{OSC}$	62.5	125	ns	
The External Memory System Must Meet These Specifications					
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE/ADV# Low to READY Setup		$T_{OSC} - 70$	ns	
T_{YLYH}	Non READY Time	No Upper Limit		ns	
T_{LLYX}	READY Hold after ALE/ADV# Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	2
T_{AVGV}	Address Valid to BUSWIDTH Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE/ADV# Low to BUSWIDTH Setup		$T_{OSC} - 60$	ns	

NOTES:
1. Test Conditions: Capacitive load on all pins = 100 pF, rise and fall times = 10 ns, F_{OSC} = 16 MHz.
2. Exceeding the maximum specification causes additional wait states.
3. If wait states are used, add $2T_{OSC} \times n$, where n = number of wait states.
4. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
5. Assuming back-to-back bus cycles.
6. 8-bit bus only.

Table 11. AC Timing Definitions (1) (Continued)

Symbol	Parameter	Min	Max	Units	Notes
The External Memory System Must Meet These Specifications (Continued)					
T_{LLGX}	BUSWIDTH Hold after ALE/ADV# Low	T_{OSC}		ns	
T_{LHDV}	ALE/ADV# High to Input Data Valid		$3T_{OSC} - 55$	ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	3
T_{RLDV}	RD# Active to Input Data Valid		$T_{OSC} - 30$	ns	3
T_{RHDZ}	End of RD# to Input Data Float		T_{OSC}	ns	
T_{RXDX}	Data Hold after RD# Inactive	0		ns	
The 8XC196MH will Meet These Specifications					
T_{XHLH}	XTAL1 Rising Edge to ALE Rising	20	110	ns	
T_{XHLL}	XTAL1 Rising Edge to ALE Falling	20	110	ns	
T_{LHLH}	ALE/ADV# Cycle Time	$4T_{OSC}$		ns	3
T_{LHLL}	ALE/ADV# High Period	$T_{OSC} - 10$	$T_{OSC} + 10$	ns	
T_{AVLH}	Address Valid to ALE/ADV# High	$T_{OSC} - 17$		ns	
T_{AVLL}	Address Valid to ALE/ADV# Low	$T_{OSC} - 17$		ns	
T_{LLAX}	Address Hold after ALE/ADV# Low	$T_{OSC} - 40$		ns	
T_{LLRL}	ALE/ADV# Low to RD# Low	$T_{OSC} - 30$		ns	
T_{RLRH}	RD# Low Period	$T_{OSC} - 5$	$T_{OSC} + 25$	ns	3
T_{RHLH}	RD# High to ALE/ADV# High	T_{OSC}	$T_{OSC} + 25$	ns	5
T_{RLAZ}	RD# Low to Address Float		5	ns	
T_{LLWL}	ALE/ADV# Low to WR# Low	$T_{OSC} - 10$		ns	
T_{QVWH}	Data Valid before WR# High	$T_{OSC} - 23$		ns	
T_{WLWH}	WR# Low Period	$T_{OSC} - 30$		ns	3
T_{WHQX}	Data Hold after WR# High	$T_{OSC} - 25$		ns	
T_{WHLH}	WR# High to ALE/ADV# High	$T_{OSC} - 10$	$T_{OSC} + 15$	ns	5
T_{WHBX}	BHE#, INST Hold after WR# High	$T_{OSC} - 10$		ns	
T_{WHAX}	A15:8 Hold after WR# High	$T_{OSC} - 30$		ns	6
T_{RHBX}	BHE#, INST Hold after RD# High	$T_{OSC} - 10$		ns	
T_{RHAX}	A15:8 Hold after RD# High	$T_{OSC} - 30$		ns	6

NOTES:
1. Test Conditions: Capacitive load on all pins = 100 pF, rise and fall times = 10 ns, F_{OSC} = 16 MHz.
2. Exceeding the maximum specification causes additional wait states.
3. If wait states are used, add $2T_{OSC} \times n$, where n = number of wait states.
4. Testing is performed down to 8 MHz, although the device is static by design and will typically operate below 1 Hz.
5. Assuming back-to-back bus cycles.
6. 8-bit bus only.

SYSTEM BUS TIMINGS

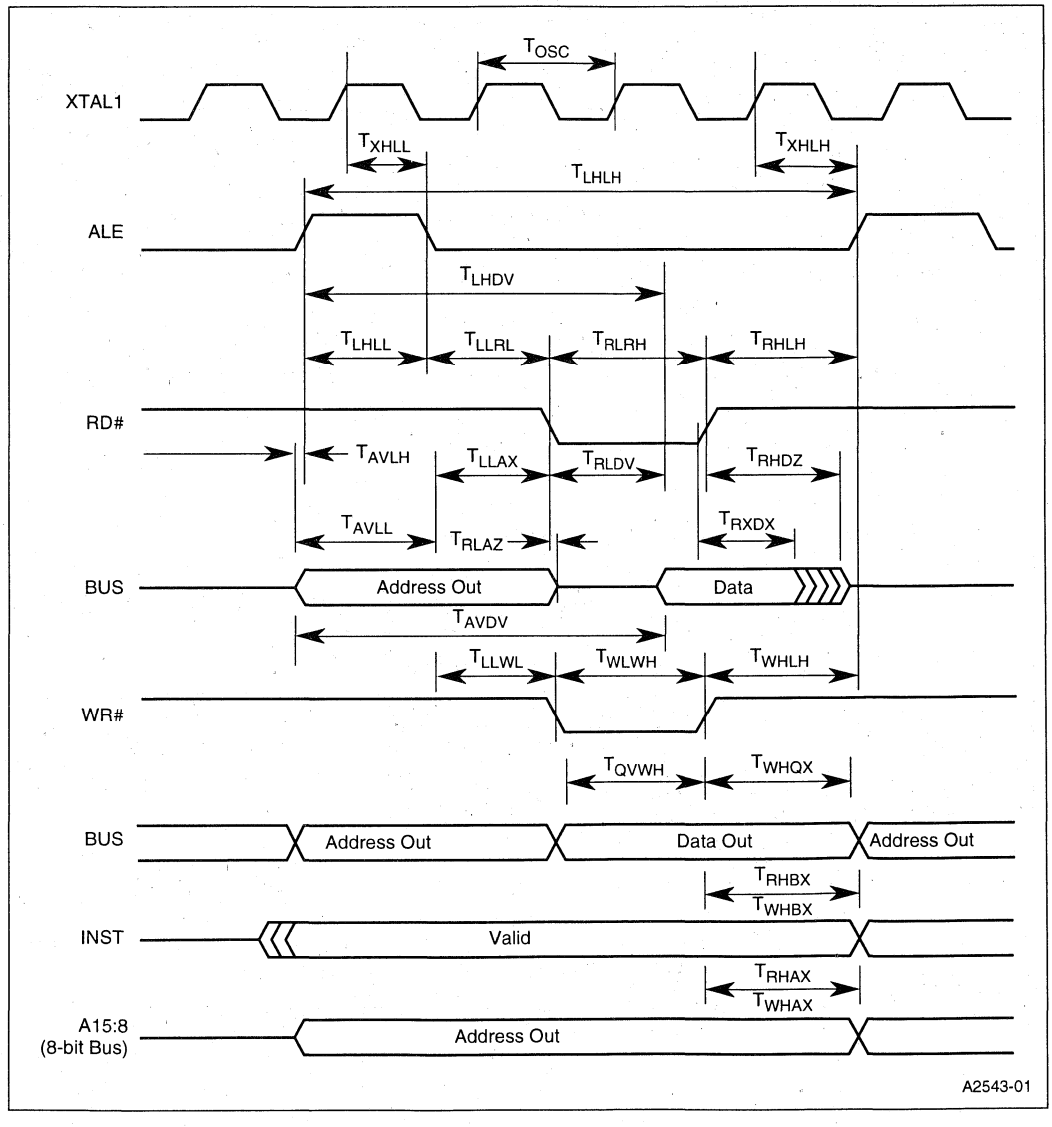


Figure 7. System Bus Timing Diagram

READY TIMING (ONE WAIT STATE)

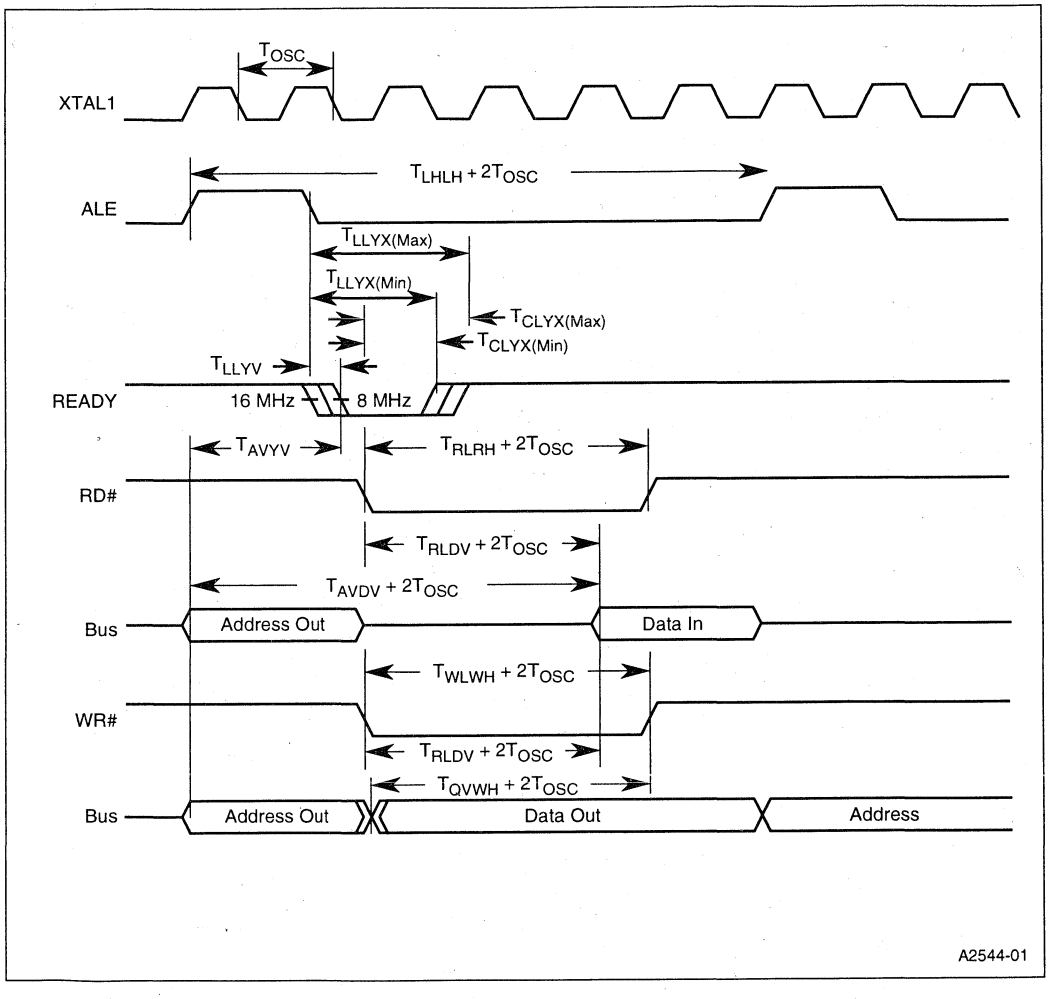


Figure 8. READY Timing Diagram (One Wait State)

BUSWIDTH TIMING

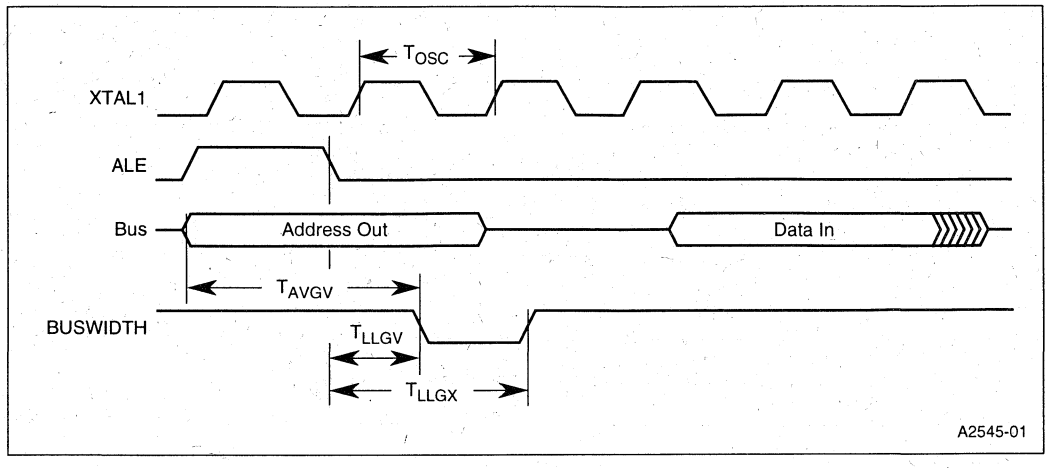


Figure 9. BUSWIDTH Timing Diagram

EXTERNAL CLOCK DRIVE

Table 12. External Clock Drive Timing

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	8	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	125	ns
T_{XHXX}	High Time	22		ns
T_{XLXX}	Low Time	22		ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

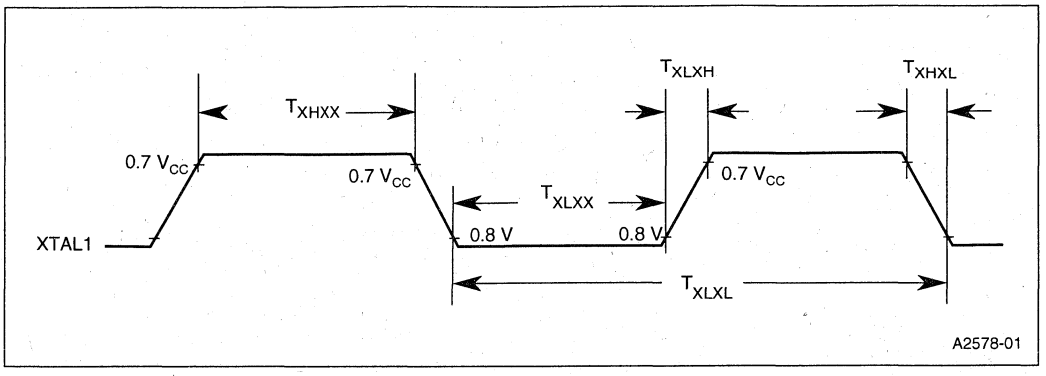


Figure 10. External Clock Drive Waveforms

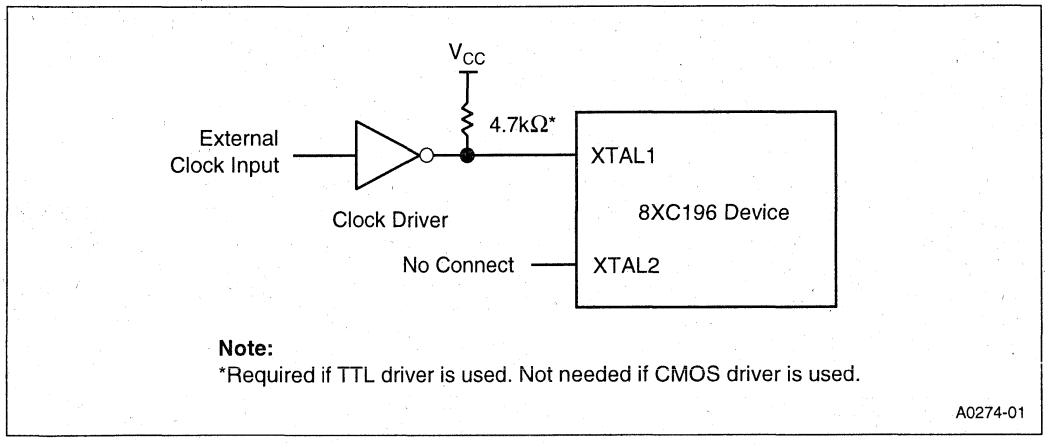
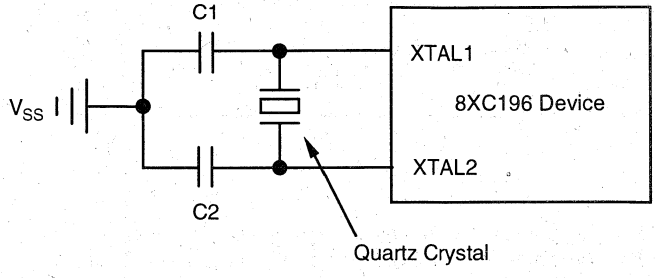


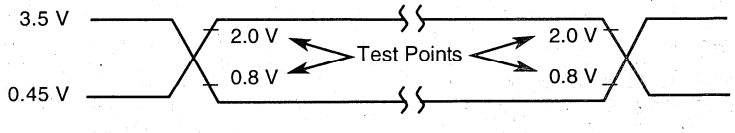
Figure 11. External Clock Connections



Note:
Keep oscillator components close to the chip and use short, direct traces to XTAL1, XTAL2, and V_{SS}. When using crystals, C1=C2≈20pF. When using ceramic resonators, consult the manufacturer for recommended oscillator circuitry.

A0273-01

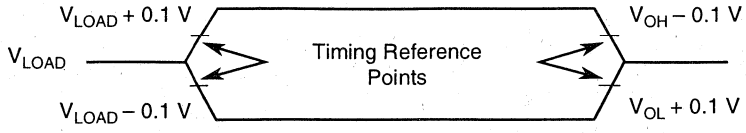
Figure 12. External Crystal Connections



AC testing inputs are driven at 3.5 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

A2120-02

Figure 13. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A2579-01

Figure 14. Float Waveforms

AC CHARACTERISTICS — SERIAL PORT, SHIFT REGISTER MODE

Table 13. Serial Port Timing — Shift Register Mode (Mode 0)

Symbol	Parameter	Min	Max	Units	Notes
T_{XLXL}	Serial Port Clock Period (Baud-rate*n* ≥ 8002H) (Baud-rate*n* = 8001H)	 $6T_{OSC}$ $4T_{OSC}$		 ns ns	 1, 2
T_{XLXH}	Serial Port Clock Low Period (Baud-rate*n* ≥ 8002H) (Baud-rate*n* = 8001H)	 $4T_{OSC} - 50$ $2T_{OSC} - 50$	 $4T_{OSC} + 50$ $2T_{OSC} + 50$	 ns ns	 1, 2
T_{QVXH}	Output Data Setup to Clock High	$2T_{OSC} - 50$		ns	
T_{XHQX}	Output Data Hold after Clock High	$2T_{OSC} - 50$		ns	
T_{XHQV}	Next Output Data Valid after Clock High		$2T_{OSC} + 50$	ns	
T_{DVXH}	Input Data Setup to Clock High	$T_{OSC} + 50$		ns	
T_{XHDX}	Input Data Hold after Clock High	0		ns	
T_{XHQZ}	Last Clock High to Output Float		T_{OSC}	ns	

NOTES:
1. *n* for Baud-rate*n* signifies Serial Port 0 or 1.
2. Maximum Serial Port Mode 0 reception is with Baud-rate*n* ≥ 8002H.

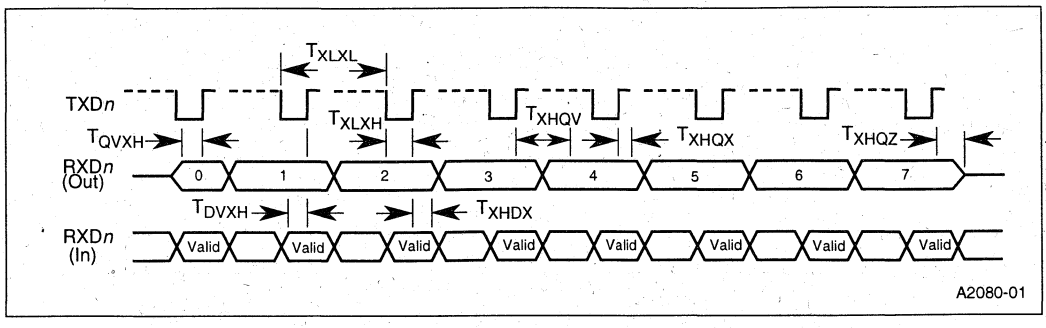


Figure 15. Serial Port Waveform — Shift Register Mode (Mode 0)

Table 14. Serial Port Timing — Mode 4

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (DIR=0)	$16T_{OSC}$	$131072T_{OSC}$	ns
T_{XLXX}	Serial Port Clock Low Period (DIR=0/1)	$(T_{XLXL}/2) - 30$		ns
T_{XHXX}	Serial Port Clock High Period (DIR=0/1)	$(T_{XLXL}/2) - 30$		ns
T_{XLXL}	Serial Port Clock Period (DIR=1)	$16T_{OSC}$		ns
T_{XHXL}	Serial Clock Falling Time (DIR=1)	0	20	ns
T_{XLXH}	Serial Clock Rising Time (DIR=1)	0	20	ns
T_{XLQV}	Clock Low to Output Data Setup		$7.5T_{OSC} - 50$	ns
T_{XLQX}	Output Data Hold after Clock Low	0		ns
T_{XHQX}	Last Output Data Hold after Clock High (DIR=1)	$13.7T_{OSC}$		ns
T_{DVXX}	Input Data Setup to Clock Low Invalid	0		ns
T_{XHDH}	Input Data Hold after Clock High	$6T_{OSC}$		ns

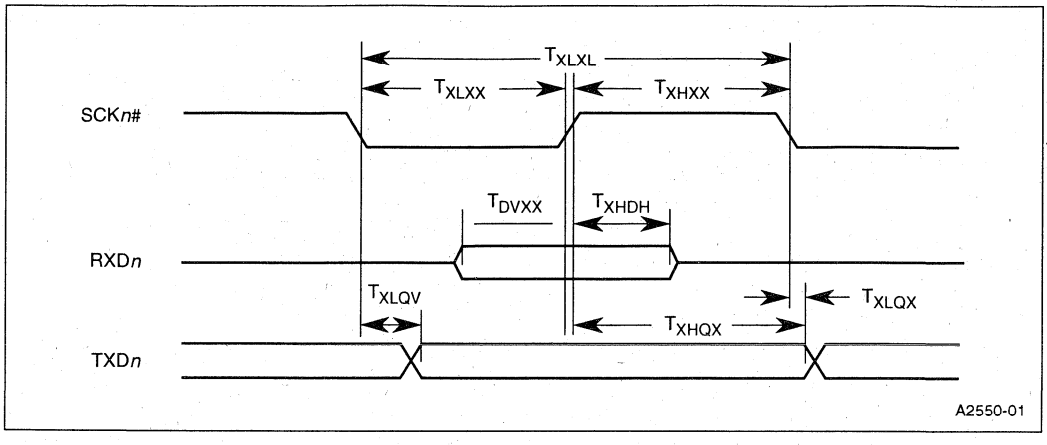


Figure 16. Serial Port Waveform — Mode 4

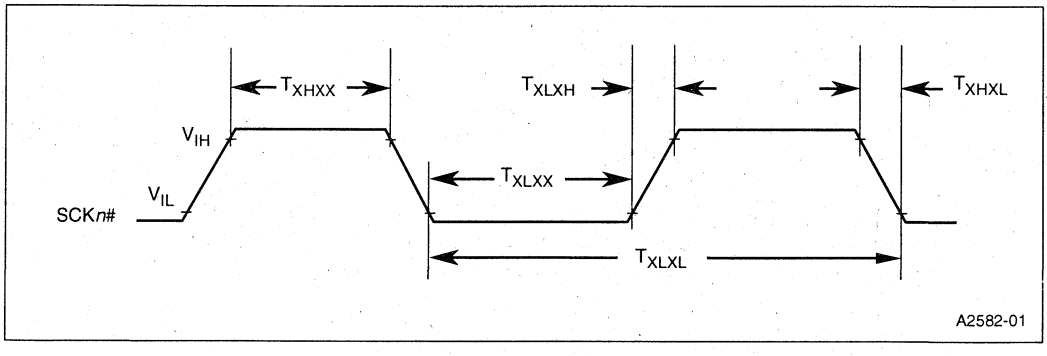


Figure 17. Serial Port Waveform — Clock Drive (DIR = 1)

BAUD-RATE CLOCK DRIVE TABLE

Table 15. Baud Rate Clock Drive

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Baud Rate Clock Period		$4T_{OSC}$	ns
T_{XHXX}	Baud Rate Clock High Time	$2T_{OSC} - 30$		ns
T_{XLXX}	Baud Rate Clock Low Time	$2T_{OSC} - 30$		ns
T_{XLXH}	Baud Rate Clock Rise Time		20	ns
T_{XHXL}	Baud Rate Clock Fall Time		20	ns

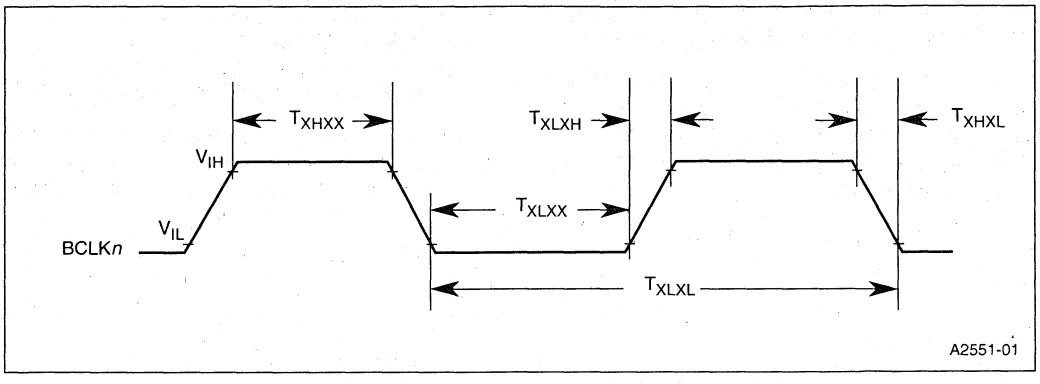


Figure 18. Baud-Rate Clock Drive Waveforms

A/D SAMPLE AND CONVERSION TIMES

Two parameters, sample time and conversion time, control the time required for an A/D conversion. The sample time is the length of time that the analog input voltage is actually connected to the sample capacitor. If this time is too short, the sample capacitor will not charge completely. If the sample time is too long, the input voltage may change and cause conversion errors. The conversion time is the length of time required to convert the analog input voltage stored on the sample capacitor to a digital value. The conversion time must be long enough for the comparator and circuitry to settle and resolve the voltage. Excessively long conversion times allow the sample capacitor to discharge, degrading accuracy.

The AD_TIME register programs the A/D sample and conversion times. Use the T_{SAM} and T_{CONV} specifications in Tables 16 and 18 to determine appropriate values for SAM and CONV; otherwise, erroneous conversion results may occur.

Use the following formulas to determine the SAM and CONV values:

$$SAM = \frac{T_{SAM} \times F_{OSC} - 2}{8}$$

$$CONV = \left[\frac{T_{CONV} \times F_{OSC} - 3}{2 \times B}\right] - 1$$

where:

SAM = 1 to 7
CONV = 2 to 31
T_{SAM} is the sample time, in µsec (Tables 16 and 18)
T_{CONV} is the conversion time, in µsec (Tables 16 and 18)
F_{OSC} is the XTAL1 frequency, in MHz
B is the number of bits to be converted (8 or 10)

When the SAM and CONV values are known, write them to the AD_TIME register. Do not write to this register while a conversion is in progress; the results are unpredictable.

AC CHARACTERISTICS — A/D CONVERTER

Table 16. 10-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	– 40	+ 85	°C	
V_{CC}	Digital Supply Voltage	4.50	5.50	V	
V_{REF}	Analog Supply Voltage	4.50	5.50	V	2
T_{SAM}	Sample Time	1.0		µs	3
T_{CONV}	Conversion Time	10.0	20.0	µs	3
F_{OSC}	Oscillator Frequency	8	16	MHz	

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than + 0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 17. 10-bit Mode A/D Characteristics Over Specified Operating Conditions (1)

Parameter	Typical (3)	Min	Max	Units (2)	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	± 3	LSBs	
Full-scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Nonlinearity	1.0 ± 2.0		± 3	LSBs	
Differential Nonlinearity		– 0.75	+ 0.75	LSBs	
Channel-to-channel Matching	± 0.1	0	± 1	LSBs	
Repeatability	± 0.25	0		LSBs	

NOTES:
1. Testing is performed with V_{REF} = 5.12 V and F_{OSC} = 16 MHz.
2. An *LSB*, as used here, has a value of approximately 5 mV.
3. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC}$ = 5.5 V.
4. DC to 100 KHz.
5. Multiplexer break-before-make guaranteed.
6. Resistance from device pin, through internal multiplexer, to sample capacitor.
7. These values may be exceeded if the pin current is limited to ± 2mA.
8. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
9. All conversions were performed with processor in idle mode.

Table 17. 10-bit Mode A/D Characteristics Over Specified Operating Conditions (1) (Continued)

Parameter	Typical (3)	Min	Max	Units (2)	Notes
Temperature Coefficients: Offset Full-scale Differential Nonlinearity	 0.009 0.009 0.009			 LSB/C LSB/C LSB/C	
Off-isolation		– 60		dB	4, 5
Feedthrough	– 60			dB	4
V_{CC} Power Supply Rejection	– 60			dB	6
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		ANGND – 0.5	V_{REF} + 0.5	V	7, 8
Sampling Capacitor	3			pF	
DC Input Leakage	± 1.0	0	± 3	µA	

NOTES:
1. Testing is performed with V_{REF} = 5.12 V and F_{OSC} = 16 MHz.
2. An *LSB*, as used here, has a value of approximately 5 mV.
3. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC}$ = 5.5 V.
4. DC to 100 KHz.
5. Multiplexer break-before-make guaranteed.
6. Resistance from device pin, through internal multiplexer, to sample capacitor.
7. These values may be exceeded if the pin current is limited to ± 2mA.
8. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
9. All conversions were performed with processor in idle mode.

Table 18. 8-bit A/D Operating Conditions (1)

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	– 40	+ 85	°C	
V_{CC}	Digital Supply Voltage	4.50	5.50	V	
V_{REF}	Analog Supply Voltage	4.50	5.50	V	2
T_{SAM}	Sample Time	1.0		µs	3
T_{CONV}	Conversion Time	7.0	20.0	µs	3
F_{OSC}	Oscillator Frequency	8	16	MHz	

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than + 0.5 V because V_{REF} supplies both the resistor ladder and the analog portion of the converter and input port pins.
3. Program the AD_TIME register to meet the T_{SAM} and T_{CONV} specifications.

Table 19. 8-bit Mode A/D Characteristics Over Specified Operating Conditions (1)

Parameter	Typical (3)	Min	Max	Units (2)	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	± 1	LSBs	
Full-scale Error	± 0.5			LSBs	
Zero Offset Error	± 0.5			LSBs	
Nonlinearity		0	± 1	LSBs	
Differential Nonlinearity		– 0.5	+ 0.5	LSBs	
Channel-to-channel Matching		0	± 1	LSBs	
Repeatability	± 0.25	0		LSBs	
Temperature Coefficients: Offset Full-scale Differential Nonlinearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	
Off Isolation		– 60		dB	4, 5
Feedthrough	– 60			dB	4
V_{CC} Power Supply Rejection	– 60			dB	4
Input Series Resistance		750	1.2K	Ω	6
Voltage on Analog Input Pin		ANGND – 0.5	V_{REF} + 0.5	V	7, 8
Sampling Capacitor	3			pF	
DC Input Leakage	± 1	0	± 3	µA	

NOTES:
1. Testing is performed with V_{REF} = 5.12 V and F_{OSC} = 16 MHz.
2. An *LSB*, as used here, has a value of approximately 20 mV.
3. Typical values are based on a limited number of samples and are not guaranteed. Operating conditions for typical values are room temperature and $V_{REF} = V_{CC}$ = 5.5 V.
4. DC to 100 KHz.
5. Multiplexer break-before-make guaranteed.
6. Resistance from device pin, through internal multiplexer, to sample capacitor.
7. These values may be exceeded if the pin current is limited to ± 2mA.
8. Applying voltage beyond these specifications will degrade the accuracy of other channels being converted.
9. All conversions were performed with processor in idle mode.

OTPROM SPECIFICATIONS

Table 20. Programming Operating Conditions

Symbol	Description	Min	Max	Units	Notes
T_A	Ambient Temperature	20	30	°C	
V_{CC}	Supply Voltage During Programming	4.50	5.50	V	3
V_{REF}	Reference Supply Voltage During Programming	4.50	5.50	V	3
V_{PP}	Programming Voltage	12.25	12.75	V	2
V_{EA}	EA Pin Voltage	12.25	12.75	V	2
F_{OSC}	Oscillator Frequency During Auto and Slave Mode Programming	6	8	MHz	
	Oscillator Frequency During Run-Time Programming	6	12	MHz	

NOTES:
1. V_{CC} and V_{REF} should be at nominally the same voltage during programming.
2. If V_{PP} and V_{EA} exceed the maximum specification, the device may be damaged.
3. V_{SS} and ANGND should be at nominally the same potential (0 volts).
4. Load capacitance during auto and slave mode programming = 150 pF.

Table 21. AC OTPROM Programming Characteristics

Symbol	Description	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	PALE# Pulse Width	50		T_{OSC}
T_{PLPH}	PROG# Pulse Width (1)	50		T_{OSC}
T_{PHLL}	PROG# High to Next PALE# Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	PROG# High to Next PROG# Low	220		T_{OSC}
T_{LHPL}	PALE# High to PROG# Low	220		T_{OSC}
T_{PLDV}	PROG# Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	RESET# High to First PALE# Low	1100		T_{OSC}
T_{PHIL}	PROG# High to AINC# Low	0		T_{OSC}
T_{ILIH}	AINC# Pulse Width	240		T_{OSC}

NOTE:
1. This specification is for Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm explained in the User's Manual.

Table 21. AC OTPROM Programming Characteristics (Continued)

Symbol	Description	Min	Max	Units
T_{ILVH}	PVER Hold after AINC# Low	50		T_{OSC}
T_{ILPL}	AINC# Low to PROG# Low	170		T_{OSC}
T_{PHVL}	PROG# High to PVER Valid		220	T_{OSC}

NOTE:
1. This specification is for Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm explained in the User's Manual.

Table 22. DC OTPROM Programming Characteristics

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current (when programming)		100	mA

NOTE: Do not apply V_{PP} until V_{CC} is stable and within specifications and the oscillator/clock has stabiliized. Otherwise, the device may be damaged.

OTPROM PROGRAMMING WAVEFORMS

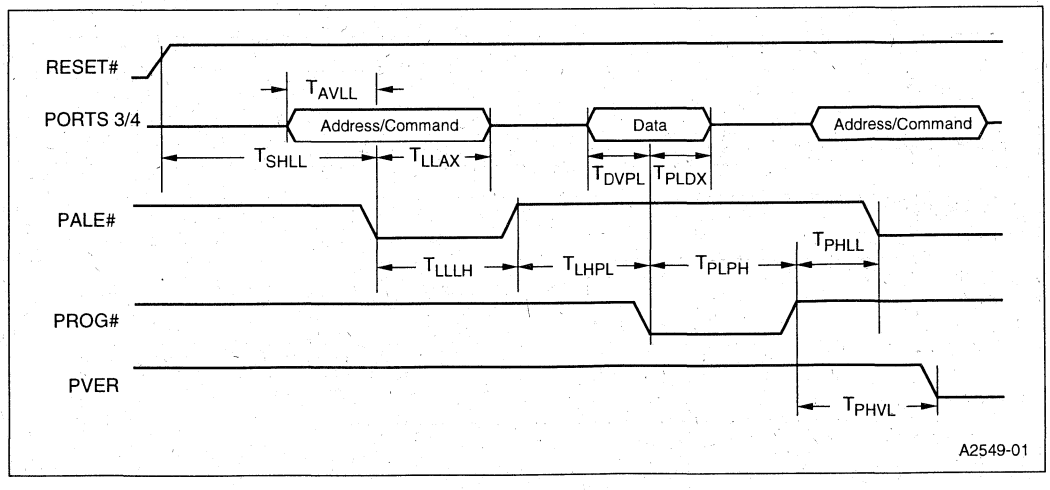


Figure 19. Slave Programming Mode Data Program Mode with Single Program Pulse

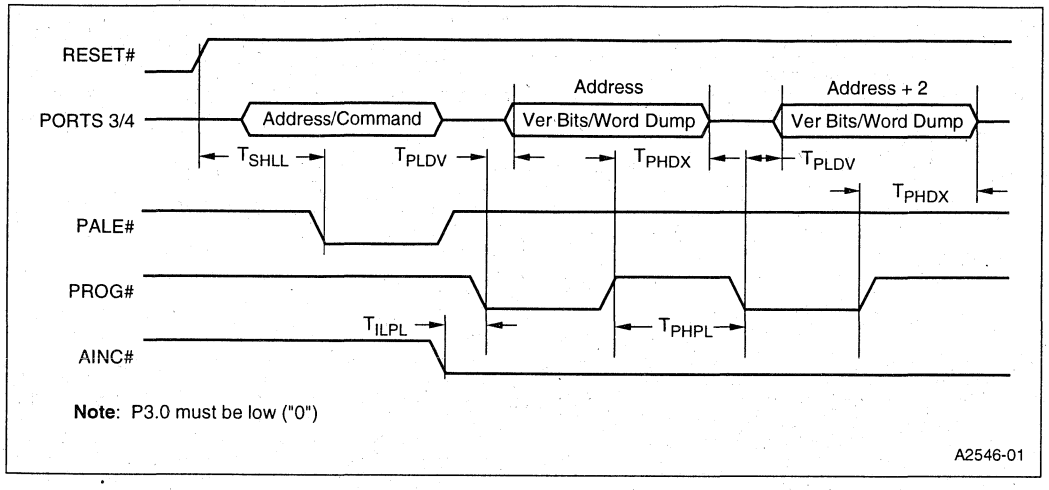


Figure 20. Slave Programming Mode in Word Dump with Autoincrement Timing

SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTOINCREMENT

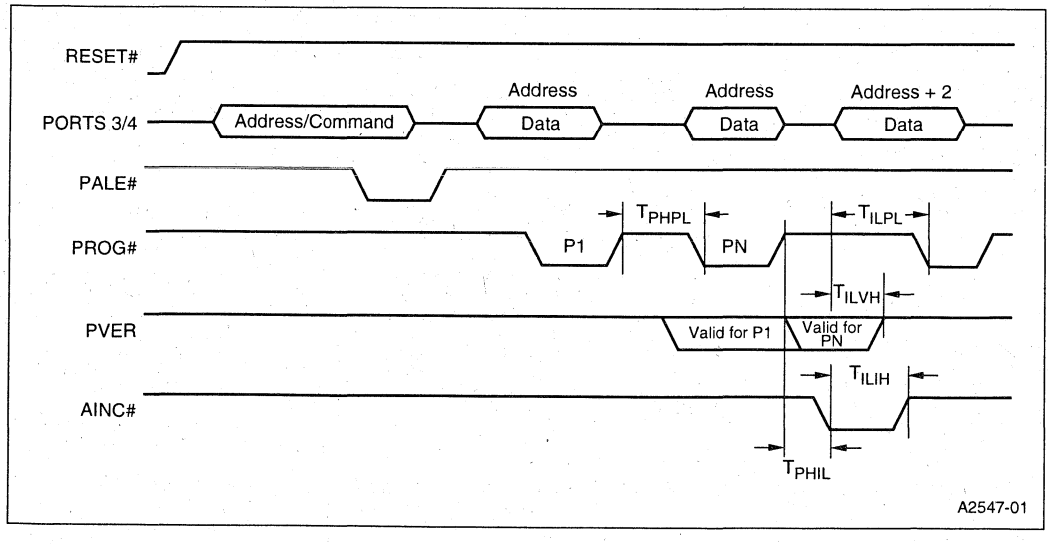


Figure 21. Slave Programming Mode in Data Program with Repeated Program Pulse and Autoincrement

8XC196MC/MD TO 8XC196MH DESIGN CONSIDERATIONS

The 8XC196MH is not pin compatible with the 8XC196MC or the 8XC196MD. Be aware that signal multiplexing sometimes differs between the 8XC196MH and the 8XC196MC/MD. For example, P2.7 is multiplexed with COMP3 on the 8XC196MC/MD and with SCLK1# and BCLK1 on the 8XC196MH.

DATA SHEET REVISION HISTORY

This is the initial publication of this data sheet (272543-001). Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

intel®

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The RUPI Family

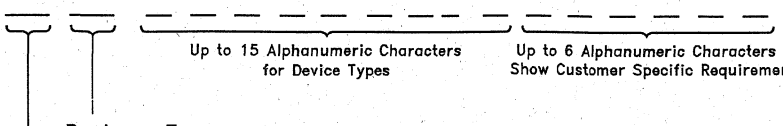
intel®

MCS®-51 and MCS®-96 Packaging Information

December 1996

Order Number: 272118-002

Intel Product Identification Codes



Package Type

A	–	Ceramic Pin Grid Array
C	–	Ceramic Dual In-Line Package
D	–	Cerdip Dual In-Line Package
KU	–	Plastic Quad Flatpack Package, Fine Pitch, Die Up
N	–	Plastic Leaded Chip Carrier
P	–	Plastic Dual In-Line Package
R	–	Ceramic Leadless Chip Carrier
S	–	Quad Flatpack Package
U	–	Plastic Dual In-Line Package (Shrink)

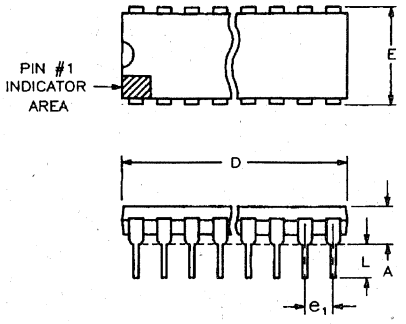
L	–	Indicates extended operating temperature range (−40°C to +85°C) express product with 160 ± 8 hrs. dynamic burn-in.
Q	–	Indicates commercial temperature range (0°C to 70°C) express product with 160 ± 8 hrs. dynamic burn-in
T	–	Indicates extended temperature range (−40°C to +85°C) express product without burn-in.

272118-12

EXAMPLES:

N80C196KR	PLCC, 16 MHz, Commercial Temperature Range
LN87C54	PLCC, 12 MHz, Extended Temperature Range (Express)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE (TYPE N)

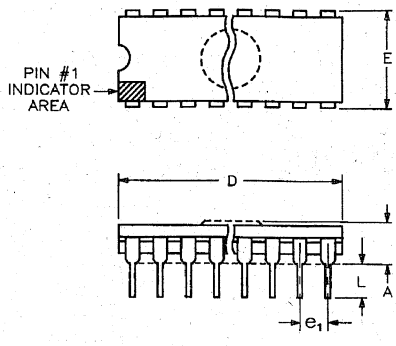


272118-1

Family: Plastic Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5	0.2
D	53	2.1
E	16	0.6
e_1	2.5	0.10
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

40-LEAD CERDIP DUAL IN-LINE PACKAGE (TYPE D)

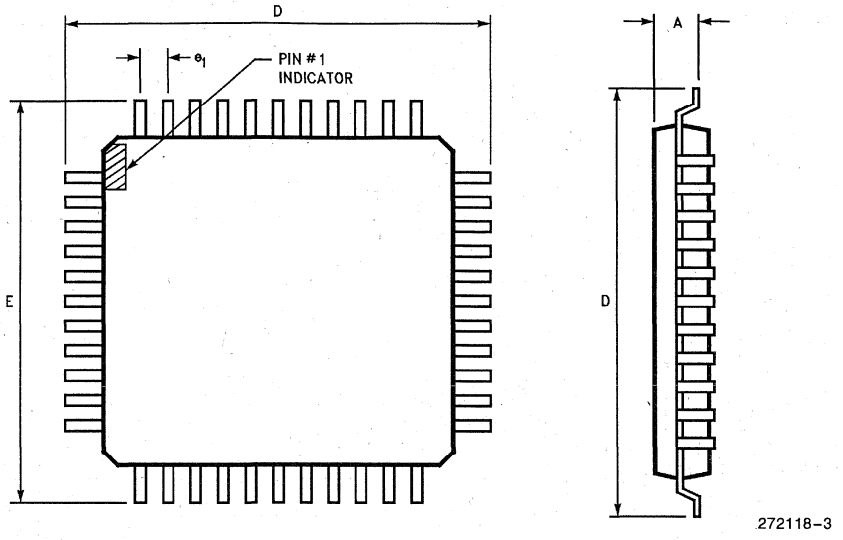


272118-2

Family: Cerdip Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5.8	0.2
D	53	2.1
E	16	0.6
e_1	2.5	0.10
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

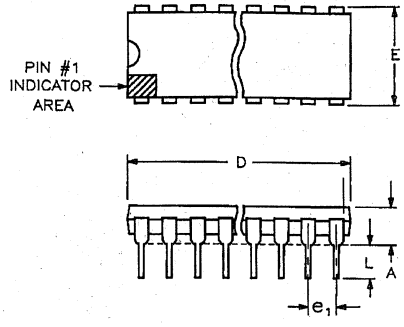
44-LEAD QUAD FLATPACK PACKAGE (TYPE S) VARIATION: SQUARE



Family: Quad Flatpack Package	
Symbol	**Millimeters Approx***
A	3
D	13
E	13
e_1	0.8

*For exact dimensions consult the Packaging Handbook (#240800).

48-LEAD PLASTIC DUAL IN-LINE PACKAGE (TYPE N)

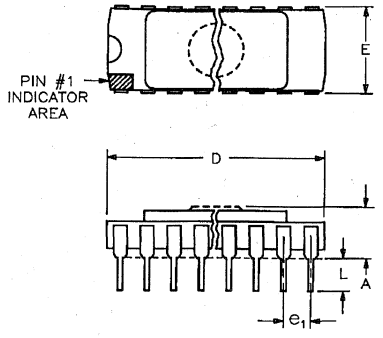


272118-4

Family: Plastic Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5	0.2
D	62	2.5
E	16	0.6
e_1	2.5	0.1
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

48-LEAD CERAMIC DUAL IN-LINE PACKAGE (TYPE C)

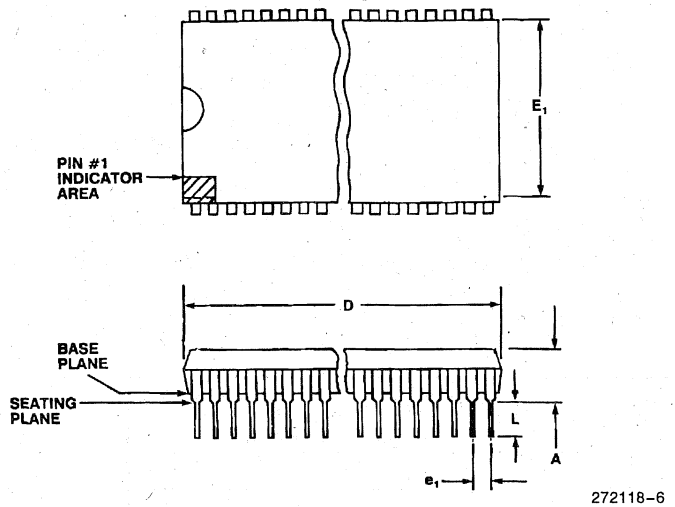


272118-5

Family: Ceramic Side Braze Dual In-Line		
Symbol	**Millimeters Approx***	**Inches Approx***
A	6(1)	0.2(1)
A	7(2)	0.3(2)
D	62	2.5
E	16	0.6
e_1	2.5	0.1
L	3	0.1

NOTES:
1. Solid LID
2. EPROM LID
*For exact dimensions consult the Packaging Handbook (#240800).

64-LEAD PLASTIC DUAL IN-LINE PACKAGE (SHRINK) (TYPE U)

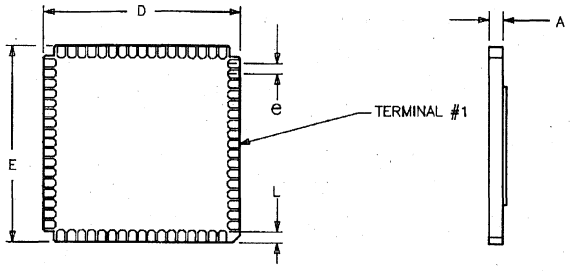


272118-6

Family: Plastic Dual In-Line Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	6	0.3
D	59	2.3
E_1	18	0.7
e_1	1.8	0.07
L	3	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

68-CERAMIC LEADLESS CHIP CARRIER (TYPE R) VARIATION: B

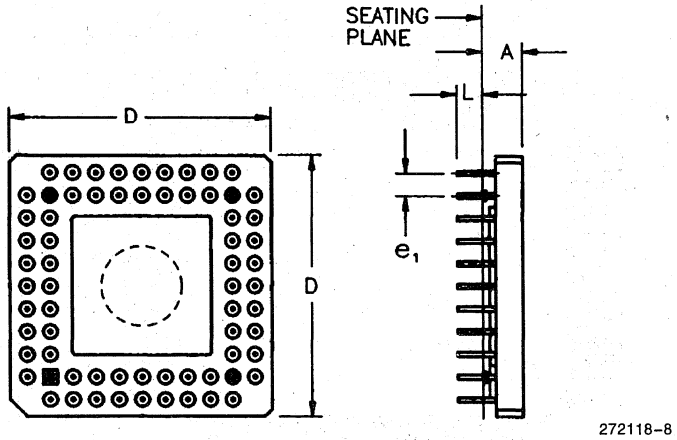


272118-7

Family: Ceramic Leadless Chip Carrier		
Symbol	**Millimeters Approx***	**Inches Approx***
A	3	0.1
D	25	1.0
E	25	1.0
e	1.3	0.05
L	1	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

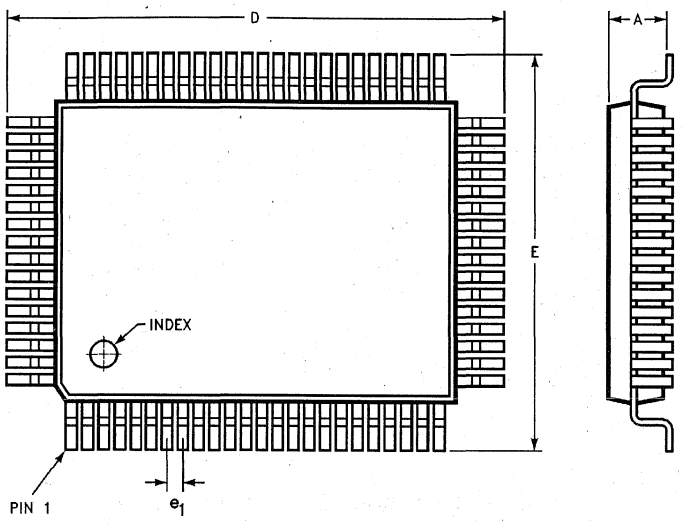
68-LEAD CERAMIC PIN GRID ARRAY PACKAGE (TYPE A)



Family: Ceramic Pin Grid Array Package		
Symbol	**Millimeters Approx***	**Inches Approx***
A	5	0.2
D	30	1.2
e_1	2.5	0.1
L	2	0.1

*For exact dimensions consult the Packaging Handbook (#240800).

80-LEAD QUAD FLATPACK PACKAGE (TYPE S) VARIATION: RECTANGULAR

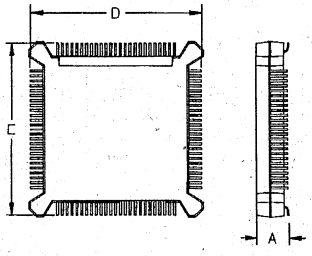


272118-9

Family: Quad Flatpack Package	
Symbol	**Millimeters Approx***
A	3
D	25
E	19
e_1	0.8

*For exact dimensions consult the Packaging Handbook (#240800).

100-LEAD PLASTIC QUAD FLATPACK PACKAGE (TYPE KU)

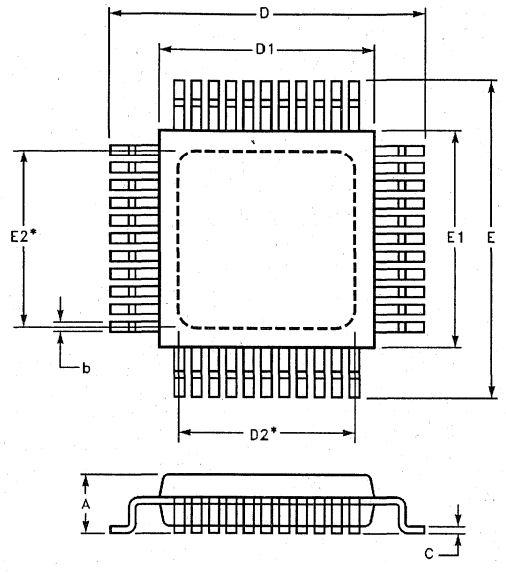


272118-10

Family: Plastic Quad Flatpack (0.025 Inch (0.635mm) Pitch)			
Symbol	**Description**	**Inches Approx***	**Millimeters Approx***
A	Package Height	0.2	5
D, E	Terminal Dimension	0.9	23

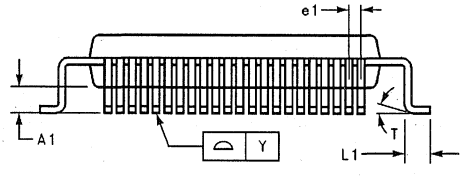
*For exact dimensions consult the Packaging Handbook (#240800).

100-LEAD SHRINK QUAD FLATPACK (SQFP) (TYPE SB)



272118-13

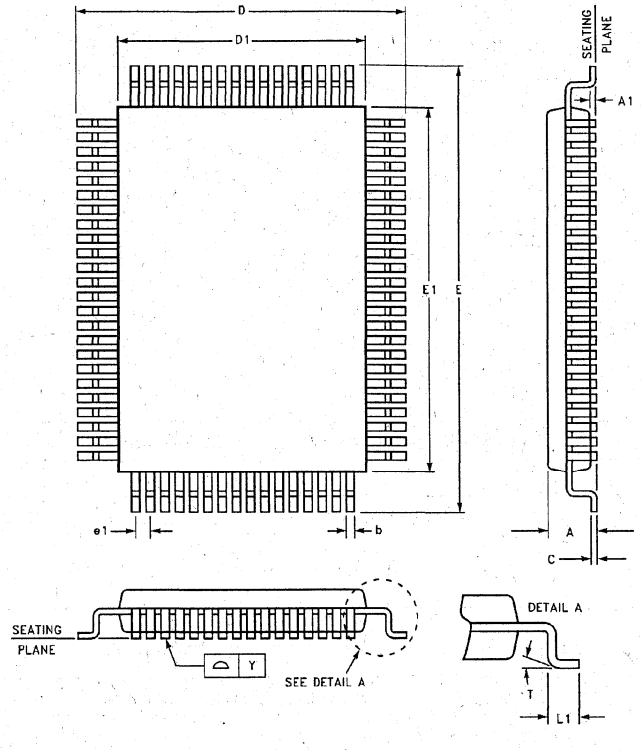
NOTE:
All dimensions in millimeters
*Optional Exposed Heatslug



272118-14

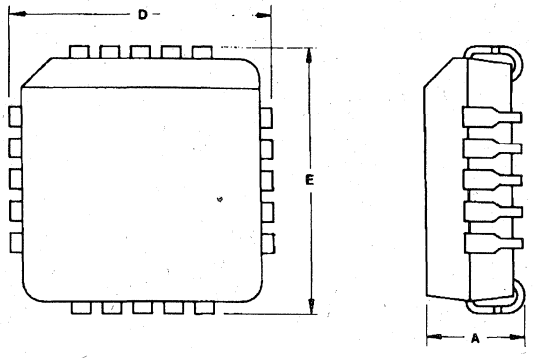
Shrink Quad Flatpack			
Symbol	**Description**	**Nom**	**Max**
N	Lead Count	100	
A	Overall Height		1.7
D_1	Package Body	14.0	
E_1	Package Body	14.0	

100-LEAD QUAD FLATPACK (QFP) (TYPE S) (RECTANGULAR)



Quad Flatpack (Rectangular Packages)			
Symbol	**Description**	**Nom**	**Max**
N	Lead Count	100	
A	Overall Height		3.15
D_1	Package Body	14.0	
E_1	Package Body	20.0	

44/52/68/84-LEAD PLASTIC LEADED CHIP CARRIER (TYPE N)



272118-11

Family: Plastic Leaded Chip Carrier—Square		
Symbol	44-Lead	
	Millimeters Approx*	Inches Approx*
A	5	0.2
D	18	0.7
E	18	0.7

Family: Plastic Leaded Chip Carrier—Square						
Symbol	Millimeters Approx*			Inches Approx*		
	68-Lead	52-Lead	84-Lead	68-Lead	52-Lead	84-Lead
A	5	5	5	0.2	0.2	0.2
D	26	21	31	1.0	0.8	1.2
E	26	21	31	1.0	0.8	1.2

*For exact dimensions consult the Packaging Handbook (#240800).

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CAN 82527 Controller

intel®

The RUPI-44 Family: Microcontroller with On-Chip Communication Controller

October 1988

Order Number: 296163-001

INTRODUCTION

The RUPI-44 family is designed for applications requiring local intelligence at remote nodes, and communication capability among these distributed nodes. The RUPI-44 integrates onto a single chip Intel's highest performance microcontroller, the 8051-core, with an intelligent and high performance Serial communication controller, called the Serial Interface Unit, or SIU. See Figure 1. This dual controller architecture allows complex control and high speed data communication functions to be realized cost effectively.

The RUPI-44 family consists of three pin compatible parts:

- 8344—8051 Microcontroller with SIU
- 8044—An 8344 with 4K bytes of on-chip ROM program memory
- 8744—An 8344 with 4K bytes of on-chip EPROM program memory

1.0 ARCHITECTURE OVERVIEW

The 8044's dual controller architecture enables the RUPI to perform complex control tasks and high speed communication in a distributed network environment.

The 8044 microcontroller is the 8051-core, and maintains complete software compatibility with it. The microcontroller contains a powerful CPU with on-chip peripherals, making it capable of serving sophisticated real-time control applications such as instrumentation, industrial control, and intelligent computer peripherals. The microcontroller features on-chip peripherals such as two 16-bit timer/counters and 5 source interrupt capability with programmable priority levels. The microcontroller's high performance CPU executes most instructions in 1 microsecond, and can perform an 8 × 8 multiply in 4 microseconds. The CPU features a Boolean processor that can perform operations on 256 directly addressable bits. 192 bytes of on-chip data RAM can be extended to 64K bytes externally. 4K bytes of on-chip program ROM can be extended to 64K bytes externally. The CPU and SIU run concurrently. See Figure 2.

The SIU is designed to perform serial communications with little or no CPU involvement. The SIU supports data rates up to 2.4 Mbps, externally clocked, and 375 Kbps self clocked (i.e., the data clock is recovered by an on-chip digital phase locked loop). SIU hardware supports the HDLC/SDLC protocol: zero bit insertion/deletion, address recognition, cyclic redundancy check, and frame number sequence check are automatically performed.

The SIU's Auto mode greatly reduces communication software overhead. The AUTO mode supports the SDLC Normal Response Mode, by performing secondary station responses in hardware without any CPU involvement. The Auto mode's interrupt control and frame sequence numbering capability eliminates software overhead normally required in conventional systems. By using the Auto mode, the CPU is free to concentrate on real time control of the application.

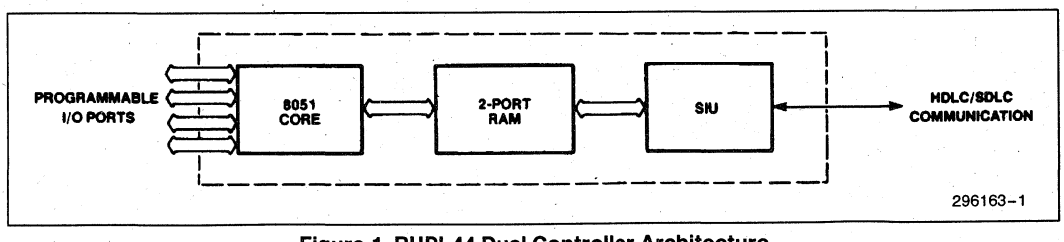


Figure 1. RUPI-44 Dual Controller Architecture

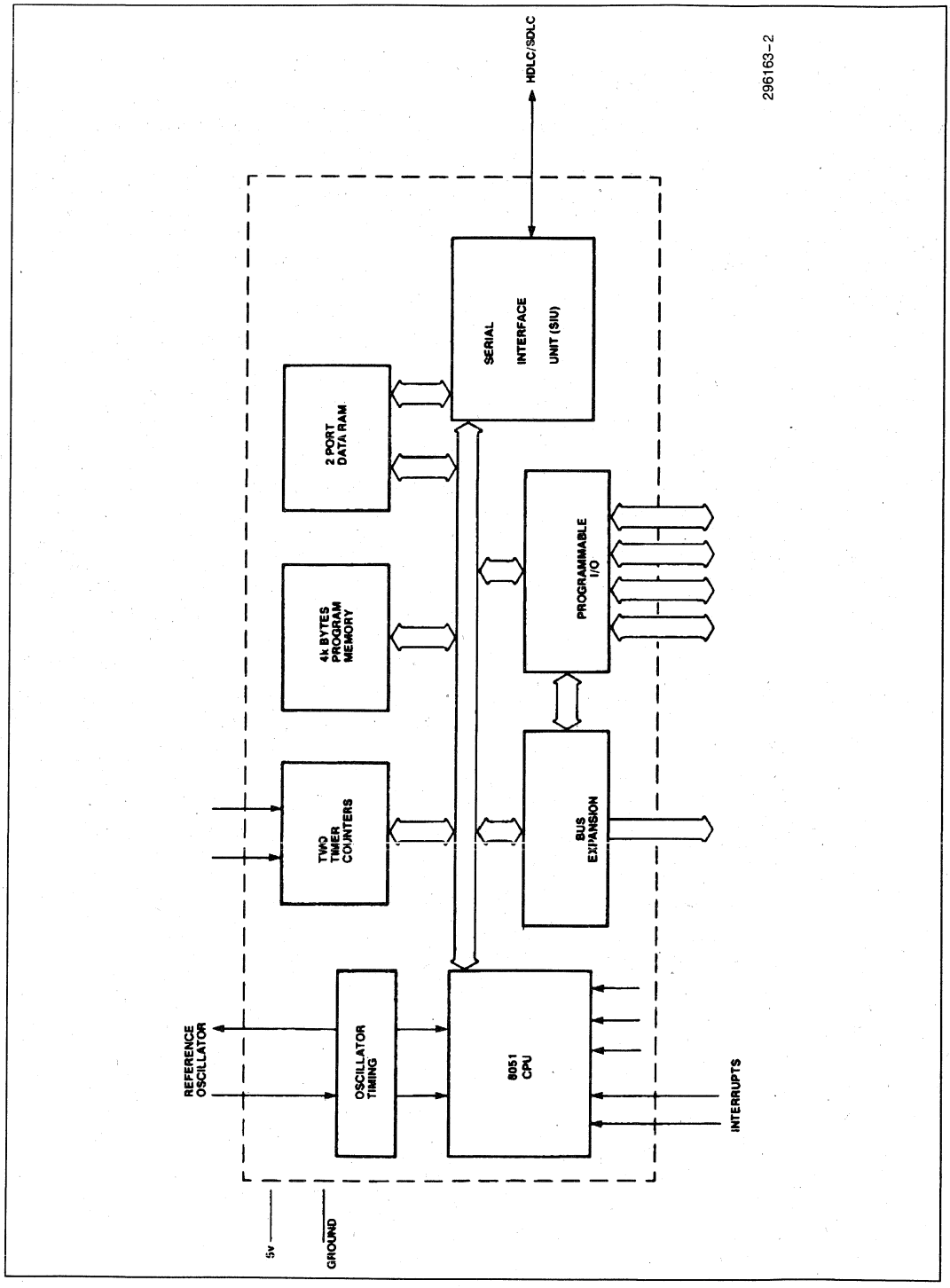


Figure 2. Simplified 8044 Block Diagram

2.0 THE HDLC/SDLC PROTOCOLS

2.1 HDLC/SDLC Advantages over Async

The High Level Data Link Control, HDLC, is a standard communication link control established by the International Standards Organization (ISO). SDLC is a subset of HDLC.

HDLC and SDLC are both well recognized standard serial protocols. The Synchronous Data Link Control, SDLC, is an IBM standard communication protocol. IBM originally developed SDLC to provide efficient, reliable and simple communication between terminals and computers.

The major advantages of SDLC/HDLC over Asynchronous communications protocol (Async):

- SIMPLE: Data Transparency
- EFFICIENT: Well Defined Message-Level Operation
- RELIABLE: Frame Check Sequence and Frame Numbering

The SDLC reduces system complexity. HDLC/SDLC are "data transparent" protocols. Data transparency means that an arbitrary data stream can be sent without concern that some of the data could be mistaken for a protocol controller. Data transparency relieves the communication controller having to detect special characters.

SDLC/HDLC provides more data throughout than Async. SDLC/HDLC runs at Message-level Operation which transmits multiple bytes within the frame, whereas Async is based on character-level operation. Async transmits or receives a character at a time. Since Async requires start and stop bits in every transmission, there is a considerable waste of overhead compared to SDLC/HDLC.

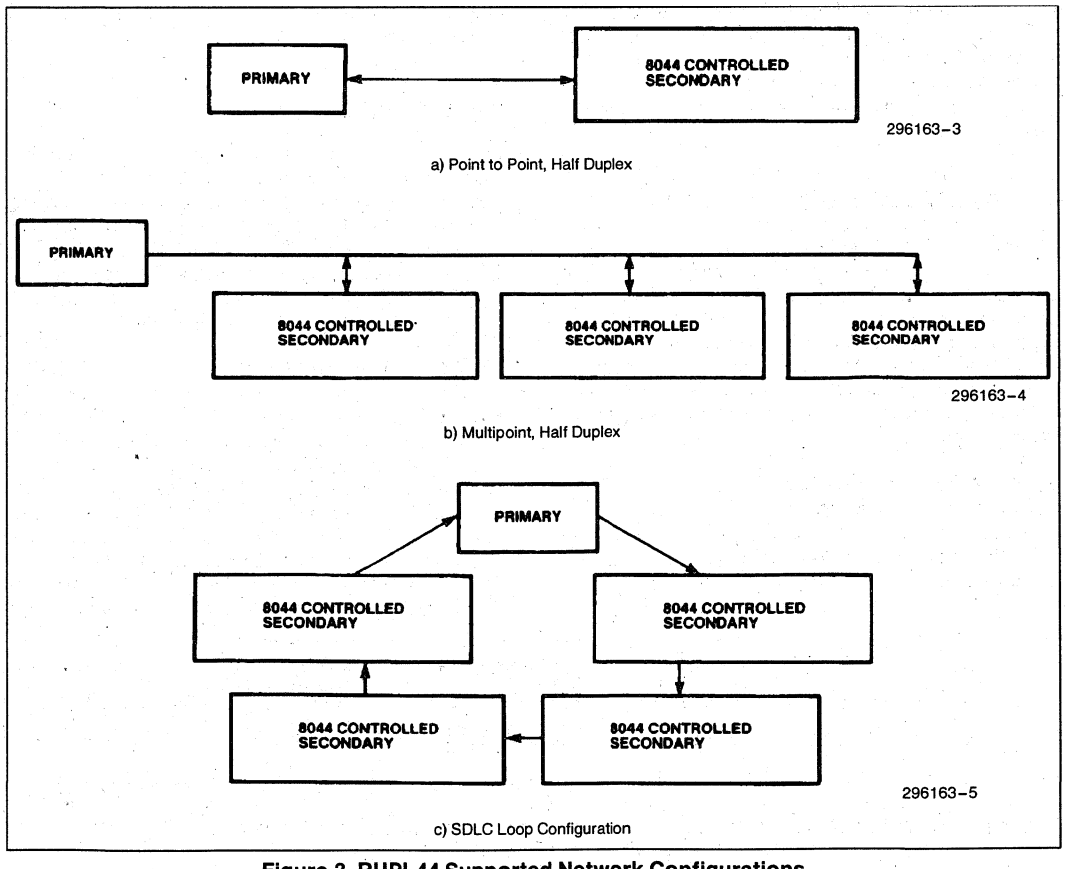


Figure 3. RUPI-44 Supported Network Configurations

Due to SDLC/HDLC's well delineated field (see Figure 4) the CPU does not have to interpret character by character to determine control field and information field. In the case of Async, CPU must look at each character to interpret what it means. The practical advantage of such feature is straight forward use of DMA for information transfer.

In addition, SDLC/HDLC further improves Data throughput using implied Acknowledgement of transferred information. A station using SDLC/HDLC may acknowledge previously received information while transmitting different information in the same frame. In addition, up to 7 messages may be outstanding before an acknowledgement is required.

The HDLC/SDLC protocol can be used to realize reliable data links. Reliable Data transmission is ensured at the bit level by sending a frame check sequence, cyclic redudancy checking, within the frame. Reliable frame transmission is ensured by sending a frame number identification with each frame. This means that a receiver can sequentially count received frames and at any time infer what the number of the next frame to be received should be. More important, it provides a means for the receiver to identify to the sender some particular frame that it wishes to have resent because of errors.

2.2 HDLC/SDLC Networks

In both the HDLC and SDLC line protocols a (Master) primary station controls the overall network (data link) and issues commands to the secondary (Slave) stations. The latter complies with instructions and responds by sending appropriate responses. Whenever a transmitting station must end transmission prematurely, it sends an abort character. Upon detecting an abort character, a receiving station ignores the transmission block called a frame.

RUPI-44 supported HDLC/SDLC network configurations are point to point (half duplex) multipoint (half duplex), and loop. In the loop configuration the stations themselves act as repeaters, so that long links can be easily realized, see Figure 3.

2.3 Frames

An HDLC/SDLC frame consists of five basic fields: Flag, Address, Control, Data and Error Detection. A frame is bounded by flags—opening and closing flags. An address field is 8 bits wide in SDLC, extendable to 2 or more bytes in HDLC. The control field is also 8 bits wide, extendable to two bytes in HDLC. The SDLC data field or information field may be any number of bytes. The HDLC data field may or may not be on an 8 bit boundary. A powerful error detection code called Frame Check Sequence contains the calculated CRC (Cycle Redundancy Code) for all the bits between the flags. See Figure 4.

In HDLC and SDLC are three types of frames; an Information Frame is used to transfer data, a Supervisory Frame is used for control purposes, and a Nonsequenced Frame is used for initialization and control of the secondary stations.

For a more detailed discussion of higher level protocol functions interested readers may refer to the references listed in Section 2.6.

2.4 Zero Bit Insertion

In data communications, it is desirable to transmit data which can be of arbitrary content. Arbitrary data transmission requires that the data field cannot contain characters which are defined to assist the transmission protocol (like opening flag in HDLC/SDLC communications). This property is referred to as "data transparency". In HDLC/SDLC, this code transparency is made possible by Zero Bit Insertion (ZBI).

The flag has a unique bit pattern: 01111110 (7E HEX). To eliminate the possibility of the data field containing a 7E HEX pattern, a bit stuffing technique called Zero Bit Insertion is used. This technique specifies that during transmission, a binary 0 be inserted by the transmitter after any succession of five contiguous binary 1's. This will ensure that no pattern of 0 1 1 1 1 1 1 0 is ever transmitted between flags. On the receiving side, after receiving the flag, the receiver hardware automatically deletes any 0 following five consecutive 1's. The 8044 performs zero bit insertion and deletion automatically.

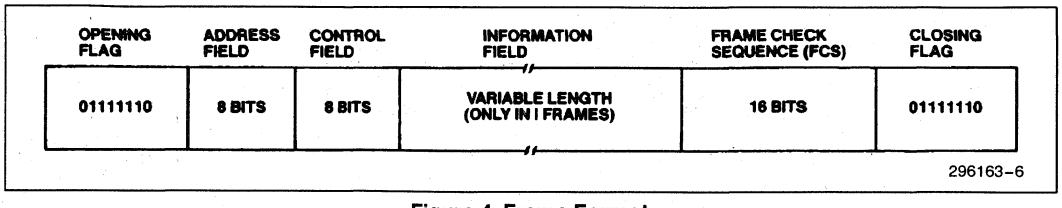


Figure 4. Frame Format

2.5 Non-return to Zero Inverted (NR21)

NRZI is a method of clock and data encoding that is well suited to the HDLC/SDLC protocol. It allows HDLC/SDLC protocols to be used with low cost asynchronous modems. NRZI coding is done at the transmitter to enable clock recovery from the data at the receiver terminal by using standard digital phase locked loop (DPLL) techniques. NRZI coding specifies that the signal condition does not change for transmitting a 1, while a 0 causes a change of state. NRZI coding ensures that an active data line will have a transition at least every 5-bit times (recall Zero Bit Insertion), while contiguous 0's will cause a change of state. Thus, ZBI and NRZI encoding makes it possible for the 8044's on-chip DPLL to recover a receive clock (from received data) synchronized to the received data and at the same time ensure data transparency.

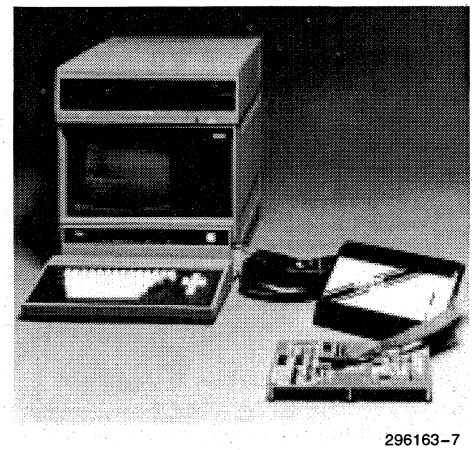
2.6 References

1. *IBM Synchronous Data Link Control General Information GA27-3093-2 File No. GENL-09.*
2. *Standard Network Access Protocol Specification, DATAPAC Trans-Canada Telephone System CCG111.*
3. *IBM 3650 Retail Store System Loop Interface OEM Information, IBM, GA27-3098-0.*
4. *Guidebook to Data Communications, Training Manual, Hewlett-Packard 5955-1715.*
5. *"Serial Backplane Suits Multiprocessor Architectures", Mike Webb, Computer Design, July 1984, pp. 85–96.*
6. *"Serial Bus Simplifies Distributed Control", P.D. MacWilliams, Control Engineering, June 1984, pp. 101–104.*
7. *"Chips Support Two Local Area Networks", Bob Dahlberg, Computer Design, May 1984, pp. 107–114.*
8. *"Build a VLSI-based Workstation for the Ethernet Environment", Mike Webb, EDN, 23 February 1984, pp. 297–307.*
9. *"Networking With the 8044", Young Sohn & Charles Gopen, Digital Design, May 1984, pp. 136–137.*

3.0 RUPI-44 DESIGN SUPPORT

3.1 Design Tool Support

A critical design consideration is time to market. Intel provides a sophisticated set of design tools to speed hardware and software development time of 8044 based products. These include ICE-44, ASM-51, PL/M-51, and EMV-44.



296163-7

Figure 5. RUPI-44 Development Support Configuration Intellec System, ICE™-44 Buffer Box, and ICE-44 Module Plugged into a User Prototype Board

A primary tool is the 8044 In Circuit Emulator, called ICE-44. See Figure 5. In conjunction with Intel's Intellec Microprocessor Development System, the ICE-44 emulator allows hardware and software development to proceed interactively. This approach is more effective than the traditional method of independent hardware and software development followed by system integration. With the ICE-44 module, prototype hardware can be added to the system as it is designed. Software and hardware integration occurs while the product is being developed.

The ICE-44 emulator assists four stages of development:

1) Software Debugging

   It can be operated without being connected to the user's system before any of the user's hardware is available. In this stage ICE-44 debugging capabilities can be used in conjunction with the Intellec text editor and 8044 macroassembler to facilitate program development.

2) Hardware Development

   The ICE-44 module's precise emulation characteristics and full-speed program RAM make it a valuable tool for debugging hardware, including the time-critical SDLC serial port, parallel port, and timer interfaces.

3) System Integration

Integration of software and hardware can begin when any functional element of the user system hardware is connected to the 8044 socket. As each section of the user's hardware is completed, it is added to the prototype. Thus, each section of the hardware and software is system tested in real-time operation as it becomes available.

4) System Test

When the user's prototype is complete, it is tested with the final version of the user system software. The ICE-44 module is then used for real-time emulation of the 8044 to debug the system as a completed unit.

The final product verification test may be performed using the 8744 EPROM version of the 8044 microcomputer. Thus, the ICE-44 module provides the user with the ability to debug a prototype or production system at any stage in its development.

A conversion kit, ICE-44 CON, is available to upgrade an ICE-51 module to ICE-44.

Intel's ASM-51 Assembler supports the 8044 special function registers and assembly program development. PL/M-51 provides designers with a high level language for the 8044. Programming in PL/M can greatly reduce development time, and ensure quick time to market.

These tools have recently been expanded with the addition of the EMV-44CON. This conversion kit allows you to convert an EMV-51 into an EMV-44 emulation vehicle. The resultant low cost emulator is designed for use with an iPDS Personal Development System, which also supports the ASM-51 assembler and PL/M-51. See Figure 6.

Emulation support is similar to the ICE-44 with support for Software and Hardware Development, System

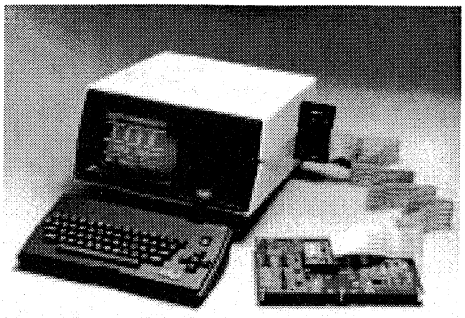


Figure 6. RUPI-44 iPDS Personal Development System, EMV-44 Buffer Box, and EMV-44 Module Plugged into a User Prototype Board

Integration, and System Test. The iPDS's rugged portability and ease of use also make it an ideal system for production tests and field service of your finished design. In addition, the iPDS offers EPROM programming module for the 8744, and direct communications with the 8044-based BITBUS via an optional iSBX-344 distributed control module.

3.2 8051 Workshop

Intel provides 8051 training to its customers through the 5-day 8051 workshop. Familiarity with the 8051 and 8044 is achieved through a combination of lecture and laboratory exercises.

For designers not familiar with the 8051, the workshop is an effective way to become proficient with the 8051 architecture and capabilities.

intel®

8044 Architecture

October 1988

Order Number: 296164-001

GENERAL

The 8044 is based on the 8051 core. The 8044 replaces the 8051's serial port with an intelligent HDLC/SDLC controller called the Serial Interface or SIU. Thus the differences between the two result from the 8044's increased on-chip RAM (192 bytes) and additional special function registers necessary to control the SIU. Aside from the increased memory, the SIU itself, and differences in 5 pins (for the serial port), the 8044 and 8051 are compatible.

This chapter describes the differences between the 8044 and 8051. Information pertaining to the 8051 core, eg. instruction set, port operation, EPROM programming, etc. is located in the 8051 sections of this manual.

A block diagram of the 8044 is shown in Figure 1. The pinpoint is shown on the inside front cover.

1.0 MEMORY ORGANIZATION OVERVIEW

The 8044 maintains separate address spaces for Program Memory and Data Memory. The Program Memory can be up to 64K bytes long, of which the lowest 4K bytes are in the on-chip ROM.

If the $\overline{EA}$ pin is held high, the 8044 executes out of internal ROM unlwess the Program Counter exceeds 0FFFH. Fetches from locations 1000H through FFFFH are directed to external Program Memory.

If the $\overline{EA}$ pin is held low, the 8044 fetches all instructions from external Program Memory.

The Data Memory consists of 192 bytes of on-chip RAM, plus 35 Special Function Registers, in addition to which the device is capable of accessing up to 64K bytes of external data memory.

The Program Memory uses 16-bit addresses. The external Data Memory can use either 8-bit or 16-bit addresses. The internal Data Memory uses 8-bit addresses, which provide a 256-location address space. The lower 192 addresses access the on-chip RAM. The Special Function Registers occupy various locations in the upper 128 bytes of the same address space.

The lowest 32 bytes in the internal RAM (locations 00 through 1FH) are divided into 4 banks of registers, each bank consisting of 8 bytes. Any one of these banks can be selected to be the "working registers" of the CPU, and can be accessed by a 3-bit address in the same byte as the opcode of an instruction. Thus, a large number of instructions are one-byte instructions.

The next higher 16 bytes of the internal RAM (locations 20H through 2FH) have individually addressable bits. These are provided for use as software flags or for one-bit (Boolean) processing. This bit-addressing capability is an important feature of the 8044. In addition to the 128 individually addressable bits in RAM, twelve of the Special Function Registers also have individually addressable bits.

A memory map is shown in Figure 2.

1.1 Special Function Registers

The Special Function Registers are as follows:

*	ACC	Accumulator (A Register)
*	B	B Register
*	PSW	Program Status Word
	SP	Stack Pointer
	DPTR	Data Pointer (consisting of DPH AND DPL)
*	P0	Port 0
*	P1	Port 1
*	P2	Port 2
*	P3	Port 3
*	IP	Interrupt Priority
*	IE	Interrupt Enable
	TMOD	Timer/Counter Mode
*	TCON	Timer/Counter Control
	TH0	Timer/Counter 0 (high byte)
	TL0	Timer/Counter 0 (low byte)
	TH1	Timer/Counter 1 (high byte)
	TL1	Timer/Counter 1 (low byte)
	SMD	Serial Mode
*	STS	Status/Command
*	NSNR	Send/Receive Count
	STAD	Station Address
	TBS	Transmit Buffer Start Address
	TBL	Transmit Buffer Length
	TCB	Transmit Control Byte
	RBS	Receive Buffer Start Address
	RBL	Receive Buffer Length
	RFL	Received Field Length
	RCB	Received Control Byte
	DMA CNT	DMA Count
	FIFO	FIFO (three bytes)
	SIUST	SIU State Counter
	PCON	Power Control

The registers marked with * are both byte- and bit-addressable.

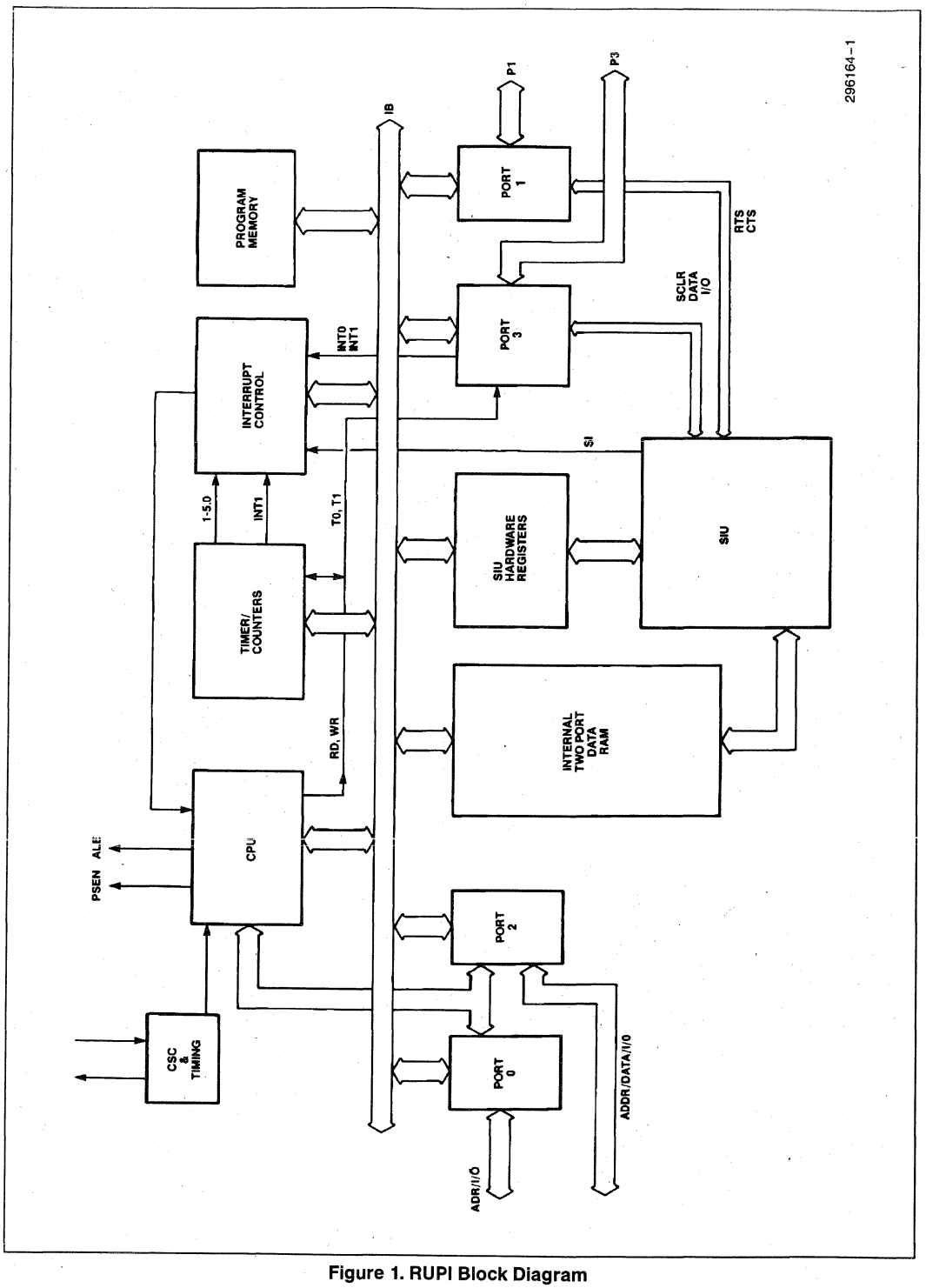


Figure 1. RUPI Block Diagram

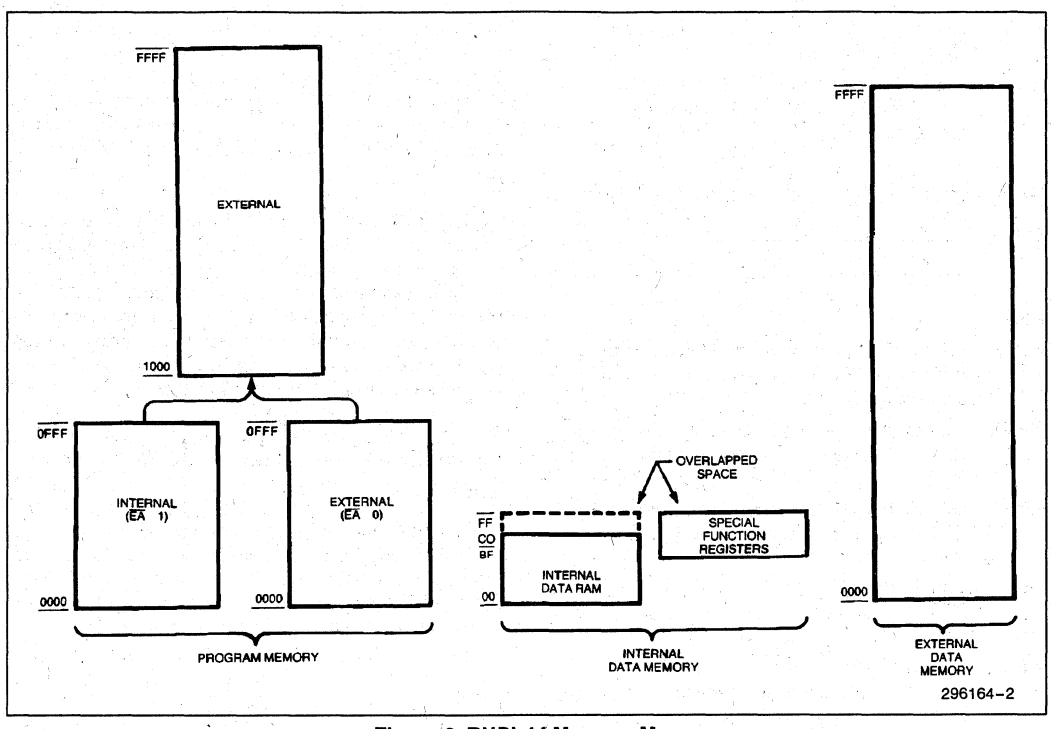


Figure 2. RUPI-44 Memory Map

Stack Pointer

The Stack Pointer is 8 bits wide. The stack can reside anywhere in the 192 bytes of on-chip RAM. When the 8044 is reset, the stack pointer is initialized to 07H. When executing a PUSH or a CALL, the stack pointer is incremented before data is stored, so the stack would begin at location 08H.

1.2 Interrupt Control Registers

The Interrupt Request Flags are as listed below:

Source	*Request Flag*	*Location*
External Interrupt 0	$\overline{INT0}$, if IT0 = 0	P3.2
	IE0, if IT0 = 1	TCON.1
Timer 0 Overflow	TF0	TCON.5
External Interrupt 1	$\overline{INT1}$, if IT1 = 0	P3.3
	IE1, if IT1 = 1	TCON.3
Timer 1 Overflow	TF1	TCON.7
Serial Interface Unit	SI	STS.4

External Interrupt control bits IT0 and IT1 are in TCON.0 and TCON.2, respectively. Reset leaves all flags inactive, with IT0 and IT1 cleared.

All the interrupt flags can be set or cleared by software, with the same effect as by hardware.

The Enable and Priority Control Registers are shown below. All of these control bits are set or cleared by software. All are cleared by reset.

IE: Interrupt Enable Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	EA	X	X	ES	ET1	EX1	ET0	EX0

where:

- EA disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
- ES enables or disables the Serial Interface Unit interrupt. If ES = 0, the Serial Interface Unit interrupt is disabled.
- ET1 enables or disables the Timer 1 Overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.

- EX1 enables or disables External Interrupt 1. If EX1 = 0, External Interrupt 1 is disabled.
- ET0 enables or disables the Timer 0 Overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.

IP: Interrupt Priority Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	X	X	X	PS	PT1	PX1	PT0	PX0

where:

- PS defines the Serial Interface Unit interrupt priority level. PS = 1 programs it to the higher priority level.
- PT1 defines the Timer 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.
- PX1 defines the External Interrupt priority level. PX1 = 1 programs it to the higher priority level.
- PT0 defines the Timer 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
- PX0 defines the External Interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.

2.0 MEMORY ORGANIZATION DETAILS

In the 8044 family the memory is organized over three address spaces and the program counter. The memory spaces shown in Figure 2 are the:

- 64K-byte Program Memory address space
- 64K-byte External Data Memory address space
- 320-byte Internal Data Memory address space

The 16-bit Program Counter register provides the 8044 with its 64K addressing capabilities. The Program Counter allows the user to execute calls and branches to any location within the Program Memory space. There are no instructions that permit program execution to move from the Program Memory space to any of the data memory spaces.

In the 8044 and 8744 the lower 4K of the 64K Program Memory address space is filled by internal ROM and EPROM, respectively. By tying the $\overline{EA}$ pin high, the processor can be forced to fetch from the internal ROM/EPROM for Program Memory addresses 0 through 4K. Bus expansion for accessing Program Memory beyond 4K is automatic since external instruction fetches occur automatically when the Program Counter increases above 4095. If the $\overline{EA}$ pin is tied low all Program Memory fetches are from external memory. The execution speed of the 8044 is the same regardless of whether fetches are from internal or external Program Memory. If all program storage is on-chip, byte location 4095 should be left vacant to prevent an undesired prefetch from external Program Memory address 4096.

Certain locations in Program Memory are reserved for specific programs. Locations 0000 through 0002 are reserved for the initialization program. Following reset, the CPU always begins execution at location 0000. Locations 0003 through 0042 are reserved for the five interrupt-request service programs. Each resource that can request an interrupt requires that its service program be stored at its reserved location.

The 64K-byte External Data Memory address space is automatically accessed when the MOVX instruction is executed.

Functionally the Internal Data Memory is the most flexible of the address spaces. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address space and a 128-byte Special Function Register address space as shown in Figure 3.

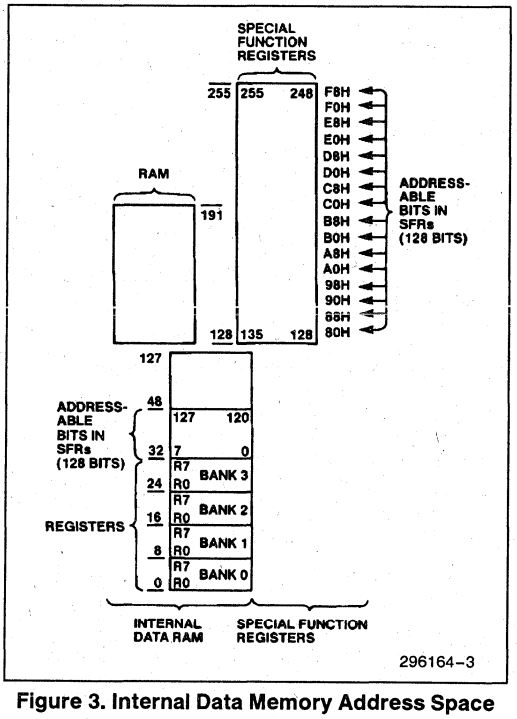


Figure 3. Internal Data Memory Address Space

The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit locations of the on-chip RAM are accessible through Direct Addressing. These bits reside in Internal Data RAM at byte locations 32 through 47. Currently locations 0 through 191 of the Internal Data RAM address space are filled with on-chip RAM.

The stack depth is limited only by the available Internal Data RAM, thanks to an 8-bit reloadable Stack Pointer. The stack is used for storing the Program Counter during subroutine calls and may be used for passing parameters. Any byte of Internal Data RAM or Special Function Register accessible though Direct Addressing can be pushed/popped.

The Special Function Register address space is 128 to 255. All registers except the Program Counter and the four 8-Register Banks reside here. Memory mapping the Special Function Registers allows them to be accessed as easily as internal RAM. As such, they can be operated on by most instructions. In the overlapping memory space (address 128-191), indirect addressing is used to access RAM, and direct addressing is used to access the SFR's. The SFR's at addresses 192–255 are also accessed using direct addressing. The Special Function Registers are listed in Figure 4. Their mapping in the Special Function Register address space is shown in Figures 5 and 6.

Performing a read from a location of the Internal Data memory where neither a byte of Internal Data RAM (i.e., RAM addresses 192-255) nor a Special Function Register exists will access data of indeterminable value.

Architecturally, each memory space is a linear sequence of 8-bit wide bytes. By Intel convention the storage of multi-byte address and data operands in program and data memories is the least significant byte at the low-order address and the most significant byte at the high-order address. Within byte X, the most significant bit is represented by X.7 while the least significant bit is X.0. Any deviation from these conventions will be explicitly stated in the text.

2.1 Operand Addressing

There are five methods of addressing source operands. They are Register Addressing, Direct Addressing, Register-Indirect Addressing, Immediate Addressing

ARITHMETIC REGISTERS:
Accumulator*, B register*,
Program Status Word*
POINTERS:
Stack Pointer, Data Pointer (high & low)
PARALLEL I/O PORTS:
Port 3*, Port 2*, Port 1*, Port 0*
INTERRUPT SYSTEM:
Interrupt Priority Control*,
Interrupt Enable Control*
TIMERS:
Timer Mode, Timer Control*, Timer 1 (high & low), Timer 0 (high & low)
SERIAL INTERFACE UNIT:
Transmit Buffer Start,
Transmit Buffer Length,
Transmit Control Byte,
Send Count Receive Count*,
DMA Count,
Station Address
Receive Field Length
Receive Buffer Start
Receive Buffer Length
Receive Control Byte,
Serial Mode,
Status Register.*

***Bits in these registers are bit addressable.**

Figure 4. Special Function Registers

ARITHMETIC REGISTERS:
Accumulator*, B register*,
Program Status Word*
POINTERS:
Stack Pointer, Data Pointer (high & low)
PARALLEL I/O PORTS:
Port 3*, Port 2*, Port 1*, Port 0*
INTERRUPT SYSTEM:
Interrupt Priority Control*,
Interrupt Enable Control*
TIMERS:
Timer Mode, Timer Control*, Timer 1 (high & low), Timer 0 (high & low)
SERIAL INTERFACE UNIT:
Serial Mode, Status/Command*,
Send/Receive Count*, Station Address,
Transmit Buffer Start Address,
Transmit Buffer Length,
Transmit Control Byte,
Receive Buffer Start Address,
Receive Buffer Length,
Receive Field Length,
Receive Control Byte,
DMA Count,
FIFO (three bytes),
SIU Controller State Counter

***Bits in these registers are bit-addressable.**

Figure 5. Mapping of Special Function Registers

and Base-Register-plus Index-Register-Indirect Addressing. The first three of these methods can also be used to address a destination operand. Since operations in the 8044 require 0 (NOP only), 1, 2, 3 or 4 operands, these five addressing methods are used in combinations to provide the 8044 with its 21 addressing modes.

Most instructions have a "destination, source" field that specifies the data type, addressing methods and operands involved. For operations other than moves, the destination operand is also a source operand. For example, in "subtract-with-borrow A,#5" the A register receives the result of the value in register A minus 5, minus C.

Most operations involve operands that are located in Internal Data Memory. The selection of the Program Memory space or External Data Memory space for a second operand is determined by the operation mnemonic unless it is an immediate operand. The subset of the Internal Data Memory being addressed is determined by the addressing method and address value. For example, the Special Function Registers can be accessed only through Direct Addressing with an address of 128-255. A summary of the operand addressing methods is shown in Figure 6. The following paragraphs describe the five addressing methods.

2.2 Register Addressing

Register Addressing permits access to the eight registers (R7-R0) of the selected Register Bank (RB). One of the four 8-Register Banks is selected by a two-bit field in the PSW. The registers may also be accessed through Direct Addressing and Register-Indirect Addressing, since the four Register Banks are mapped into the lowest 32 bytes of internal Data RAM as shown in Figures 9 and 10. Other Internal Data Memory locations that are addressed as registers are A, B, C, AB and DPTR.

2.3 Direct Addressing

Direct Addressing provides the only means of accessing the memory-mapped byte-wide Special Function Registers and memory mapped bits within the Special Function Registers and Internal Data RAM. Direct Addressing of bytes may also be used to access the lower 128 bytes of Internal Data RAM. Direct Addressing of bits gains access to a 128 bit subset of the Special Function Registers as shown in Figures 5, 6, 9, and 10.

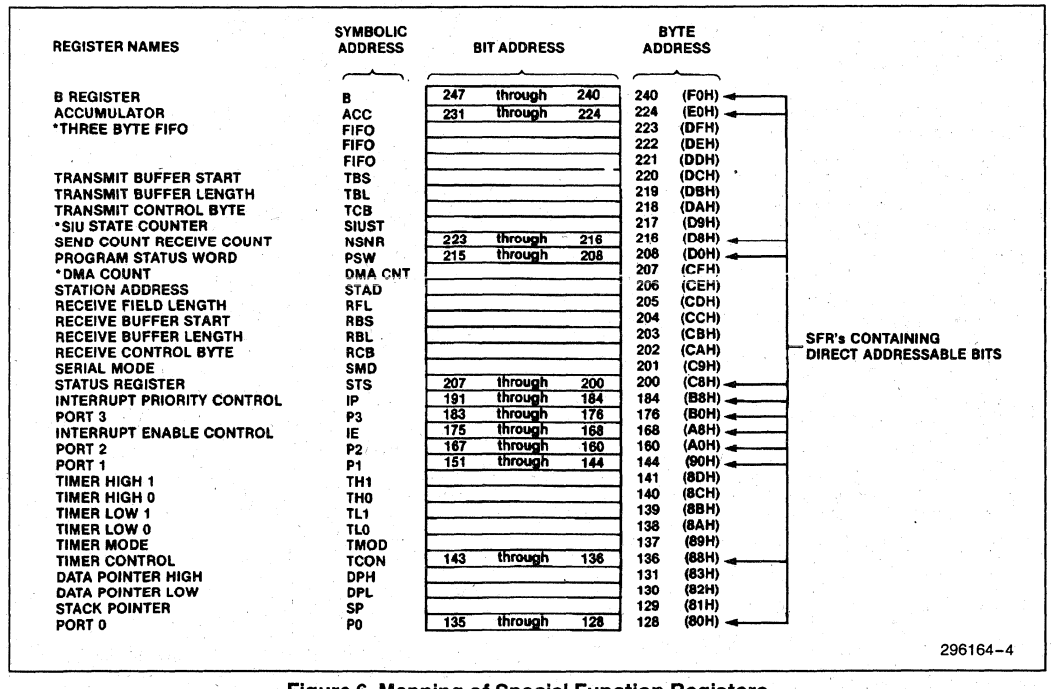


Figure 6. Mapping of Special Function Registers

Direct Byte Address	Bit Address (MSB)							(LSB)	Hardware Register Symbol
240	F7	F6	F5	F4	F3	F2	F1	F0	B
224	E7	E6	E5	E4	E3	E2	E1	E0	ACC
	NS2	NS1	NS0	SES	NR2	NR1	NR0	SER	
216	DF	DE	DD	DC	DB	DA	D9	D8	NSNR
	CY	AC	FO	RS1	RSO	OV		P	
204	D7	D6	D5	D4	D3	D2	D1	D0	PSW
	TBF	RE	RTS	SI	BV	CPB	AM	RBP	
200	CF	CE	CD	CC	CB	CA	C9	C8	STS
				PS	PT1	PX1	PT0	PX0	
184	—	—	—	BC	BB	BA	B9	B8	IP
176	B7	B6	B5	B4	B3	B2	B1	B0	P3
	EA			E5	ET1	EX1	ET0	EX0	
168	AF	—	—	AC	AB	AA	A9	A8	IE
160	A7	A6	A5	A4	A3	A2	A1	A0	P2
144	97	96	95	94	93	92	91	90	P1
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
136	8F	8E	8D	8C	8B	8A	89	88	TCON
128	87	86	85	84	83	82	81	80	P0

Figure 7. Special Function Register Bit Address

- **Register Addressing**
  - — **R7-R0**
  - — **A, B, C (bit), AB (two bytes), DPTR (double byte)**
- **Direct Addressing**
  - — **Lower 128 bytes of Internal Data RAM**
  - — **Special Function Registers**
  - — **128 bits in subset of Special Function Register address space**
- **Register-Indirect Addressing**
  - — **Internal Data RAM [@R1, @R0, @SP (PUSH and POP only)]**
  - — **Least Significant Nibbles in Internal Data RAM (@R1, @R0)**
  - — **External Data Memory (@R1, @R0, @DPTR)**
- **Immediate Addressing**
  - — **Program Memory (in-code constant)**
- **Base-Register-plus Index-Register-Indirect Addressing**
  - — **Program Memory (@ DPTR + A, @ PC + A)**

Figure 8. Operand Addressing Methods

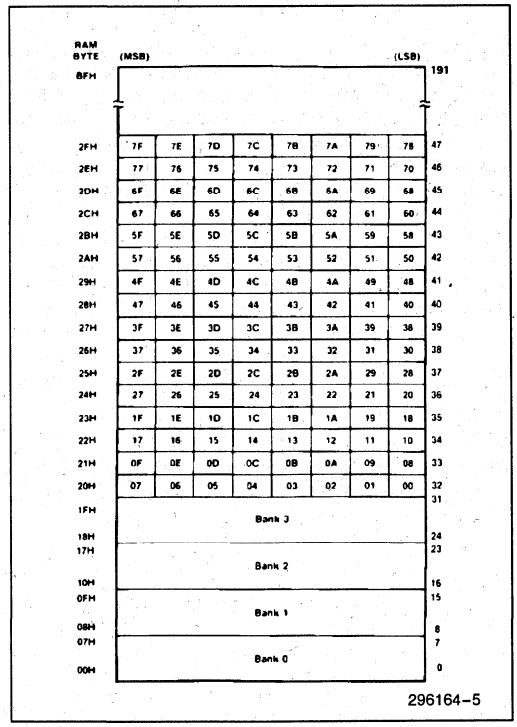


Figure 9. RAM Bit Address

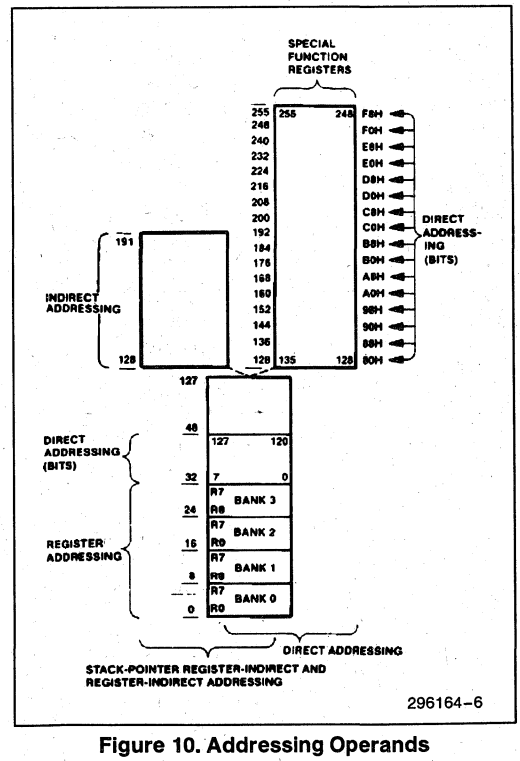


Figure 10. Addressing Operands in Internal Data Memory

Register-Indirect Addressing using the content of R1 or R0 in the selected Register Bank, or using the content of the Stack Pointer (PUSH and POP only), addresses the Internal Data RAM. Register-Indirect Addressing is also used for accessing the External Data Memory. In this case, either R1 or R0 in the selected Register Bank may be used for accessing locations within a 256-byte block. The block number can be preselected by the contents of a port. The 16-bit Data Pointer may be used for accessing any location within the full 64K external address space.

3.0 RESET

Reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) *while the oscillator is running.* The CPU responds by executing an internal reset. It also configures the ALE and PSEN pins as inputs. (They are quasi-bidirectional.) The internal reset is executed during the second cycle in which RST is high and is repeated every cycle until RST goes low. It leaves the internal registers as follows:

Register	Content
PC	0000H
A	00H
B	00H
PSW	00H
SP	07H
DPTR	0000H
P0-P3	0FFH
IP	(XXX00000)
IE	(0XX00000)
TMOD	00H
TCON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
SMD	00H
STS	00H
NSNR	00H
STAD	00H
TBS	00H
TBL	00H
TCB	00H
RBS	00H
RBL	00H
RFL	00H
RCB	00H
DMA CNT	00H
FIFO1	00H
FIFO2	00H
FIFO3	00H
SIUST	01H
PCON	(0XXXXXXX)

The internal RAM is not affected by reset. When VCC is turned on, the RAM content is indeterminate unless VPD was applied prior to VCC being turned off (see Power Down Operation.)

4.0 RUPI-44 FAMILY PIN DESCRIPTION

VSS: Circuit ground potential.

VCC: Supply voltage during programming (of the 8744), verification (of the 8044 or 8744), and normal operation.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accessses to external memory (during which accesses it activates internal pullups). It also outputs instruction bytes during program verification. (External pullups are required during program verification.) Port 0 can sink eight LS TTL inputs.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during program verification in the 8044 or 8744. Port 1 can sink/source four LS TTL inputs, It can drive MOS inputs without external pullups.

Two of the Port 1 pins serve alternate functions, as listed below:

Port Pin	*Alternate Function*
P1.6	$\overline{\text{RTS}}$ (Request to Send). In a non-loop configuration, $\overline{\text{RTS}}$ signals that the 8044 is ready to transmit data.

8044AH/8344AH/8744H
HIGH PERFORMANCE 8-BIT MICROCONTROLLER WITH ON-CHIP SERIAL COMMUNICATION CONTROLLER

- **8044AH—Includes Factory Mask Programmable ROM**
- **8344AH—For Use with External Program Memory**
- **8744H—Includes User Programmable/Eraseable EPROM**

8051 MICROCONTROLLER CORE

- **Optimized for Real Time Control 12 MHz Clock, Priority Interrupts, 32 Programmable I/O Lines, Two 16-bit Timer/Counters**
- **Boolean Processor**
- **4K × 8 ROM, 192 × 8 RAM**
- **64K Accessible External Program Memory**
- **64K Accessible External Data Memory**
- **4 μs Multiply and Divide**

SERIAL INTERFACE UNIT (SIU)

- **Serial Communication Processor that Operates Concurrently to CPU**
- **2.4 Mbps Maximum Data Rate**
- **375 Kbps using On-Chip Phase Locked Loop**
- **Communication Software in Silicon:**
  — Complete Data Link Functions
  — Automatic Station Response
- **Operates as an SDLC Primary or Secondary Station**

The RUPI-44 family integrates a high performance 8-bit Microcontroller, the Intel 8051 Core, with an Intelligent/high performance HDLC/SDLC serial communication controller, called the Serial Interface Unit (SIU). See Figure 1. This dual architecture allows complex control and high speed data communication functions to be realized cost effectively.

Specifically, the 8044's Microcontroller features: 4K byte On-Chip program memory space; 32 I/O lines; two 16-bit timer/event counters; a 5-source; 2-level interrupt structure; a full duplex serial channel; a Boolean processor; and on-chip oscillator and clock circuitry. Standard TTL and most byte-oriented MCS-80 and MCS-85 peripherals can be used for I/O amd memory expansion.

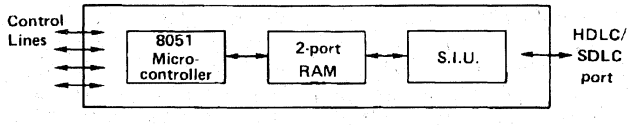
The Serial Interface Unit (SIU) manages the interface to a high speed serial link. The SIU offloads the On-Chip 8051 Microcontroller of communication tasks, thereby freeing the CPU to concentrate on real time control tasks.

The RUPI-44 family consists of the 8044, 8744, and 8344. All three devices are identical except in respect of on-chip program memory. The 8044 contains 4K bytes of mask-programmable ROM. User programmable EPROM replaces ROM in the 8744. The 8344 addresses all program memory externally.

The RUPI-44 devices are fabricated with Intel's reliable +5 volt, silicon-gate HMOSII technology and packaged in a 40-pin DIP.

The 8744H is available in a hermetically sealed, ceramic, 40-lead dual in-line package which includes a window that allows for EPROM erasure when exposed to ultraviolet light (See Erasure Characteristics). During normal operation, ambient light may adversely affect the functionality of the chip. Therefore applications which expose the 8744H to ambient light may require an opaque label over the window.

8044's Dual Controller Architecture



231663-1

Figure 1. Dual Controller Architecture

October 1994 Order Number: 231663-004

Table 1. RUPI-44 Family Pin Description

VSS

Circuit ground potential.

VCC

+5V power supply during operation and program verification.

PORT 0

Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads (six in 8744).

PORT 1

Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.

In non-loop mode two of the I/O lines serve alternate functions:

— $\overline{RTS}$ (P1.6). Request-to-Send output. A low indicates that the RUPI-44 is ready to transmit.

— $\overline{CTS}$ (P1.7) Clear-to-Send input. A low indicates that a receiving station is ready to receive.

PORT 2

Port 2 is an 8-bit quasi-bidirection I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

PORT 3

Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS LTT loads.

In addition to I/O, some of the pins also serve alternate functions as follows:

— I/$\overline{O}$ RxD (P3.0). In point-to-point or multipoint configurations, this pin controls the direction of pin P3.1. Serves as Receive Data input in loop and diagnostic modes.

— DATA TxD (P3.1) In point-to-point or multipoint configurations, this pin functions as data input/output. In loop mode, it serves as transmit pin. A '0' written to this pin enables diagnostic mode.

— $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.

— $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1.

— TO (P3.4). Input to counter 0.

— SCLK T1 (P3.5). In addition to I/O, this pin provides input to counter 1 or serves as SCLK (serial clock) input.

— $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.

— $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

RST

A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx 8.2K\Omega$) from RST to V_{SS} permits power-on reset when a capacitor ($\approx 10\mu f$) is also connected from this pin to V_{CC}.

ALE/$\overline{PROG}$

Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. It also receives the program pulse input for programming the EPROM version.

$\overline{PSEN}$

The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

$\overline{EA}$/VPP

When held at a TTL high level, the RUPI-44 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the RUPI-44 fetches all instructions from external Program Memory. The pin also receives the 21V EPROM programming supply voltage on the 8744.

Table 1. RUPI-44 Family Pin Description (Continued)

XTAL 1	XTAL 2
Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2.	Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

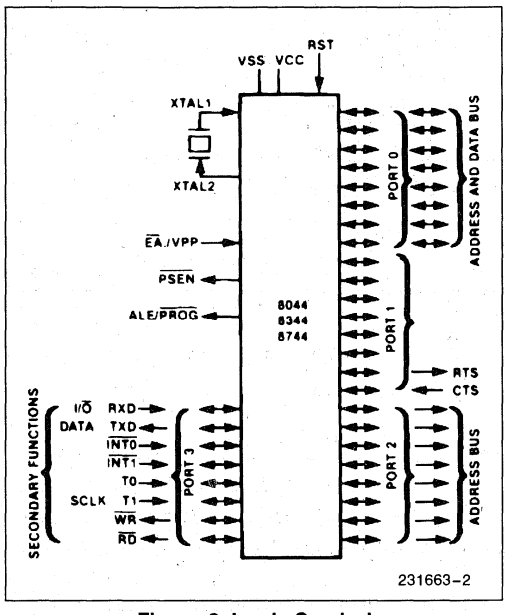


Figure 2. Logic Symbol

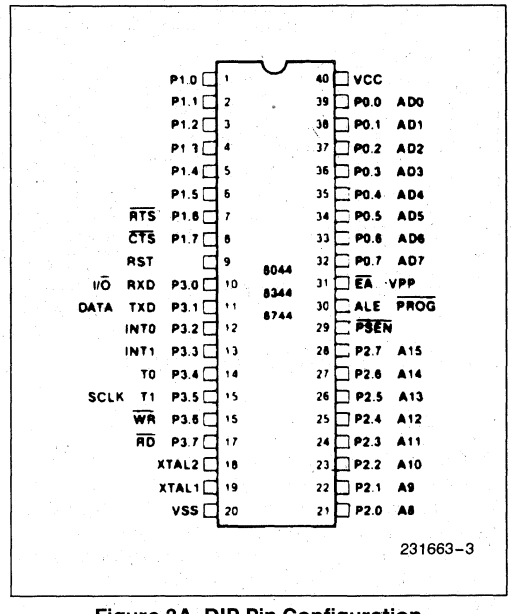


Figure 3A. DIP Pin Configuration

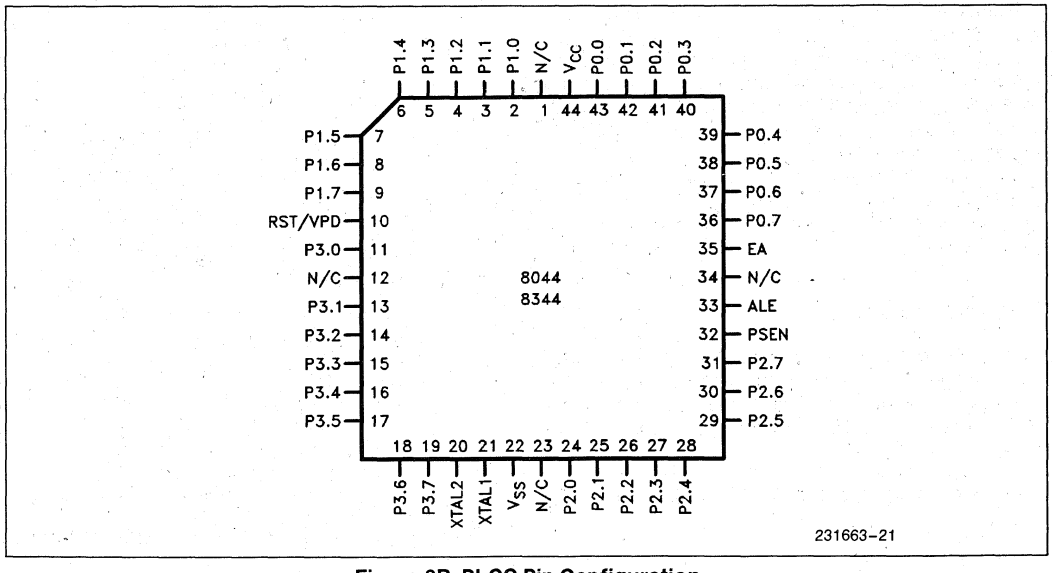


Figure 3B. PLCC Pin Configuration

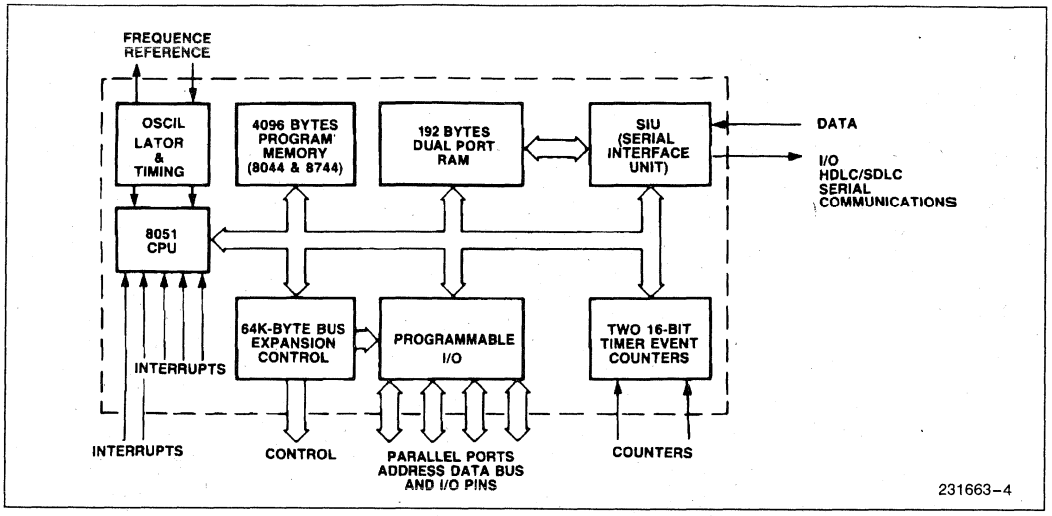


Figure 4. Block Diagram

FUNCTIONAL DESCRIPTION

General

The 8044 integrates the powerful 8051 microcontroller with an intelligent Serial Communication Controller to provide a single-chip solution which will efficiently implement a distributed processing or distributed control system. The microcontroller is a self-sufficient unit containing ROM, RAM, ALU, and its own peripherals. The 8044's architecture and instruction set are identical to the 8051's. The 8044 replaces the 8051's serial interface with an intelligent SDLC/HDLC Serial Interface Unit (SIU). 64 more bytes of RAM have been added to the 8051 RAM array. The SIU can communicate at bit rates up to 2.4 M bps. The SIU works concurrently with the Microcontroller so that there is no throughput loss in either unit. Since the SIU possesses its own intelligence, the CPU is off-loaded from many of the communications tasks, thus dedicating more of its computing power to controlling local peripherals or some external process.

The Microcontroller

The microcontroller is a stand-alone high-performance single-chip computer intended for use in sophisticated real-time application such as instrumentation, industrial control, and intelligent computer peripherals.

The major features of the microcontroller are:

- 8-bit CPU
- on-chip oscillator
- 4K bytes of ROM
- 192 bytes of RAM
- 32 I/O lines
- 64K address space for external Data Memory
- 64K address space for external Program Memory
- two fully programmable 16-bit timer/counters
- a five-source interrupt structure with two priority levels
- bit addressability for Boolean processing

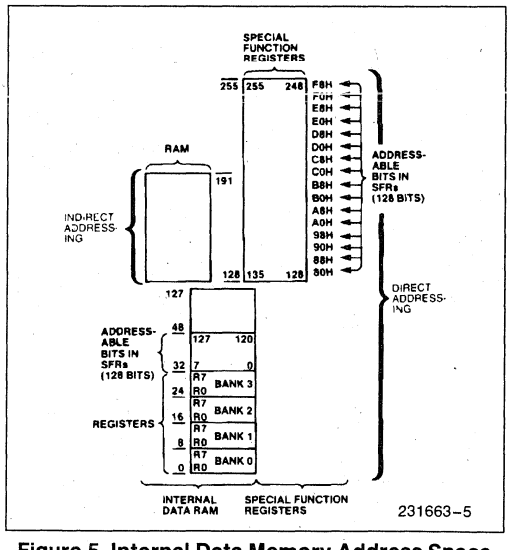


Figure 5. Internal Data Memory Address Space

- 1 μs instruction cycle time for 60% of the instructions 2 μs instruction cycle time for 40% of the instructions
- 4 μs cycle time for 8 by 8 bit unsigned Multiply/Divide

INTERNAL DATA MEMORY

Functionally the Internal Data Memory is the most flexible of the address spaces. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address space and a 128-bit Special Function Register address space as shown in Figure 5.

The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit locations of the on-chip RAM are accessible through Direct Addressing. These bits reside in Internal Data RAM at byte locations 32 through 47. Currently locations 0 through 191 of the Internal Data RAM address space are filled with on-chip RAM.

Parallel I/O

The 8044 has 32 general-purpose I/O lines which are arranged into four groups of eight lines. Each group is called a port. Hence there are four ports; Port 0, Port 1, Port 2, and Port 3. Up to five lines from Port 3 are dedicated to supporting the serial channel when the SIU is invoked. Due to the nature of the serial port, two of Port 3's I/O lines (P3.0 and P3.1) do not have latched outputs. This is true whether or not the serial channel is used.

Port 0 and Port 2 also have an alternate dedicated function. When placed in the external access mode, Port 0 and Port 2 become the means by which the 8044 communicates with external program memory. Port 0 and Port 2 are also the means by which the 8044 communicates with external data memory. Peripherals can be memory mapped into the address space and controlled by the 8044.

Table 2. MCS®-51 Instruction Set Description

Mnemonic		Description	Byte	Cyc
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB	A,#data	Subtract immed data from A with Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic		Description	Byte	Cyc
LOGICAL OPERATIONS				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@RI	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@RI	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1

Mnemonic		Description	Byte	Cyc
LOGICAL OPERATIONS (Continued)				
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@RI	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic		Description	Byte	Cyc
DATA TRANSFER (Continued)				
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit) addr	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind RAM w A	1	1
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry Flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry Flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C/bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,/bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2
PROGRAM AND MACHINE CONTROL				
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp, immed, to A & Jump if Not Equal	3	2

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic	Description	Byte	Cyc
PROGRAM AND MACHINE CONTROL (Continued)			
CJNE Rn,#data,rel	Comp, immed, to reg & Jump if Not Equal	3	2
CJNE @Ri,#data, rel	Comp, immed, to ind. & Jump if Not Equal	3	2
DJNZ Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP	No operation	1	1

Notes on data addressing modes:

Rn — Working register R0-R7

direct — 128 internal RAM locations, any I/O port, control or status register

@Ri — Indirect internal RAM location addressed by register R0 or R1

Notes on data addressing modes:

(Continued)

#data — 8-bit constant included in instruction

#data16 — 16-bit constant included as bytes 2 & 3 of instruction

bit — 128 software flags, any I/O pin, controll or status bit

Notes on program addressing modes:

addr16 — Destination address for LCALL & LJMP may be anywhere within the 64-K program memory address space

Addr11 — Destination address for ACALL & AJMP will be within the same 2-K page of program memory as the first byte of the following instruction

rel — SJMP and all conditional jumps include an 8-bit offset byte, Range is +127 −128 bytes relative to first byte of the following instruction

Timer/Counters

The 8044 contains two 16-bit counters which can be used for measuring time intervals, measuring pulse widths, counting events, generating precise periodic interrupt requests, and clocking the serial communications. Internally the Timers are clocked at 1/12 of the crystal frequency, which is the instruction cycle time. Externally the counters can run up to 500 KHz.

Interrupt System

External events and the real-time driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two priority level, nested interrupt system is provided. Interrupt response latency ranges from 3 μsec to 7 μsec when using a 12 MHz clock.

All five interrupt sources can be mapped into one of the two priority levels. Each interrupt source can be enabled or disabled individually or the entire interrupt system can be enabled or disabled. The five interrupt sources are: Serial Interface Unit, Timer 1, Timer 2, and two external interrupts. The external interrupts can be either level or edge triggered.

Serial Interface Unit (SIU)

The Serial Interface Unit is used for HDLC/SDLC communications. It handles Zero Bit Insertion/Deletion, Flags automatic access recognization, and a 16-bit cyclic redundancy check. In addition it implements in hardware a subset of the SDLC protocol certain applications it is advantageous to have the CPU control the reception or transmission of every single frame. For this reason the SIU has two modes of operation: "AUTO" and "FLEXIBLE" (or "NON-AUTO"). It is in the AUTO mode that the SIU responds to SDLC frames without CPU intervention; whereas, in the FLEXIBLE mode the reception or transmission of every single frame will be under CPU control.

There are three control registers and eight parameter registers that are used to operate the serial interface. These registers are shown in Figure 5 and Figure 6. The control register set the modes of operation and provide status information. The eight parameter registers buffer the station address, receive and transmit control bytes, and point to the on-chip transmit and receive buffers.

Data to be received or transmitted by the SIU must be buffered anywhere within the 192 bytes of on-chip RAM. Transmit and receive buffers are not allowed to "wrap around" in RAM; a "buffer end" is generated after address 191 is reached.

REGISTER NAMES	SYMBOLIC ADDRESS	BIT ADDRESS	BYTE ADDRESS	
B REGISTER	B	247 through 240	240	(F0H)
ACCUMULATOR	ACC	231 through 224	224	(E0H)
*THREE BYTE FIFO	FIFO		223	(DFH)
	FIFO		222	(DEH)
	FIFO		221	(DDH)
TRANSMIT BUFFER START	TBS		220	(DCH)
TRANSMIT BUFFER LENGTH	TBL		219	(DBH)
TRANSMIT CONTROL BYTE	TCB		218	(DAH)
* SIU STATE COUNTER	SIUST		217	(D9H)
SEND COUNT RECEIVE COUNT	NSNR	223 through 216	216	(D8H)
PROGRAM STATUS WORD	PSW	215 through 208	208	(D0H)
*DMA COUNT	DMA CNT		207	(CFH)
STATION ADDRESS	STAD		206	(CEH)
RECEIVE FIELD LENGTH	RFL		205	(CDH)
RECEIVE BUFFER START	RBS		204	(CCH)
RECEIVE BUFFER LENGTH	RBL		203	(CBH)
RECEIVE CONTROL BYTE	RCB		202	(CAH)
SERIAL MODE	SMD		201	(C9H)
STATUS REGISTER	STS	207 through 200	200	(C8H)
INTERRUPT PRIORITY CONTROL	IP	191 through 184	184	(B8H)
PORT 3	P3	183 through 176	176	(B0H)
INTERRUPT ENABLE CONTROL	IE	175 through 168	168	(A8H)
PORT 2	P2	167 through 160	160	(A0H)
PORT 1	P1	151 through 144	144	(90H)
TIMER HIGH 1	TH1		141	(8DH)
TIMER HIGH 0	TH0		140	(8CH)
TIMER LOW 1	TL1		139	(8BH)
TIMER LOW 0	TL0		138	(8AH)
TIMER MODE	TMOD		137	(89H)
TIMER CONTROL	TCON	143 through 136	136	(88H)
DATA POINTER HIGH	DPH		131	(83H)
DATA POINTER LOW	DPL		130	(82H)
STACK POINTER	SP		129	(81H)
PORT 0	P0	135 through 128	128	(80H)

SFR's CONTAINING DIRECT ADDRESSABLE BITS

231663-6

NOTE:
*ICE Support Hardware registers. Under normal operating conditions there is no need for the CPU to access these registers.

Figure 5. Mapping of Special Function Registers

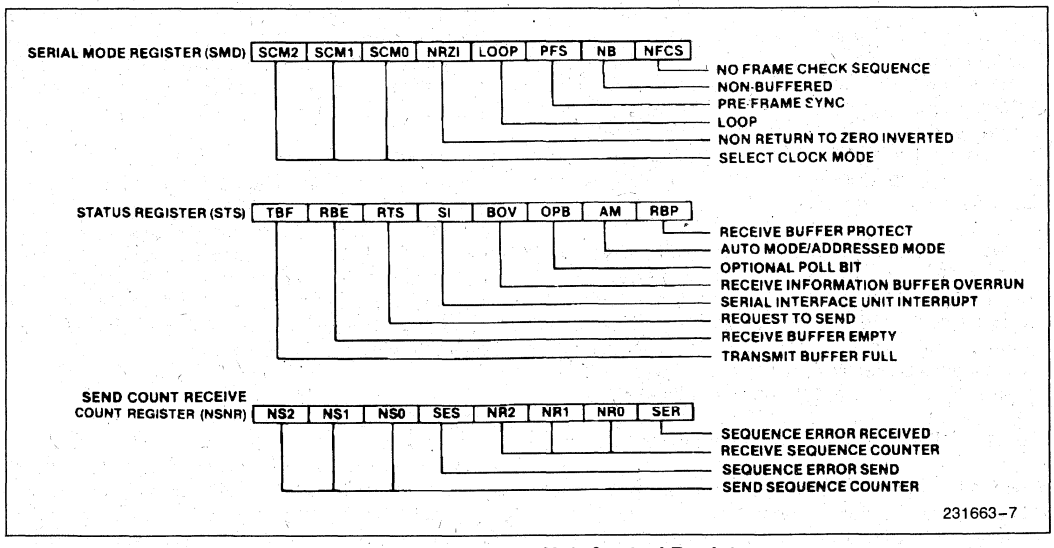


Figure 6. Serial Interface Unit Control Registers

With the addition of only a few bytes of code, the 8044's frame size is not limited to the size of its internal RAM (192 bytes), but rather by the size of external buffer with no degradation of the RUPI's features (e.g. NRZI, zero bit insertion/deletion, address recognition, cyclic redundancy check). There is a special function register called SIUST whose contents dictates the operation of the SIU. At low data rates, one section of the SIU (the Byte Processor) performs no function during known intervals. For a given data rate, these intervals (stand-by mode) are fixed. The above characteristics make it possible to program the CPU to move data to/from external RAM and to force the SIU to perform some desired hardware tasks while transmission or reception is taking place. With these modifications, external RAM can be utilized as a transmit and received buffer instead of the internal RAM.

AUTO Mode

In the AUTO mode the SIU implements in hardware a subset of the SDLC protocol such that it responds to many SDLC frames without CPU intervention. All AUTO mode responses to the primary station will comform to IBM's SDLC definition. The advantages of the AUTO mode are that less software is required to implement a secondary station, and the hardware generated response to polls is much faster than doing it in software. However, the Auto mode can not be used at a primary station.

To transmit in the AUTO mode the CPU must load the Transmit Information Buffer, Transmit Buffer Start register, Transmit Buffer Length register, and set the Transmit Buffer Full bit. The SIU automatically responds to a poll by transmitting an information frame with the P/F bit in the control field set. When the SIU receives a positive acknowledgement from the primary station, it automatically increments the Ns field in the NSNR register and interrupts the CPU. A negative acknowledgement would cause the SIU to retransmit the frame.

To receive in the AUTO mode, the CPU loads the Receive Buffer Start register, the Receive Buffer Length register, clears the Receive Buffer Protect bit, and sets the Receive Buffer Empty bit. If the SIU is polled in this state, and the TBF bit indicates that the Transmit Buffer is empty, an automatic RR response will be generated. When a valid information frame is received the SIU will automatically increment Nr in the NSNR register and interrupt the CPU.

While in the AUTO mode the SIU can recognize and respond to the following commands without CPU intervention: I (Information), RR (Receive Ready), RNR (Receive Not Ready), REJ (Reject), and UP (Unnumbered Poll). The SIU can generate the following responses without CPU intervention: I (Information), RR (Receive Ready), and RNR (Receive Not Ready).

When the Receive Buffer Empty bit (RBE) indicates that the Receive Buffer is empty, the receiver is enabled, and when the RBE bit indicates that the Receive Buffer is full, the receiver is disabled. Assuming that the Receiver Buffer is empty, the SIU will respond to a poll with an I frame if the Transmit Buffer is full. If the Transmit Buffer is empty, the SIU will respond to a poll with a RR command if the Receive Buffer Protect bit (RBP) is cleared, or an RNR command if RBP is set.

FLEXIBLE (or NON-AUTO) Mode

In the FLEXIBLE mode all communications are under control of the CPU. It is the CPU's task to encode and decode control fields, manage acknowledgements, and adhere to the requirements of the HDLC/SDLC protocols. The 8044 can be used as a primary or a secondary station in this mode.

To receive a frame in the FLEXIBLE mode, the CPU must load the Receive Buffer Start register, the Receive Buffer Length register, clear the Receive Buffer Protect bit, and set the Receive Buffer Empty bit. If a valid opening flag is received and the address field matches the byte in the Station Address register or the address field contains a broadcast address, the 8044 loads the control field in the receive control byte register, and loads the I field in the receive buffer. If there is no CRC error, the SIU interrupts the CPU, indicating a frame has just been received. If there is a CRC error, no interrupt occurs. The Receive Field Length register provides the number of bytes that were received in the information field.

To transmit a frame, the CPU must load the transmit information buffer, the Transmit Buffer Start register, the Transmit Buffer Length register, the Transmit Control Byte, and set the TBF and the RTS bit. The SIU, unsolicited by an HDLC/SDLC frame, will transmit the entire information frame, and interrupt the CPU, indicating the completion of transmission. For supervisory frames or unnumbered frames, the transmit buffer length would be 0.

CRC

The FCS register is initially set to all 1's prior to calculating the FCS field. The SIU will not interrupt the CPU if a CRC error occurs (in both AUTO and FLEXIBLE modes). The CRC error is cleared upon receiving of an opening flag.

Frame Format Options

In addition to the standard SDLC frame format, the 8044 will support the frames displayed in Figure 7. The standard SDLC frame is shown at the top of this figure. For the remaining frames the information field will incorporate the control or address bytes and the frame check sequences; therefore these fields will be stored in the Transmit and Receive buffers. For example, in the non-buffered mode the third byte is treated as the beginning of the information field. In the non-addressed mode, the information field begins after the opening flag. The mode bits to set the frame format options are found in the Serial Mode register and the Status register.

FRAME OPTION	NFCS	NB	AM[1]	FRAME FORMAT
Standard SDLC NON-AUTO Mode	0	0	0	F A C I FCS F
Standard SDLC AUTO Mode	0	0	1	F A C I FCS F
Non-Buffered Mode NON-AUTO Mode	0	1	1	F A I FCS F
Non-Addressed Mode NON-AUTO Mode	0	1	0	F I FCS F
No FCS Field NON-AUTO Mode	1	0	0	F A C I F
No FCS Field AUTO Mode	1	0	1	F A C I F
No FCS Field Non-Buffered Mode NON-AUTO Mode	1	1	1	F A I F
No FCS Field Non-Addressed Mode NON-AUTO Mode	1	1	0	F I F

Mode Bits:
AM — "AUTO" Mode/Addressed Mode
NB — Non-Buffered Mode
NFCS — No FCS Field Mode

Key to Abbreviations:
F = Flag (01111110)
A = Address Field
C = Control Field
I = Information Field
FCS= Frame Check Sequence

Note 1:
The AM bit function is controlled by the NB bit. When NB = 0, AM becomes AUTO mode select, when NB = 1, AM becomes Address mode select.

Figure 7. Frame Format Options

Extended Addressing

To realize an extended control field or an extended address field using the HDLC protocol, the FLEXIBLE mode must be used. For an extended control field, the SIU is programmed to be in the non-buffered mode. The extended control field will be the first and second bytes in the Receive and Transmit Buffers. For extended addressing the SIU is placed in the non-addressed mode. In this mode the CPU must implement the address recognition for received frames. The addressing field will be the initial bytes in the Transmit and Receive buffers followed by the control field.

The SIU can transmit and receive only frames which are multiples of 8 bits. For frames received with other than 8-bit multiples, a CRC error will cause the SIU to reject the frame.

SDLC Loop Networks

The SIU can be used in an SDLC loop as a secondary or primary station. When the SIU is placed in the Loop mode it receives the data on pin 10 and transmits the data one bit time delayed on pin 11. It can also recognize the Go ahead signal and change it into a flag when it is ready to transmit. As a secondary station the SIU can be used in the AUTO or FLEXIBLE modes. As a primary station the FLEXIBLE mode is used; however, additional hardware is required for generating the Go Ahead bit pattern. In the Loop mode the maximum data rate is 1 Mbps clocked or 375 Kpbs self-clocked.

SDLC Multidrop Networks

The SIU can be used in a SDLC non-loop configuration as a secondary or primary station. When the SIU is placed in the non-loop mode, data is received and transmitted on pin 11, and pin 10 drives a tri-state buffer. In non-loop mode, modem interface pins, RTS and CTS, become available.

Data Clocking Options

The 8044's serial port can operate in an externally clocked or self clocked system. A clocked system provides to the 8044 a clock synchronization to the data. A self-clocked system uses the 8044's on-chip Digital Phase Locked Loop (DPLL) to recover the clock from the data, and clock this data into the Serial Receive Shift Register.

In this mode, a clock synchronized with the data is externally fed into the 8044. This clock may be generated from an External Phase Locked Loop, or possibly supplied along with the data. The 8044 can transmit and receive data in this mode at rates up to 2.4 Mbps.

This self clocked mode allows data transfer without a common system data clock. An on-chip Digital Phase Locked Loop is employed to recover the data clock which is encoded in the data stream. The DPLL will converge to the nominal bit center within eight bit transitions, worst case. The DPLL requires a reference clock of either 16 times (16x) or 32 times (32x) the data rate. This reference clock may be externally applied or internally generated. When internally generated either the 8044's internal logic clock (crystal frequency divided by two) or the timer 1 overflow is used as the reference clock. Using the internal timer 1 clock the data rates can vary from 244 to 62.5 Kbps. Using the internal logic clock at a 16x sampling rate, receive data can either be 187.5 Kbps, or 375 Kbps. When the reference clock for the DPLL is externally applied the data rates can vary from 0 to 375 Kbps at a 16x sampling rate.

To aid in a Phase Locked Loop capture, the SIU has a NRZI (Non Return to Zero Inverted) data encoding and decoding option. Additionally the SIU has a preframe sync option that transmits two bytes of alternating 1's and 0's to ensure that the receive station DPLL will be synchronized with the data by the time it receives the opening flag.

Control and Status Registers

There are three SIU Control and Status Registers:

Serial Mode Register (SMD)

Status/Command Register (STS)

Send/Receive Count Register (NSNR)

The SMD, STS, and NSNR, registers are all cleared by system reset. This assures that the SIU will power up in an idle state (neither receiving nor transmitting).

These registers and their bit assignments are described below.

SMD: Serial Mode Register (byte-addressable)

Bit 7:	6	5	4	3	2	1	0
SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

The Serial Mode Register (Address C9H) selects the operational modes of the SIU. The 8044 CPU can both read and write SMD. The SIU can read SMD but cannot write to it. To prevent conflict between CPU and SIU access to SMD, the CPU should write SMD only when the Request To Send (RTS) and

Receive Buffer Empty (RBE) bits (in the STS register) are both false (0). Normally, SMD is accessed only during initialization.

The individual bits of the Serial Mode Register are as follows:

Bit #	Name	Description
SMD.0	NFCS	No FCS field in the SDLC frame.
SMD.1	NB	Non-Buffered mode. No control field in the SDLC frame.
SMD.2	PFS	Pre-Frame Sync mode. In this mode, the 8044 transmits two bytes before the first flag of a frame, for DPLL synchronization. If NRZI is enabled, 00H is sent; otherwise, 55H is sent. In either case, 16 preframe transitions are guaranteed.
SMD.3	LOOP	Loop configuration.
SMD.4	NRZI	NRZI coding option. If bit = 1, NRZI coding is used. If bit = 0, then it is straight binary (NRZ).
SMD.5	SCM0	Select Clock Mode—Bit 0
SMD.6	SCM1	Select Clock Mode—Bit 1
SMD.7	SCM2	Select Clock Mode—Bit 2

The SCM bits decode as follows:

SCM				Data Rate
2	1	0	Clock Mode	(Bits/sec)*
0	0	0	Externally clocked	0-2.4M**
0	0	1	Reserved	
0	1	0	Self clocked, timer overflow	244-62.5K
0	1	1	Reserved	
1	0	0	Self clocked, external 16x	0-375K
1	0	1	Self clocked, external 32x	0-187.5K
1	1	0	Self clocked, internal fixed	375K
1	1	1	Self clocked, internal fixed	187.5K

NOTES:
*Based on a 12 Mhz crystal frequency
**0-1 M bps in loop configuration

STS: Status/Command Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	TBF	RBE	RTS	SI	BOV	OPB	AM	RBP

The Status/Command Register (Address C8H) provides operational control of the SIU by the 8044 CPU, and enables the SIU to post status information for the CPU's access. The SIU can read STS, and can alter certain bits, as indicated below. The CPU can both read and write STS asynchronously. However, 2-cycle instructions that access STS during both cycles ('JBC/B, REL' and 'MOV/B, C.') should not be used, since the SIU may write to STS between the two CPU accesses.

The individual bits of the Status/Command Register are as follows:

Bit #	Name	Description
STS.0	RBP	Receive Buffer Protect. Inhibits writing of data into the receive buffer. In AUTO mode, RBP forces an RNR response instead of an RR.
STS.1	AM	AUTO Mode/Addressed Mode. Selects AUTO mode where AUTO mode is allowed. If NB is true, (= 1), the AM bit selects the addressed mode. AM may be cleared by the SIU.
STS.2	OPB	Optional Poll Bit. Determines whether the SIU will generate an AUTO response to an optional poll (UP with P = 0). OPM may be set or cleared by the SIU.
STS.3	BOV	Receive Buffer Overrun. BOV may be set or cleared by the SIU.
STS.4	SI	SIU Interrupt. This is one of the five interrupt sources to the CPU. The vector location = 23H. SI may be set by the SIU. It should be cleared by the CPU before returning from an interrupt routine.
STS.5	RTS	Request To Send. Indicates that the 8044 is ready to transmit or is transmitting. RTS may be read or written by the CPU. RTS may be read by the SIU, and in AUTO mode may be written by the SIU.
STS.6	RBE	Receive Buffer Empty. RBE can be thought of as Receive Enable. RBE is set to one by the CPU when it is ready to receive a frame, or has just read the buffer, and to zero by the SIU when a frame has been received.
STS.7	TBF	Transmit Buffer Full. Written by the CPU to indicate that it has filled the transmit buffer. TBF may be cleared by the SIU.

NSNR: Send/Receive Count Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	NS2	NS1	NS0	SES	NR2	NR1	NR0	SER

The Send/Receive Count Register (Address D8H) contains the transmit and receive sequence numbers, plus tally error indications. The SIU can both read and write NSNR. The 8044 CPU can both read and write NSNR asynchronously. However, 2-cycle instructions that access NSNR during both cycles ('JBC /B, REL,' and 'MOV /B,C') should not be used, since the SIU may write to NSMR between the two 8044 CPU accesses.

The individual bits of the Send/Receive Count Register are as follows:

Bit#	Name	Description
NSNR.0	SER	Receive Sequence Error: NS (P) ≠ NR (S)
NSNR.1	NR0	Receive Sequence Counter—Bit 0
NSNR.2	NR1	Receive Sequence Counter—Bit 1
NSNR.3	NR2	Receive Sequence Counter—Bit 2
NSNR.4	SES	Send Sequence Error: NR (P) ≠ NS (S) and NR (P) ≠ NS (S) + 1
NSNR.5	NS0	Send Sequence Counter—Bit 0
NSNR.6	NS1	Send Sequence Counter—Bit 1
NSNR.7	NS2	Send Sequence Counter—Bit 2

Parameter Registers

There are eight parameter registers that are used in connection with SIU operation. All eight registers may be read or written by the 8044 CPU. RFL and RCB are normally loaded by the SIU.

The eight parameter registers are as follows:

STAD: Station Address Register (byte-addressable)

The Station Address register (Address CEH) contains the station address. To prevent acess conflict, the CPU should access STAD only when the SIU is idle (RTS = 0 and RBE = 0). Normally, STAD is accessed only during initialization.

TBS: Transmit Buffer Start Address Register (byte-addressable)

The Transmit Buffer Start address register (Address DCH) points to the location in on-chip RAM for the beginning of the I-field of the frame to be transmitted. The CPU should access TBS only when the SIU is not transmitting a frame (when TBF = 0).

TBL: Transmit Buffer Length Register (byte = addressable)

The Transmit Buffer Length register (Address DBH) contains the length (in bytes) of the I-field to be transmitted. A blank I-field (TBL = 0) is valid. The CPU should access TBL only when the SIU is not transmitting a frame (when TBF = 0).

NOTE:
The transmit and receive buffers are not allowed to "wrap around" in the on-chip RAM. A "buffer end" is automatically generated if address 191 (BFH) is reached.

TCB: Transmit Control Byte Register (byte-addressable)

The Transmit Control Byte register (Address DAH) contains the byte which is to be placed in the control field of the transmitted frame, during NON-AUTO mode transmission. The CPU should access TCB only when the SIU is not transmitting a frame (when TBF = 0). The N_S and N_R counters are not used in the NON-AUTO mode.

RBS: Receive Buffer Start Address Register (byte-addressable)

The Receive Buffer Start address register (Address CCH) points to the location in on-chip RAM where the beginning of the I-field of the frame being received is to be stored. The CPU should write RBS only when the SIU is not receiving a frame (when RBE = 0).

RBL: Receive Buffer Length Register (byte-addressable)

The Receive Buffer Length register (Address CBH) contains the length (in bytes) of the area in on-chip RAM allocated for the received I-field. RBL=0 is valid. The CPU should write RBL only when RBE=0.

RFL: Receive Field Length Register (byte-addressable)

The Receive Field Length register (Address CDH) contains the length (in bytes) of the received I-field that has just been loaded into on-chip RAM. RFL is loaded by the SIU. RFL = 0 is valid. RFL should be accessed by the CPU only when RBE = 0.

RCB: Receive Control Byte Register (byte-addressable)

The Received Control Byte register (Address CAH) contains the control field of the frame that has just been received. RCB is loaded by the SIU. The CPU can only read RCB, and should only access RCB when RBE = 0.

ICE Support

The 8044 In-Circuit Emulator (ICE-44) allows the user to exercise the 8044 application system and monitor the execution of instructions in real time.

The emulator operates with Intel's Intellec development system. The development system interfaces with the user's 8044 system through an in-cable buffer box. The cable terminates in a 8044 pin-compatible plug, which fits into the 8044 socket in the user's system. With the emulator plug in place, the user can excercise his system in real time while collecting up to 255 instruction cycles of real-time data. In addition, he can single-step the program.

Static RAM is available (in the in-cable buffer box) to emulate the 8044 internal and external program memory and external data memory. The designer can display and alter the contents of the replacement memory in the buffer box, the internal data memory, and the internal 8044 registers, including the SFR's.

SIUST: SIU State Counter (byte-addressable)

The SIU State Counter (Address D9H) reflects the state of the internal logic which is under SIU control. Therefore, care must be taken not to write into this register. This register provides a useful means for debugging 8044 receiver problem.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature.....−65°C to −150°C
Voltage on $\overline{EA}$, VPP Pin to VSS...−0.5V to −21.5V
Voltage on Any Other Pin to VSS ....−0.5V to −7V
Power Dissipation 2W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

D.C. CHARACTERISTICS T_A = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter		Min	Max	Unit	Test Conditions
VIL	Input Low Voltage (Except $\overline{EA}$ Pin of 8744H)		−0.5	0.8	V	
VIL1	Input Low Voltage to $\overline{EA}$ Pin of 8744H		0	0.8	V	
VIH	Input High Voltage (Except XTAL2, RST)		2.0	VCC + 0.5	V	
VIH1	Input High Voltage to XTAL2, RST		2.5	VCC + 0.5	V	XTAL1 = VSS
VOL	Output Low Voltage (Ports 1, 2, 3)*			0.45	V	IOL = 1.6mA
VOL1	Output Low Voltage (Port 0,ALE,$\overline{PSEN}$)*					
		8744H		0.60 0.45	V V	IOL = 3.2 mA IOL = 2.4 mA
		8044AH/8344AH		0.45	V	IOL = 3.2 mA
VOH	Output High Voltage (Ports 1, 2, 3)		2.4		V	IOH = −80 μA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)		2.4		V	IOH = −400 μA
IIL	Logical 0 Input Current (Ports 1, 2, 3)			−500	μA	Vin = 0.45V
IIL1	Logical 0 Input Current to $\overline{EA}$ Pin of 8744H only			−15	mA	
IIL2	Logical 0 Input Current (XTAL2)			−4.0	mA	Vin = 0.45V
ILI	Input Leakage Current (Port 0) 8744H 8044AH/8344AH			 ±100 ±10	 μA μA	 0.45 < Vin < VCC 0.45 < Vin < VCC
IIH	Logical 1 Input Current to $\overline{EA}$ Pin of 8744H			500	μA	
IIH1	Input Current to RST to Activate Reset			500	μA	Vin < (VCC − 1.5V)
ICC	Power Supply Current: 8744H 8044AH/8344AH			 285 200	 mA mA	All Outputs Disconnected: $\overline{EA}$ = VCC
CIO	Pin Capacitance			10	pF	Test Freq. = 1MHz(1)

***NOTES:**
1. Sampled not 100% tested. T_A = 25°C.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pin when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, VCC = 5V ± 10%, VSS = 0V, Load Capacitance for Port 0, ALE, and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL-40		ns
TLLAX[1]	Address Hold After ALE Low	48		TCLCL-35		ns
TLLIV	ALE Low to Valid Instr in 8744H 8044AH/8344AH		 183 233		 4TCLCL-150 4TCLCL-100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width 8744H 8044AH/8344AH	 190 215		 3TCLCL-60 3TCLCL-35		 ns ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr in 8744H 8044AH/8344AH		 100 125		 3TCLCL-150 3TCLCL-125	 ns ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ[2]	Input Instr Float After $\overline{PSEN}$		63		TCLCL-20	ns
TPXAV[2]	$\overline{PSEN}$ to Address Valid	75		TCLCL-8		ns
TAVIV	Address to Valid Instr in 8744H 8044AH/8344AH		 267 302		 5TCLCL-150 5TCLCL-115	 ns ns
TAZPL	Address Float to $\overline{PSEN}$	−25		−25		ns

NOTES:
1. TLLAX for access to program memory is different from TLLAX for data memory.
2. Interfacing RUPI-44 devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL-100		ns
TLLAX	Address Hold after ALE	48		TCLCL-35		ns
TRLDV	$\overline{RD}$ Low to Valid Data in		252		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL-50	3TLCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition 8744H 8044AH/8344AH	 13 23		 TCLCL-70 TCLCL-60		 ns ns
TQVWH	Data Setup Before $\overline{WR}$ High	433		7TCLCL-150		ns
TWHQX	Data Held After $\overline{WR}$	33		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		25		25	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High 8744H 8044AH/8344AH	 33 43	 133 123	 TCLCL-50 TCLCL-40	 TCLCL+50 TCLCL+50	 ns ns

NOTE:
1. TLLAX for access to program memory is different from TLLAX for access data memory.

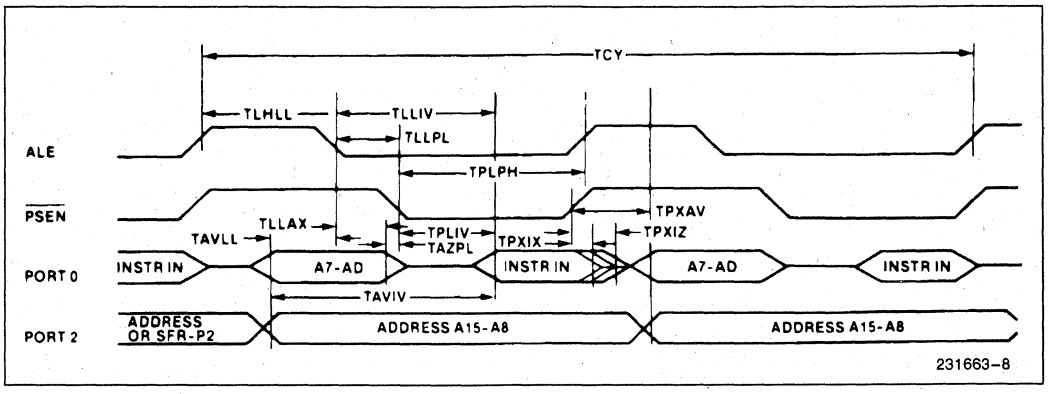
Serial Interface Characteristics

Symbol	Parameter	Min	Max	Unit
TDCY	Data Clock	420		ns
TDCL	Data Clock Low	180		ns
TDCH	Data Clock High	100		ns
tTD	Transmit Data Delay		140	ns
tDSS	Data Setup Time	40		ns
tDHS	Data Hold Time	40		ns

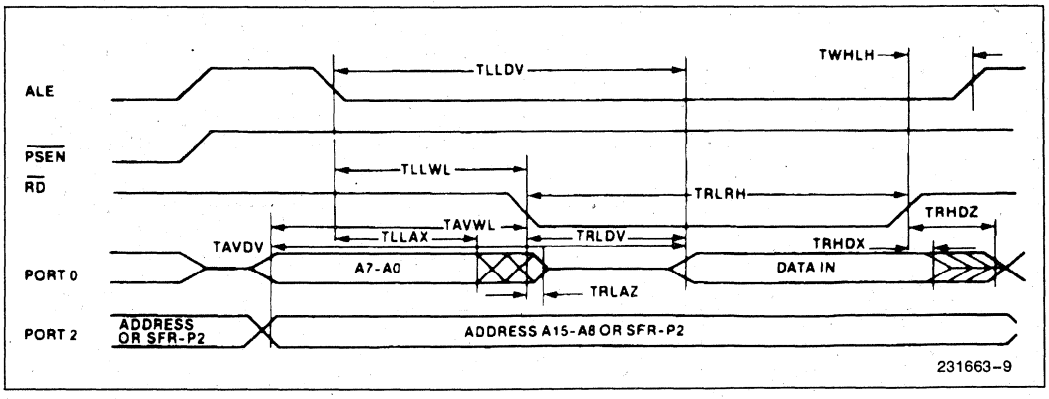
WAVEFORMS

Memory Access

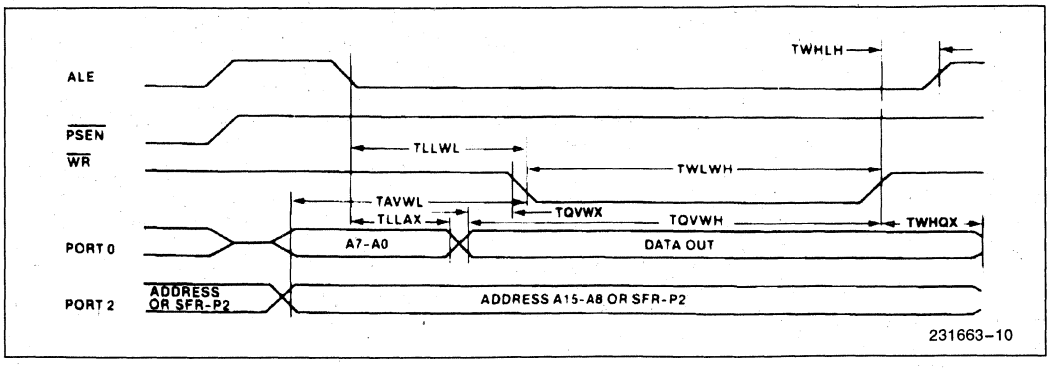
PROGRAM MEMORY READ CYCLE



DATA MEMORY READ CYCLE

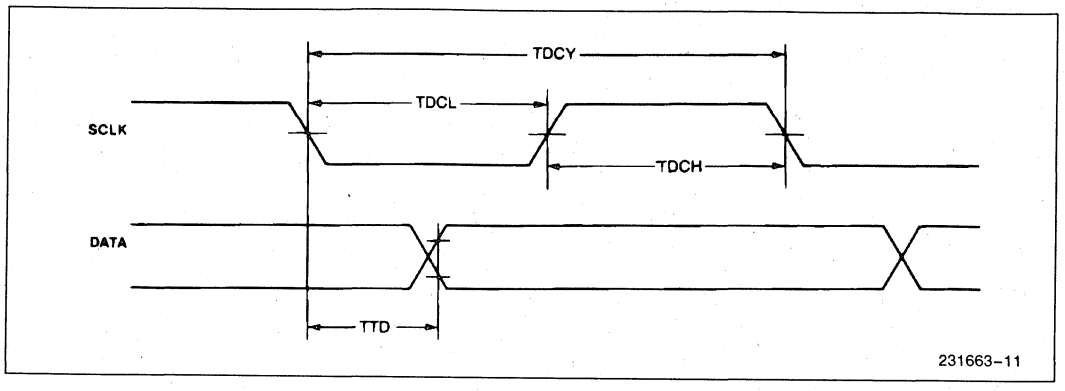


DATA MEMORY WRITE CYCLE

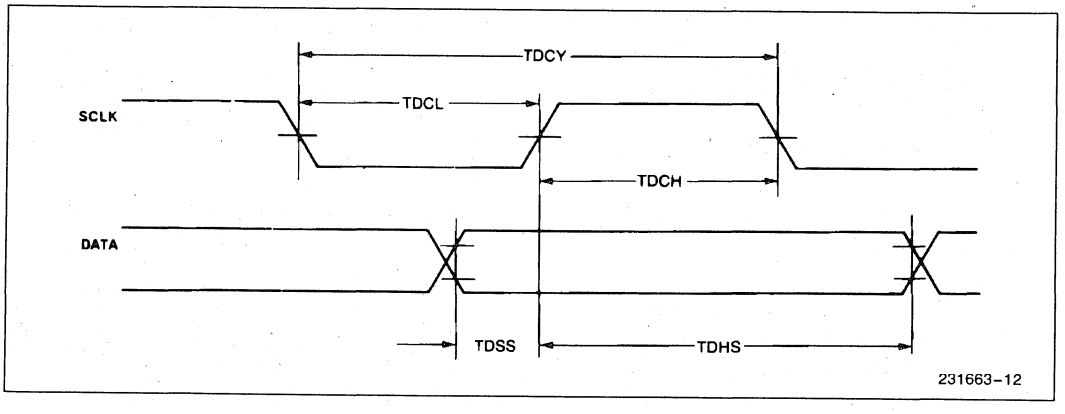


SERIAL I/O WAVEFORMS

SYNCHRONOUS DATA TRANSMISSION

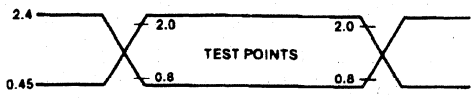


SYNCHRONOUS DATA RECEPTION



AC TESTING INPUT, OUTPUT, FLOAT WAVEFORMS

INPUT/OUTPUT



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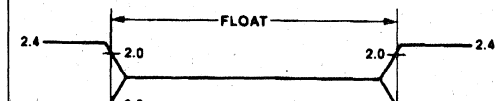
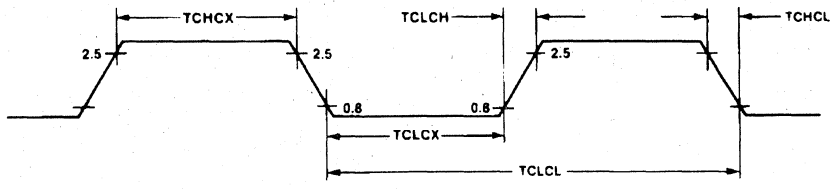
AC testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT



231663-14

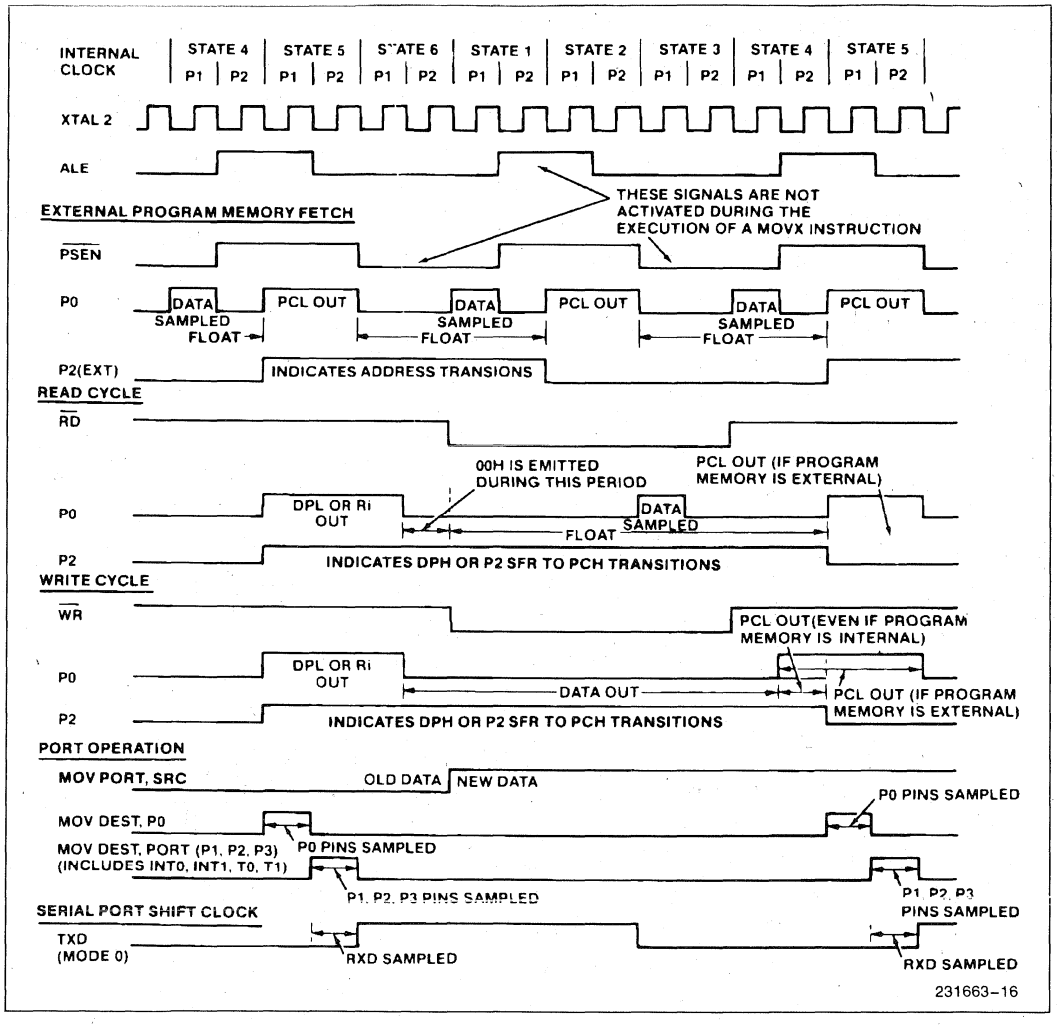
EXTERNAL CLOCK DRIVE XTAL2



231663-15

Symbol	Parameter	Variable Clock Freq = 3.5 MHz to 12 MHz		Unit
		Min	Max	
TCLCL	Oscillator Period	83.3	285.7	ns
TCHCX	High Time	20	TCLCL-TCLCX	ns
TCLCX	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

8744H EPROM CHARACTERISTICS

Erasure Characteristics

Erasure of the 8744H Program Memory begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Ångstroms. Since sunlight and fluorescent lighting have wavelengths in this range, constant exposure to these light sources over an extended period of time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause unintentional erasure. If an application subjects the 8744H to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Ångstroms) to an integrated dose of at least 15 W-sec/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Programming the EPROM

To be programmed, the 8744H must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0-P2.3 of Port 2, while the data byte is applied to Port 0. Pins P2.4-P2.6 and $\overline{PSEN}$ should be held low, and P2.7 and RST high. (These are all TTL levels except RST, which requires 2.5V for high.) $\overline{EA}$/VPP is held normally high, and is pulsed to +21V. While EA/VPP is at 21V, the ALE/$\overline{PROG}$ pin, which is normally being held high, is pulsed low for 50 msec. Then EA/VPP is returned to high. This is illustrated in Figure 8. Detailed timing specifications are provided in the EPROM Programming and Verification Characteristics section of this data sheet.

Program Memory Security

The program memory security feature is developed around a "security bit" in the 8744H EPROM array. Once this "hidden bit" is programmed, electrical access to the contents of the entire program memory array becomes impossible. Activation of this feature is accomplished by programming the 8744H as described in "Programming the EPROM" with the exception that P2.6 is held at a TTL high rather than a TTL low. In addition, Port 1 and P2.0-P2.3 may be in any state. Figure 9 illustrates the security bit programming configuration. Deactivating the security feature, which again allows programmability of the EPROM, is accomplished by exposing the EPROM to ultraviolet light. This exposure, as described in "Erasure Characteristics," erases the entire EPROM array. Therefore, attempted retrieval of "protected code" results in its destruction.

Program Verification

Program Memory may be read only when the "security feature" has not been activated. Refer to Figure 10 for Program Verification setup. To read the Program Memory, the following procedure can be used. The unit must be running with a 4 to 6 MHz oscillator. The address of a Program Memory location to be read is applied to Port 1 and pins P2.0-P2.3 of Port 2. Pins P2.4-P2.6 and $\overline{PSEN}$ are held at TTL low, while the ALE/$\overline{PROG}$, RST, and $\overline{EA}$/VPP pins are held at TTL high. (These are all TTL levels except RST, which requires 2.5V for high.) Port 0 will be the data output lines. P2.7 can be used as a read strobe. While P2.7 is held high, the Port 0 pins float. When P2.7 is strobed low, the contents of the addressed location will appear at Port 0. External pullups (e.g., 10K) are required on Port 0 during program verification.

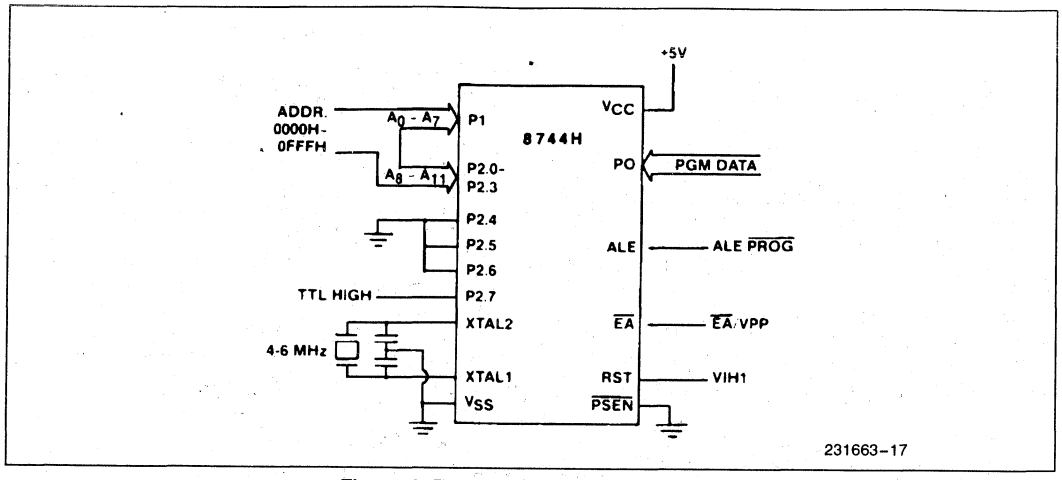


Figure 8. Programming Configuration

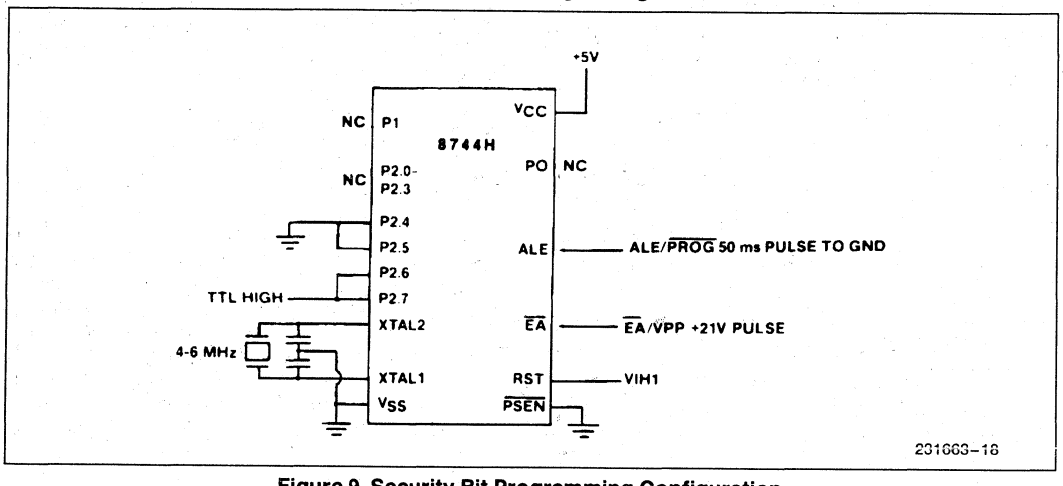


Figure 9. Security Bit Programming Configuration

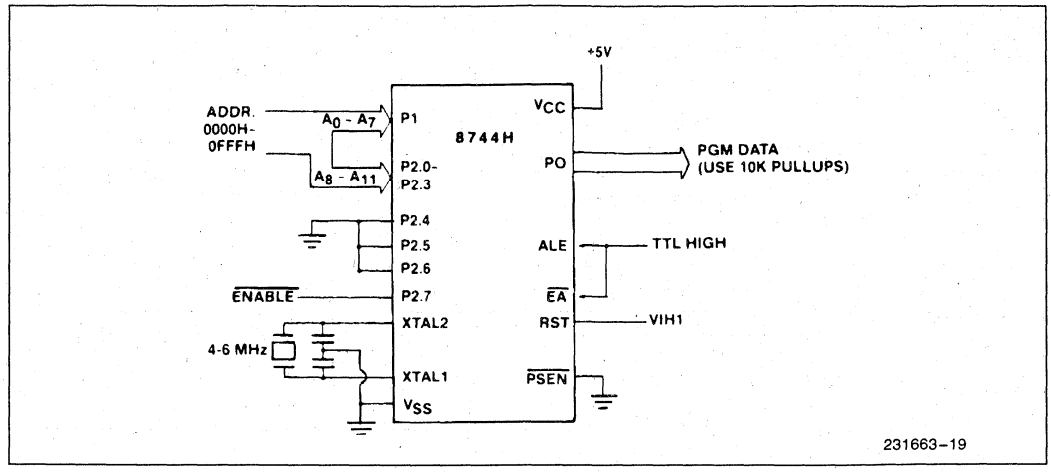


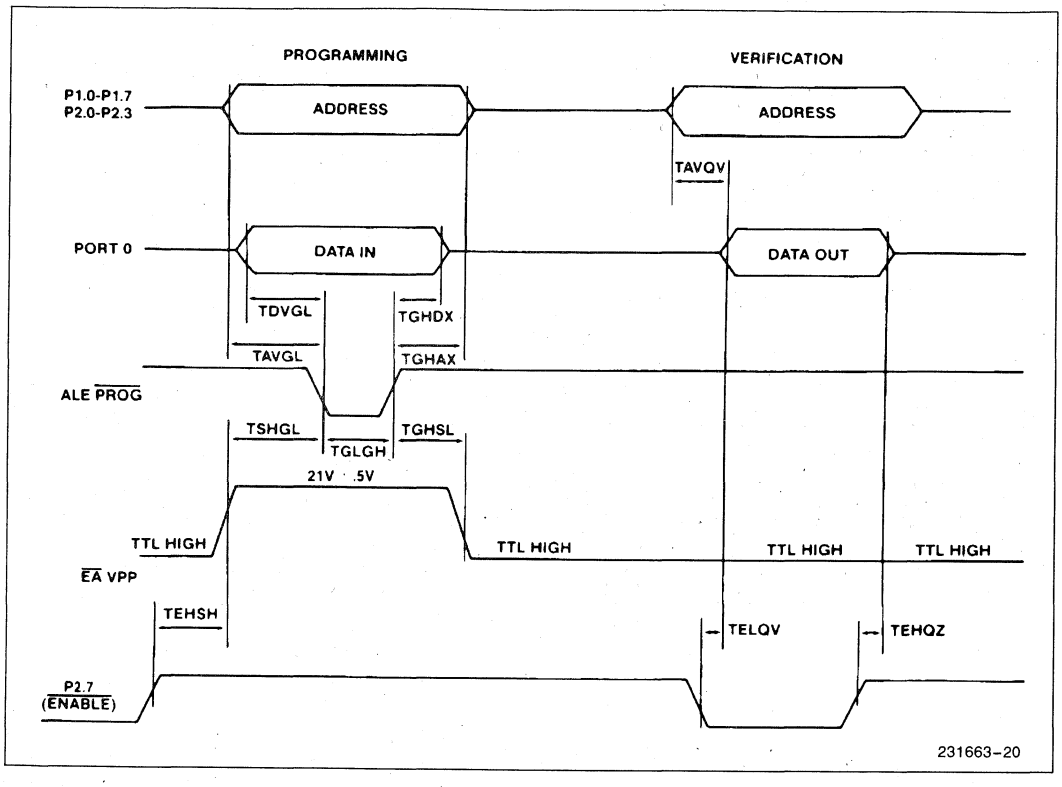
Figure 10. Program Verification Configuration

EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION CHARACTERISTICS

TA = 21°C to 27°C, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	20.5	21.5	V
IPP	Programming Current		30	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	$\overline{ENABLE}$ High to Vpp	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$	10		µsec
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µsec
TGLGH	$\overline{PROG}$ Width	45	55	msec
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ to Data Valid		48TCLCL	
TEHQZ	Data Float after $\overline{ENABLE}$	0	48TCLCL	

EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION WAVEFORMS



82527
SERIAL COMMUNICATIONS CONTROLLER CONTROLLER AREA NETWORK PROTOCOL

Automotive

- **Supports CAN Specification 2.0**
  - **— Standard Data and Remote Frames**
  - **— Extended Data and Remote Frames**
- **Programmable Global Mask**
  - **— Standard Message Identifier**
  - **— Extended Message Identifier**
- **15 Message Objects of 8-Byte Data Length**
  - **— 14 Tx/Rx Buffers**
  - **— 1 Rx Buffer with Programmable Mask**
- **Flexible CPU Interface**
  - **— 8-Bit Multiplexed**
  - **— 16-Bit Multiplexed**
  - **— 8-Bit Non-Multiplexed (Synchronous/Asynchronous)**
  - **— Serial Interface**
- **Programmable Bit Rate**
- **Programmable Clock Output**
- **Flexible Interrupt Structure**
- **Flexible Status Interface**
- **Configurable Output Driver**
- **Configurable Input Comparator**
- **Two 8-Bit Bidirectional I/O Ports**
- **44-Lead PLCC Package**
- **44-Lead QFP Package**
- **Pinout Compatibility with the 82526**

The 82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search, and interrupt search with minimal interaction from the host microcontroller, or CPU.

The 82527 is Intel's first device to support the standard and extended message frames in CAN Specification 2.0 Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames. Due to the backwardly compatible nature of CAN Specification 2.0, the 82527 also fully supports the standard message frames in CAN Specification 2.0 Part A.

The 82527 features a powerful CPU interface that offers flexibility to directly interface to many different CPUs. It can be configured to interface with CPUs using an 8-bit multiplexed, 16-bit multiplexed, or 8-bit non-multiplexed address/data bus for Intel and non-Intel architectures. A flexible serial interface (SPI) is also available when a parallel CPU interface is not required.

The 82527 provides storage for 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object. The last message object is a receive-only buffer with a special mask design to allow select groups of different message identifiers to be received.

The 82527 also implements a global masking feature for message filtering. This feature allows the user to globally mask any identifier bits of the incoming message. The programmable global mask can be used for both standard and extended messages.

The 82527 PLCC offers hardware, or pinout, compatibility with the 82526. It is pin-to-pin compatible with the 82526 except for pins 9, 30, and 44. These pins are used as chip selects on the 82526 and are used as CPU interface mode selection pins on the 82527.

The 82527 is fabricated using Intel's reliable CHMOS III 5V technology and is available in either 44-lead PLCC or 44-lead QFP for the automotive temperature range (−40°C to +125°C).

December 1995

Order Number: 272250-006

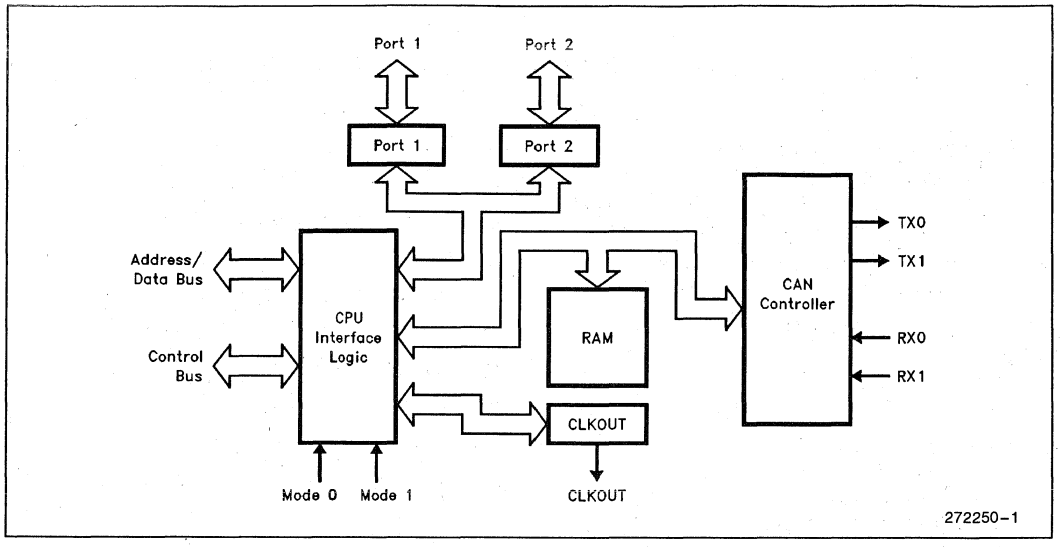


Figure 1. 82527 Block Diagram

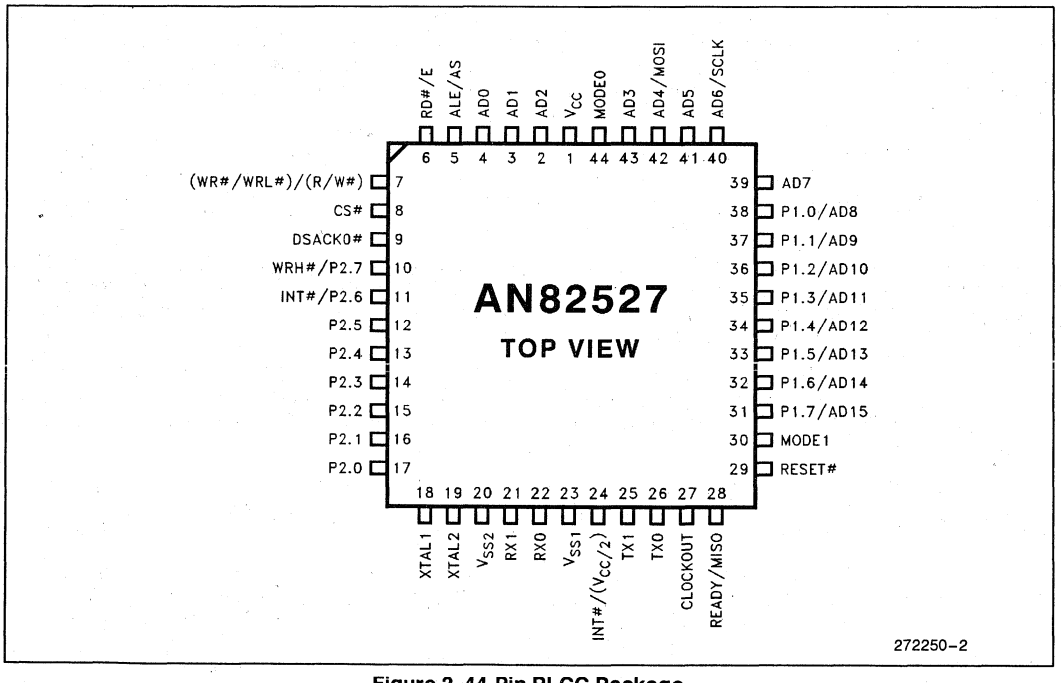


Figure 2. 44-Pin PLCC Package

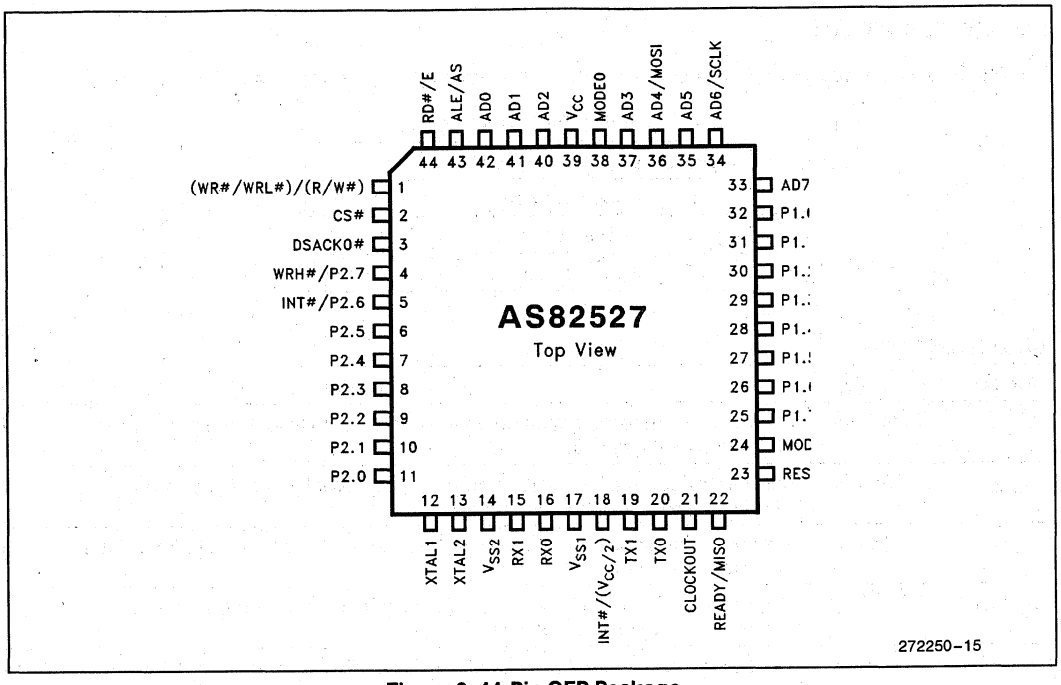


Figure 3. 44-Pin QFP Package

PIN DESCRIPTION

The 82527 pins are described in this section. Table 1 presents the legend for interpreting the pin types.

Table 1. Pin Type Legend

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin can be either input or output

PIN DESCRIPTIONS

Pin Name	Pin Type	Pin Description
V_{SS1}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides digital ground.
V_{SS2}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides ground for analog comparator.
V_{CC}	Power	POWER connection must be connected externally to +5V DC. Provides power for entire device.
XTAL1	I	Input for an external clock. XTAL1 (along with XTAL2) are the crystal connections to an internal oscillator.
XTAL2	O	Push-pull output from the internal oscillator. XTAL2 (along with XTAL1) are the crystal connections to an internal oscillator. If an external oscillator is used XTAL2 must be floated, or not be connected. XTAL2 must not be used as a clock output to drive other CPUs.
CLKOUT	O	Programmable clock output. This output may be used to drive the oscillator of the host microcontroller.
RESET#	I	Warm Reset: (V_{CC} remains valid while RESET# is asserted), RESET# must be driven to a valid low level for 1 ms minimum. Cold Reset: (V_{CC} is driven to a valid level while RESET# is asserted), RESET# must be driven low for 1 ms minimum measured from a valid V_{CC} level. No falling edge on the reset pin is required during a cold reset event.
CS#	I	A low level on this pin enables CPU access to the 82527 device.
INT# (V_{CC}/2)	O O	The interrupt pin is an open-drain output to the host microcontroller. V_{CC}/2 is the power supply for the ISO low speed physical layer. The function of this pin is determined by the MUX bit in the CPU Interface Register (Address 02H) as follows: MUX = 1: pin 24 (PLCC) = V_{CC}/2, pin 11 = INT# MUX = 0: pin 24 (PLCC) = INT#
RX0 RX1	I I	Inputs from the CAN bus line(s) to the input comparator. A recessive level is read when RX0 > RX1. A dominant level is read when RX1 > RX0. When the CoBy bit (Bus Configuration register) is programmed as a "1", the input comparator is bypassed and RX0 is the CAN bus line input.
TX0 TX1	O O	Serial data push-pull output to the CAN bus line. During a recessive bit TX0 is high and TX1 is low. During a dominant bit TX0 is low and TX1 is high.

Pin Name	Pin Type	Pin Description
AD0/A0/ICP AD1/A1/CP AD2/A2/CSAS AD3/A3/STE AD4/A4/MOSI AD5/A5 AD6/A6/SCLK AD7/A7	I/O-I-I I/O-I-I I/O-I-I I/O-I I/O-I-I I/O-I I/O-I-I I/O-I	Address/Data bus in 8-bit multiplexed mode. Address bus in 8-bit non-multiplexed mode. Low byte of A/D bus in 16-bit multiplexed mode. In Serial Interface mode, the following pins have the following meaning: AD0: ICP Idle Clock Polarity AD1: CP Clock Phase AD2: CSAS Chip Select Active State AD3: STE Sync Transmit Enable AD6: SCLK Serial Clock Input AD4: MOSI Serial Data Input
AD8/D0/P1.0 AD9/D1/P1.1 AD10/D2/P1.2 AD11/D3/P1.3 AD12/D4/P1.4 AD13/D5/P1.5 AD14/D6/P1.6 AD15/D7/P1.7	I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O	High byte of A/D bus in 16-bit multiplexed mode. Data bus in 8-bit non-multiplexed mode. Low speed I/O port. P1 pins in 8-bit multiplexed mode and serial mode. Port pins have weak pullups until the port is configured by writing to 9FH and AFH.
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6/INT# P2.7/WRH#	I/O I/O I/O I/O I/O I/O I/O-O I/O-I	P2 in all modes. P2.6 is INT# when MUX = 1 and is open-drain. P2.7 is WRH# in 16-bit multiplexed mode.
Mode0 Mode1	I I	These pins select one of the four parallel interfaces. These pins are weakly held low during reset. **Mode1 Mode0** 0 0 8-bit multiplexed — Intel 0 0 Serial Interface mode entered when RD# = 0, WR# = 0 upon reset. 0 1 16-bit multiplexed — Intel 1 0 8-bit multiplexed — non-Intel 1 1 8-bit non-multiplexed
ALE/AS	I-I	ALE used for Intel modes. AS used for non-Intel modes, except Mode 3 this pin must be tied high.
RD# E	I I	RD# used for Intel modes. E used for non-Intel modes, except Mode 3 Asynchronous this pin must be tied high.
WR#/WRL# R/W#	I I	WR# in 8-bit Intel mode and WRL# in 16-bit Intel mode. R/W# used for non-Intel modes.
READY MISO	O O	READY is an output to synchronize accesses from the host microcontroller to the 82527. READY is an open-drain output to the host microcontroller. MISO is the serial data output for the serial interface mode.
DSACK0#	O	DSACK0# is an open-drain output to synchronize accesses from the host microcontroller to the 82527.

ELECTRICAL CHARACTERISTICS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −60°C to +150°C

Voltage from Any Pin to V_{SS} ..... −0.5V to +7.0V

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Laboratory testing shows the 82527 will withstand up to 10 mA of injected current into both RX0 and RX1 pins for a total of 20 days without sustaining permanent damage. This high current condition may be the result of shorted signal lines. The 82527 will not function properly if the RX0/RX1 input voltage exceeds V_{CC} + 0.5V.

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

Symbol	Parameter	Min	Max	Conditions
V_{IL}	Input Low Voltage (All except RX0, RX1, AD0–AD7 in Mode 3)	−0.5V	0.8V	
V_{IL1}	Input Low Voltage for AD0–AD7 in Mode 3	−0.5V	0.5V	
V_{IL2}	Input Low Voltage (RX0) for Comparator Bypass Mode		0.5V	
V_{IL3}	Input Low Voltage for Port 1 and Port 2 Pins Not Used for Interface to Host CPU		0.3 V_{CC}	
V_{IH}	Input High Voltage (All except RX0, RX1, RESET#)	3.0V	V_{CC} + 0.5V	
V_{IH1}	Input High Voltage (RESET#) Hysteresis on RESET#	3.0V 200 mV	V_{CC} + 0.5V	
V_{IH2}	Input High Voltage (RX0) for Comparator Bypass Mode	4.0V		
V_{IH3}	Input High Voltage for Port 1 and Port 2 Pins Not Used for Interface to Host CPU	0.7 V_{CC}		
V_{OL}	Output Low Voltage (All Outputs except TX0, TX1)		0.45V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (All Outputs except TX0, TX1, CLOCKOUT)	V_{CC} − 0.8V		I_{OH} = −200 μA
V_{OHR1}	Output High Voltage (CLOCKOUT)	0.8 V_{CC}		I_{OH} = −80 μA
I_{LK}	Input Leakage Current		±10 μA	$V_{SS} < V_{IN} < V_{CC}$
C_{IN}	PIN Capacitance**		10 pF	f_{XTAL} = 1 KHz

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

Symbol	Parameter	Min	Max	Conditions
I_{CC}	Supply Current(1)		50 mA	f_{XTAL} = 16 MHz
I_{SLEEP}	Sleep Current(1) with $V_{CC}/2$ Output Enabled, No Load with $V_{CC}/2$ Output Disabled		 700 μA 100 μA	
I_{PD}	Powerdown Current(1)		25 μA	XTAL1 Clocked

NOTES:
**Typical value based on characterization data.
Port pins are weakly held after reset until the port configuration registers are written (9FH, AFH).
1. All pins are driven to V_{SS} or V_{CC} including RX0 and RX1.

PHYSICAL LAYER SPECIFICATIONS Load Condition: 100 pF

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

RX0/RX1 and TX0/TX1	Min	Max	Conditions
Input Voltage	−0.5V	V_{CC} + 0.5V	
Common Mode Range	V_{SS} + 1V	V_{CC} − 1V	
Differential Input Threshold	±100 mV		
Internal Delay 1: Sum of the Comparator Input Delay and the TX0/TX1 Output Driver Delay		60 ns	Load on TX0, TX1 = 100 pF, +100 mV to −100 mV RX0/RX1 differential
Internal Delay 2: Sum of the RX0 Pin Delay (if the Comparator is Bypassed) and the TX0/TX1 Output Driver Delay		50 ns	Load on TX0, TX1 = 100 pF
Source Current on Each TX0, TX1		−10 mA	V_{OUT} = V_{CC} − 1.0V
Sink Current on Each TX0, TX1		10 mA	V_{OUT} = 1.0V
Input Hysteresis for RX0/RX1		0V	
$V_{CC}/2$			
$V_{CC}/2$	2.38V	2.62V	$I_{OUT} \leq 75$ μA, V_{CC} = 5V

CLOCKOUT SPECIFICATIONS

Load Condition: 50 pF

Parameter	Min	Max
CLOCKOUT Frequency	XTAL/15	XTAL

A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Conditions: $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -40°C$ to $+125°C$, $C_L = 100$ pF

Symbol	Parameter	Min	Max	Conditions
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz	
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz	
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz	
t_{AVLL}	Address Valid to ALE Low	7.5 ns		
t_{LLAX}	Address Hold after ALE Low	10 ns		
t_{LHLL}	ALE High Time	30 ns		
t_{LLRL}	ALE Low to RD# Low	20 ns		
t_{CLLL}	CS# Low to ALE Low	10 ns		
t_{QVWH}	Data Setup to WR# High	27 ns		
t_{WHQX}	Input Data Hold after WR# High	10 ns		
t_{WLWH}	WR# Pulse Width	30 ns		
t_{WHLH}	WR# High to Next ALE High	8 ns		
t_{WHCH}	WR# High to CS# High	0 ns		
t_{RLRH}	RD# Pulse Width This time is long enough to initiate a double read cycle by loading the High Speed Registers (04H, 05H), but is too short to READ from 04H and 05H (See t_{RLDV})	40 ns		
t_{RLDV}	RD# Low to Data Valid (Only for Registers 02H, 04H, 05H)	0 ns	55 ns	
t_{RLDV1}	RD# Low Data to Data Valid (for Registers except 02H, 04H, 05H) for Read Cycle without a Previous Write(1) for Read Cycle with a Previous Write(1)		 1.5 t_{MCLK} + 100 ns 3.5 t_{MCLK} + 100 ns	
t_{RHDZ}	Data Float after RD# High	0 ns	45 ns	
t_{CLYV}	CS# Low to READY Setup Condition: Load Capacitance on the READY Output: 50 pF		32 ns 40 ns	$V_{OL} = 1.0V$ $V_{OL} = 0.45V$
t_{WLYZ}	WR# Low to READY Float for a Write Cycle if No Previous Write is Pending(2)		145 ns	
t_{WHYZ}	End of Last Write to READY Float for a Write Cycle if a Previous Write Cycle is Active(2)		2 t_{MCLK} + 100 ns	
t_{RLYZ}	RD# Low to READY Float (for registers except 02H, 04H, 05H) for Read Cycle without a Previous Write(1) for Read Cycle with a Previous Write(1)		 2 t_{MCLK} + 100 ns 4 t_{MCLK} + 100 ns	

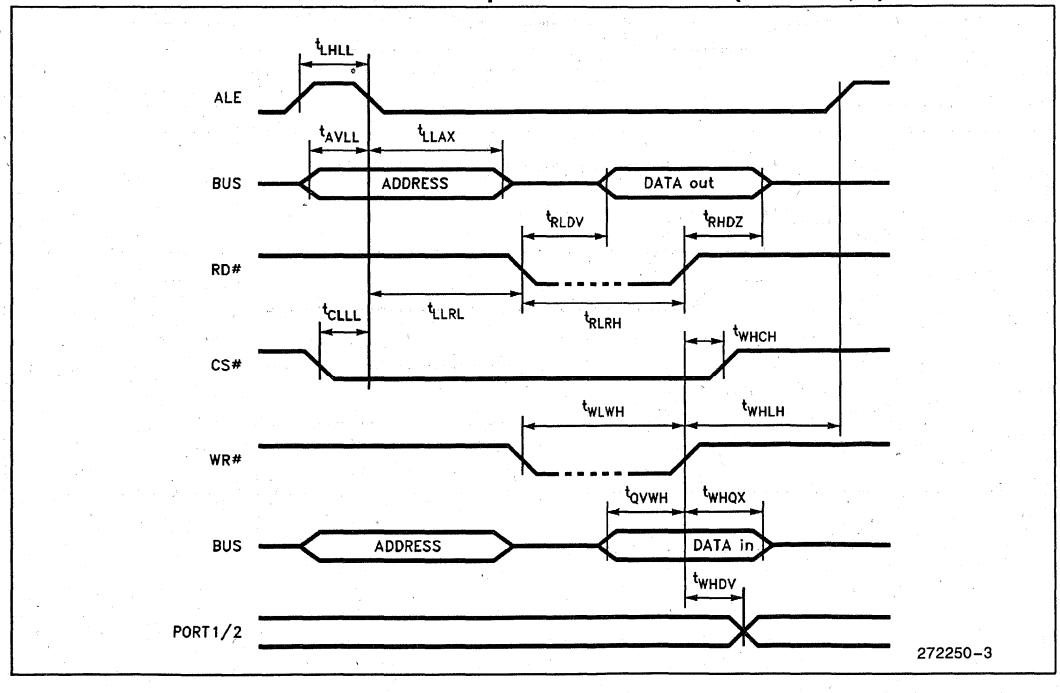
A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF (Continued)

Symbol	Parameter	Min	Max	Conditions
t_{WHDV}	WR# High to Output Data Valid on Port 1/2	t_{MCLK}	2 t_{MCLK} + 500 ns	
t_{COPO}	CLKOUT Period	$(CD_V + 1) * t_{OSC}$(3)		
t_{CHCL}	CLKOUT High Period	$(CD_V + 1) * ½ t_{OSC} - 10$	$(CD_V + 1) * ½ t_{OSC} + 15$	

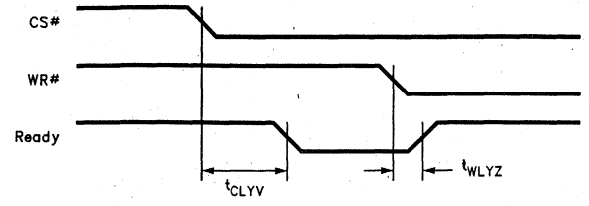
NOTES:
References to WR# also pertain to WRH#.
1. Definition of "read cycle without a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the falling edge of RD# (for the current read cycle) is greater than 2 t_{MCLK}.
2. Definition of "write cycle with a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the rising edge of WR#/WRH# (for the current write cycle) is less than 2 t_{MCLK}.
3. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)



A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Ready Output Timing for a Write Cycle if No Previous Write is Pending



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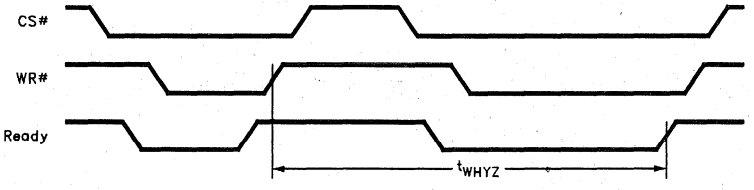
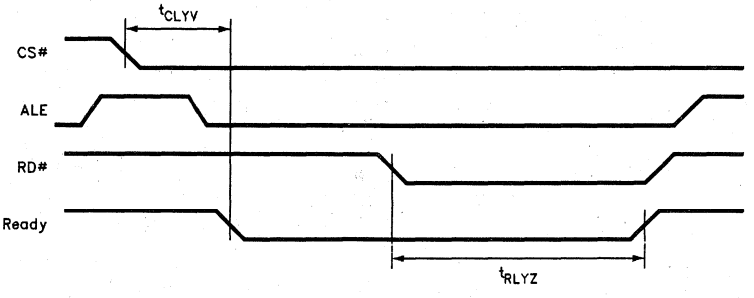
Ready Output Timing for a Write Cycle if a Previous Write Cycle is Active



272250-5

Ready Output Timing for a Read Cycle



272250-6

A.C. Characteristics for 8-Bit Multiplexed Non-Intel Mode (Mode 2)

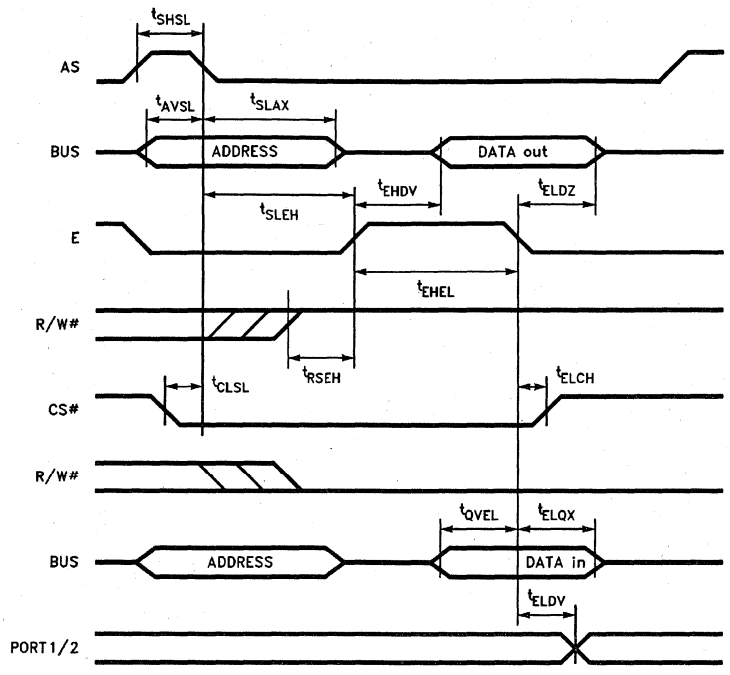
Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVSL}	Address Valid to AS Low	7.5 ns	
t_{SLAX}	Address Hold after AS Low	10 ns	
t_{ELDZ}	Data Float after E Low	0 ns	45 ns
t_{EHDV}	E High to Data Valid for Registers 02H, 04H, 05H	0 ns	45 ns
	for Read Cycle without a Previous Write(1) for Read Cycle with a Previous Write (for Registers except for 02H, 04H, 05H)		$1.5\ t_{MCLK} + 100$ ns $3.5\ t_{MCLK} + 100$ ns
t_{QVEL}	Data Setup to E Low	30 ns	
t_{ELQX}	Input Data Hold after E Low	20 ns	
t_{ELDV}	E Low to Output Data Valid on Port 1/2	t_{MCLK}	$2\ t_{MCLK} + 500$ ns
t_{EHEL}	E High Time	45 ns	
t_{ELEL}	End of Previous Write (Last E Low) to E Low for a Write Cycle	$2\ t_{MCLK}$	
t_{SHSL}	AS High Time	30 ns	
t_{RSEH}	Setup Time of R/W# to E High	30 ns	
t_{SLEH}	AS Low to E High	20 ns	
t_{CLSL}	CS# Low to AS Low	20 ns	
t_{ELCH}	E Low to CS# High	0 ns	
t_{COPD}	CLKOUT Period	$(CD_V + 1) * t_{OSC}$(3)	
t_{CHCL}	CLKOUT High Period	$(CD_V + 1) * ½\ t_{OSC} - 10$	$(CD_V + 1) * ½ t_{OSC} + 15$

NOTES:

1. Definition of "Read Cycle without a Previous Write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than $2\ t_{MCLK}$.
2. Definition of "Write Cycle with a Previous Write": The time between the falling edge of E (for the previous write cycle) and the falling edge of E (for the current write cycle) is less than $2\ t_{MCLK}$.
3. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8-Bit Multiplexed Non-Intel Mode (Mode 2)



A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous (Mode 3)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

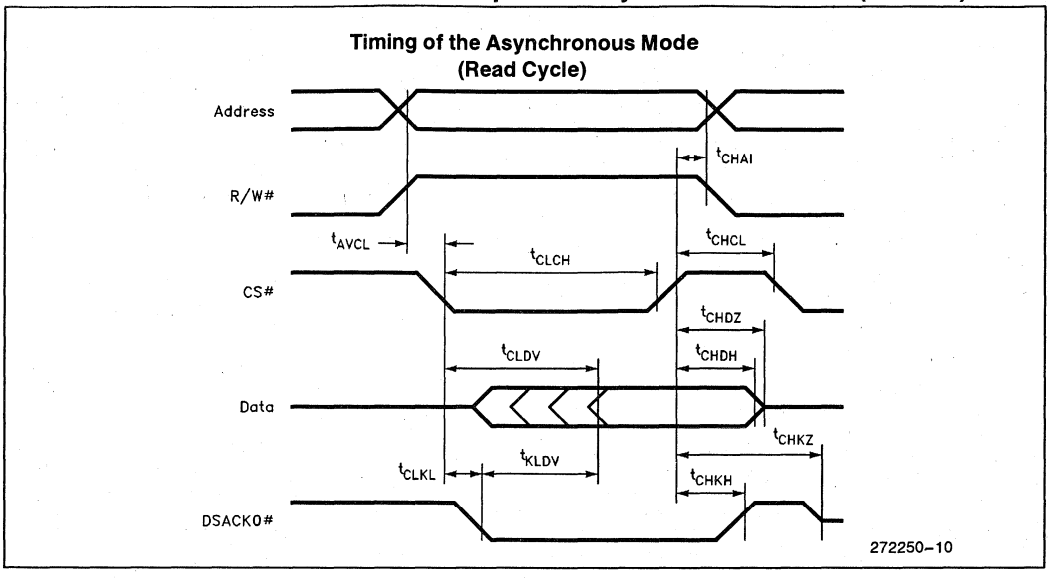
Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVCL}	Address or R/W# Valid to CS# Low Setup	3 ns	
t_{CLDV}	CS# Low to Data Valid for High Speed Registers (02H, 04H, 05H)	0 ns	55 ns
	For Low Speed Registers (Read Cycle without Previous Write)(1)	0 ns	1.5 t_{MCLK} + 100 ns
	For Low Speed Registers (Read Cycle with Previous Write)(1)	0 ns	3.5 t_{MCLK} + 100 ns
t_{KLDV}	DSACK0# Low to Output Data Valid for High Speed Read Register		23 ns
	For Low Speed Read Register	<0 ns	
t_{CHDV}	82527 Input Data Hold after CS# High	15 ns	
t_{CHDH}	82527 Output Data Hold after CS# High	0 ns	
t_{CHDZ}	CS# High to Output Data Float		35 ns
t_{CHKH_1}	CS# High to DSACK0# = 2.4V(3)	0 ns	55 ns
t_{CHKH_2}	CS# High to DSACK0# = 2.8V		150 ns
t_{CHKZ}	CS# High to DSACK0# Float	0 ns	100 ns
t_{CHCL}	CS# Width between Successive Cycles	25 ns	
t_{CHAI}	CS# High to Address Invalid	7 ns	
t_{CHRI}	CS# High to R/W# Invalid	5 ns	
t_{CLCH}	CS# Width Low	65 ns	
t_{DVCH}	CPU Write Data Valid to CS# High	20 ns	
t_{CLKL}	CS# Low to DSACK0# Low for High Speed Registers and Low Speed Registers Write Access without Previous Write(2)	0 ns	67 ns
t_{CHKL}	End of Previous Write (CS# High) to DSACK0# Low for a Write Cycle with a Previous Write(2)	0 ns	2 t_{MCLK} + 145 ns
t_{COPD}	CLKOUT Period	(CD_V + 1) * t_{OSC}(4)	
t_{CHCL}	CLKOUT High Period	(CD_V + 1) * ½ t_{OSC} − 10	(CD_V + 1) * ½ t_{OSC} + 15

NOTES:

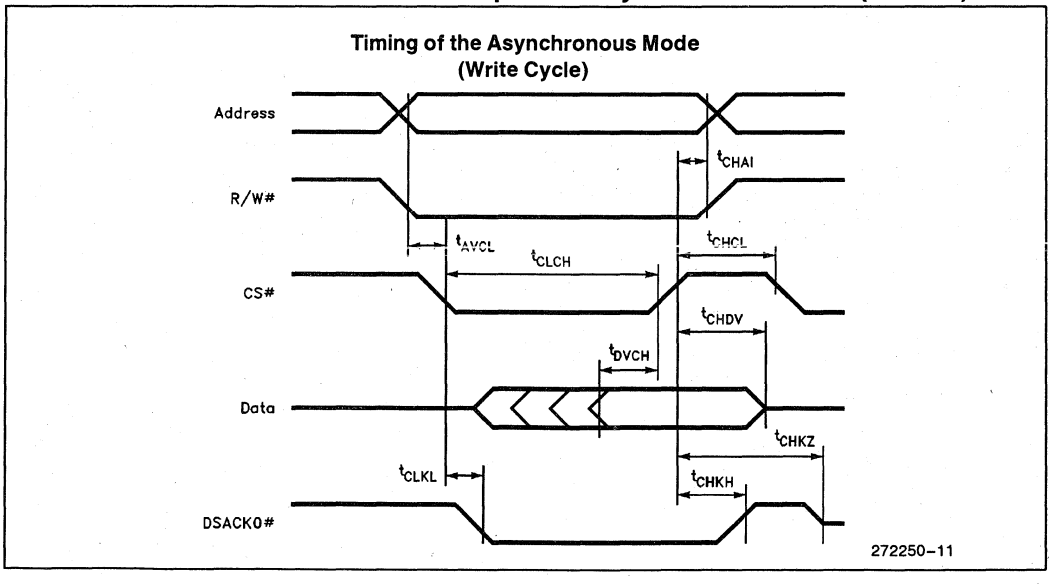
E and AS must be tied high in this mode.

1. Definition of "Read Cycle without a Previous Write": The time between the rising edge of CS# (for the previous write cycle) and the falling edge of CS# (for the current read cycle) is greater than 2 t_{MCLK}.
2. Definition of "Write Cycle without a Previous Write": The time between the rising edge of CS# (for the previous write cycle) and the rising edge of CS# (for the current write cycle) is greater than 2 t_{MCLK}.
3. An on-chip pullup will drive DSACK0# to approximately 2.4V. An external pullup is required to drive this signal to a higher voltage.
4. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3)



A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3)



A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)

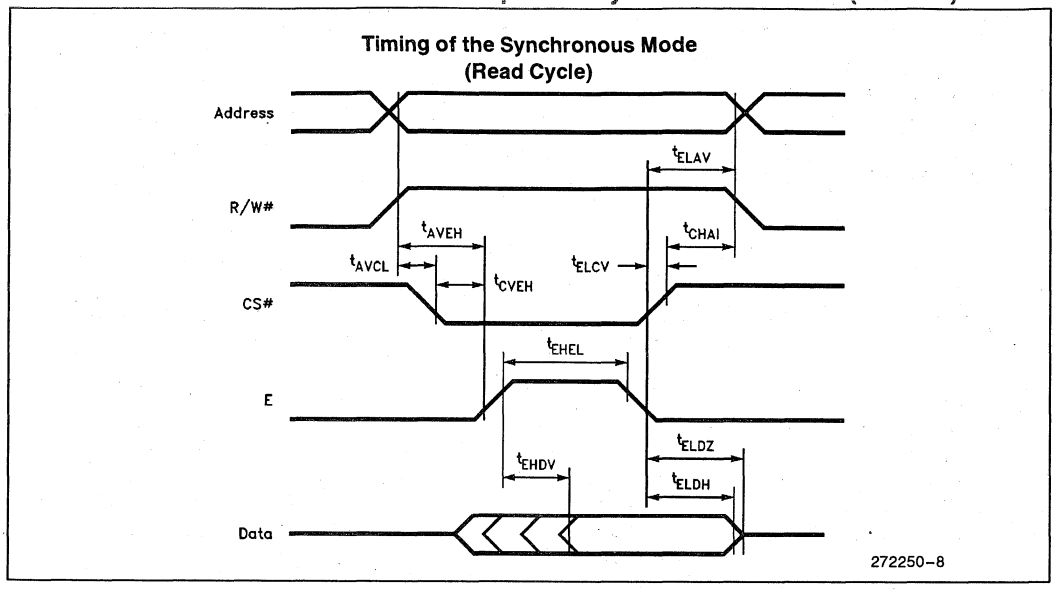
Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{EHDV}	E High to Data Valid out of High Speed Register (02H, 04H, 05H)		55 ns
	Read Cycle without Previous Write for Low Speed Registers(1)		1.5 t_{MCLK} + 100 ns
	Read Cycle with Previous Write for Low Speed Registers(1)		3.5 t_{MCLK} + 100 ns
t_{ELDH}	Data Hold after E Low for a Read Cycle	5 ns	
t_{ELDZ}	Data Float after E Low		35 ns
t_{ELDV}	Data Hold after E Low for a Write Cycle	15 ns	
t_{AVEH}	Address and R/W# to E Setup	25 ns	
t_{ELAV}	Address and R/W# Valid after E Falls	15 ns	
t_{CVEH}	CS# Valid to E High	0 ns	
t_{ELCV}	CS# Valid after E Low	0 ns	
t_{DVEL}	Data Setup to E Low	55 ns	
t_{EHEL}	E Active Width	100 ns	
t_{AVAV}	Start of a Write Cycle after a Previous Write Access	2 t_{MCLK}	
t_{AVCL}	Address or R/W# to CS# Low Setup	3 ns	
t_{CHAI}	CS# High to Address Invalid	7 ns	
t_{COPD}	CLKOUT Period	(CD_V + 1) * t_{OSC}(2)	
t_{CHCL}	CLKOUT High Period	(CD_V + 1) * ½ t_{OSC} − 10	(CD_V + 1) * ½ t_{OSC} + 15

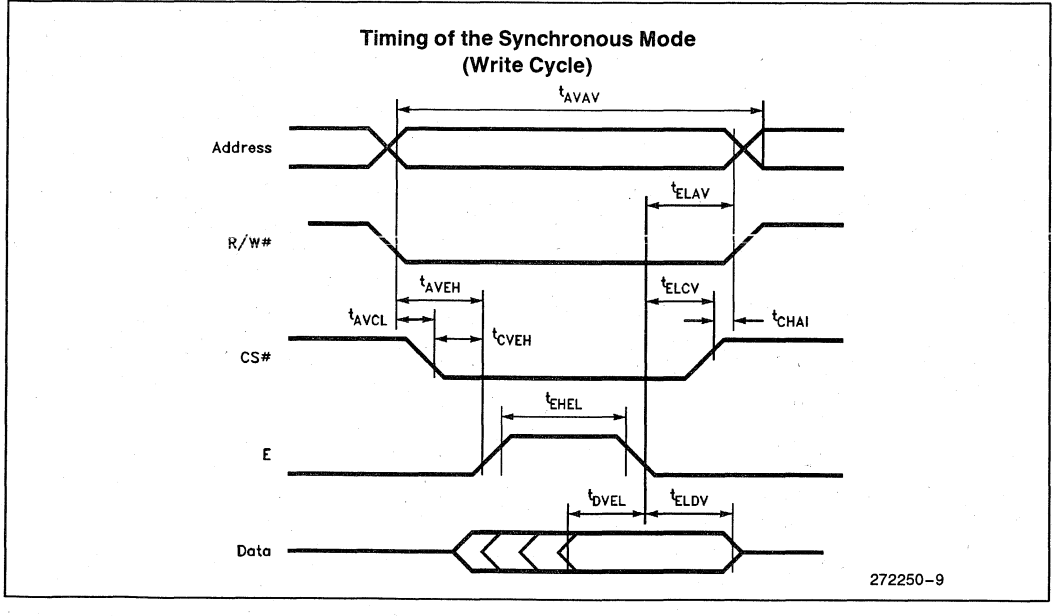
NOTES:

1. Definition of "Read Cycle without a Previous Write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 t_{MCLK}.
2. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)



A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)



A.C. Characteristics for Serial Interface Mode

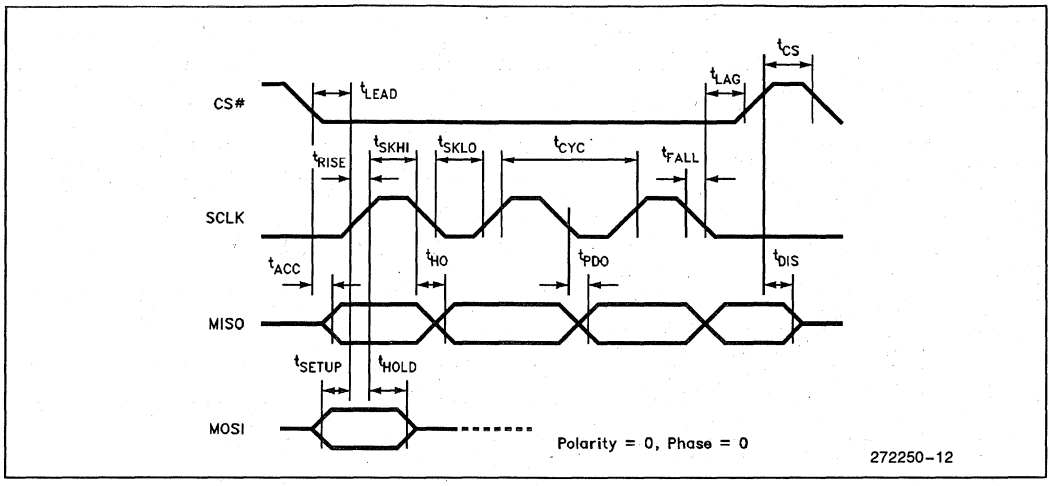
Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

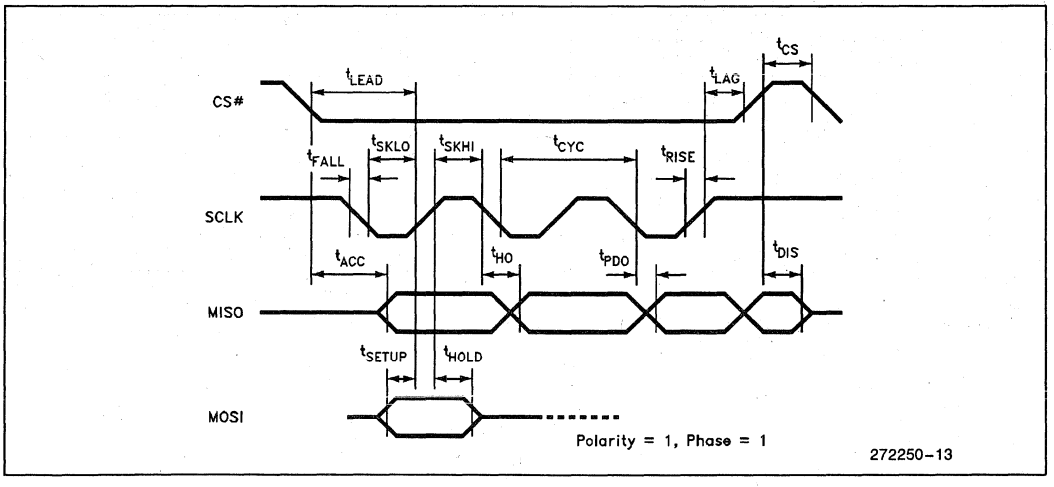
Symbol	Parameter	Min	Max
SCLK	SPI Clock	0.5 MHz	8 MHz
t_{CYC}	1/SCLK	125 ns	2000 ns
t_{SKHI}	Minimum Clock High Time	84 ns	
t_{SKLO}	Minimum Clock Low Time	84 ns	
t_{LEAD}	ENABLE Lead Time	70 ns	
t_{LAG}	Enable Lag Time	109 ns	
t_{ACC}	Access Time		60 ns
t_{PDO}	Maximum Data Out Delay Time		59 ns
t_{HO}	Minimum Data Out Hold Time	0 ns	
t_{DIS}	Maximum Data Out Disable Time		665 ns
t_{SETUP}	Minimum Data Setup Time	35 ns	
t_{HOLD}	Minimum Data Hold Time	84 ns	
t_{RISE}	Maximum Time for Input to go from V_{OL} to V_{OH}		100 ns
t_{FALL}	Maximum Time for Input to go from V_{OH} to V_{OL}		100 ns
t_{CS}	Minimum Time between Consecutive CS# Assertions	670 ns	
t_{COPD}	CLKOUT Period	$(CD_V + 1) * t_{OSC}$(1)	
t_{CHCL}	CLKOUT High Period	$(CD_V + 1) * ½ t_{OSC} - 10$	$(CD_V + 1) * ½ t_{OSC} + 15$

NOTE:

1. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

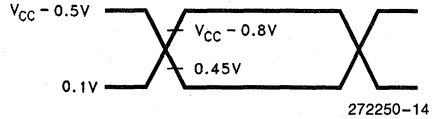
A.C. Characteristics for Serial Interface Mode





A.C. TESTING INPUT

Input, Output Waveforms



NOTE:
AC Inputs during testing are driven at V_{CC} – 0.5V for a Logic "1" and 0.1V for a Logic "0". Timing measurements are made at V_{OH} Min for a Logic "1" and V_{OL} Max for a Logic "0".

DATA SHEET REVISION HISTORY

This is the -006 revision of the 82527 data sheet. The following differences exist between the -005 version and the -006 revision. There were no specification changes between the -004 version and the -005 revision.

1. The 82527 44-ld QFP was added to the product description, the pinmap for the QFP package is also included.
2. The pin numbers were removed from the pin description list to accommodate the new 44-ld QFP package.

3. Removed XTAL1 and XTAL2 from the exceptions for V_{IL} spec. XTAL1 V_{IL} is now specified at min = −0.5V, max = 0.8V. XTAL2 is an output.
4. Removed XTAL1 and XTAL2 from the exceptions for V_{IH} spec. XTAL1 V_{IH} is now specified at min = 3.0V, max = V_{CC} + 0.5V. XTAL2 is an output.
5. Source and Sink current for TX0 and TX1 were corrected from minimum values to maximum values.
6. Mode 2; The t_{AVSL} specification was decreased to 7.5 ns from 33 ns.
7. Mode 2; The t_{SLAX} specification was decreased to 10 ns from 20 ns.
8. Mode 3, Asynchronous; The t_{DVCH} specification was decreased to 20 ns from 32 ns.
9. All modes; Two specifications were added for CLKOUT. These specifications are t_{COPD} (CLKOUT Period) = $(CD_V + 1)*t_{OSC}$, and t_{CHCL} (CLKOUT High Period) = min $(CD_v + 1) * ½ t_{OSC} - 10$ ns and max $(CD_V + 1) * ½ t_{OSC} + 15$ ns. **NOTE:** CD_V represented the value loaded in the lower nibble of the CLKOUT Register (1FH).
10. Serial Interface Mode; The maximum SCLK (SPI Clock) rate was increased to 8 MHz from 4.2 MHz. The minimum t_{CYC} (1/SCLK) was set at 125 ns from 238 ns to reflect the increased maximum SPI clock rate.
11. MODE0/1, the t_{WHQX} Specifications was decreased to 10 ns from 12.5 ns.

This is the -004 revision of the 82527 data sheet. The following differences exist between the -003 version and the -004 revision.

1. Remove notice on page 1 concerning Advance Information Data Sheet.
2. Page 4, AS pin description, add "pin tied high in Asycnhronous mode 3".
3. Page 4, E pin description, add "pin tied high in mode 3".
4. Page 5, add V_{IH} = 0.7 V_{CC} and V_{IL} = 0.3 V_{CC} for LSIO port pins (pins not used to interface to host-CPU).
5. Page 6, change Differential Input Threshold from MAX spec to MIN spec.
6. Page 6, add Input Hysteresis spec for RX0/RX1 = 0V maximum.
7. Page 7, t_{LLAX} decreased from 20 ns to 10 ns (to interface to 20 MHz C196).
8. Page 7, t_{QVWH} decreased from 30 ns to 27 ns (to interface to 20 MHz C196).
9. Page 7, t_{WLWH} decreased from 40 ns to 30 ns (to interface to 20 MHz C196).
10. Page 7, t_{RLDV} increased from 45 ns to 55 ns.
11. Page 12, t_{CHKH} specification added for V_{IH} = 2.8V = 150 ns.
12. Page 12, t_{CHAI} decreased from 10 ns to 7 ns.
13. Page 13, timing diagram for t_{AVCL} revised to show common CL low level.
14. Page 14, t_{CHAI} decreased from 10 ns to 7 ns.

15. Page 7, t_{CLLL} decreased from 20 ns to 10 ns.
16. Page 3, RESET# description addition:

    Warm reset: (V_{CC} remains valid while RESET# is asserted), RESET# must be driven to a valid low level for 1 ms minimum.

    Cold reset: (V_{CC} is driven to a valid level while RESET# is asserted, RESET# must be driven low for 1 ms minimum measured from a valid V_{CC} level. No falling edge on the reset pin is required during a cold reset event.
17. Page 2, Figure 2: Pin 7 name changed to (WR#/WRL#)/(R/W#) from WR#/(R/W#).
18. Page 4, pin description name changed to (WR#/WRL#)/(R/W#) from WR#/(R/W#) and WR# in 8-bit Intel mode and WRL# in 16-bit Intel mode replaces the description WR# used for Intel modes.
19. Page 5, ABSOLUTE MAXIMUM RATINGS addition: Laboratory testing shows the 82527 will withstand up to 10 mA for injected current into both RX0 and RX1 pins for a total of 20 days without sustaining permanent damage. This high current condition may be the result of shorted signal lines. The 82527 will not function properly if the RX0/RX1 input voltage exceeds V_{CC} + 0.5V.
20. Page 12, t_{CHDV} decreased from 25 ns to 15 ns.
21. Page 14, t_{ELDV} decreased from 25 ns to 15 ns.
22. Page 7, t_{AVLL} decreased from 20 ns to 7.5 ns.
23. Page 7, t_{WHQX} decreased from 20 ns to 12.5 ns.

This is the -003 revision of the 82527 data sheet. The following differences exist between the -002 version and the -003 revision.

1. The data sheet has been revised to ADVANCE from PRELIMINARY, indicating the specifications have been verified through electrical tests.
2. ABSOLUTE MAXIMUM RATINGS have been added.
3. V_{IL} no longer applies to the AD0–AD7 pins in CPU Interface mode 3.
4. V_{IL1} has been added to specify Input Low Voltage for AD0–AD7 pins in CPU Interface mode 3 as −0.5V minimum and +0.5V maximum.
5. I_{CC} supply current has been reduced to 50 mA from 100 mA.
6. Note 2 was added stating during I_{PD} testing, all pins are driven to V_{SS} or V_{CC}, including RX0 and RX1.
7. t_{AVLL} has been decreased to 20 ns from 33 ns.
8. t_{RLDV1} has been decreased to 1.5 t_{MCLK} + 100 ns from 2 t_{MCLK} + 100 ns for a Read Cycle without a previous Write (Modes 0, 1).

   t_{RLDV1} has been decreased to 3.5 t_{MCLK} + 100 ns from 4 t_{MCLK} + 100 ns for a Read Cycle with a previous Write (Modes 0, 1).
9. t_{CLYV} has added the condition of V_{OL} = 1.0V for a 32 ns delay. t_{CLYV} is 40 ns for V_{OL} = 0.45 (Modes 0, 1).
10. t_{WHYZ} has been decreased to 2 t_{MCLK} + 100 ns from 2 t_{MCLK} + 145 ns (Modes 0, 1).
11. t_{EHDV} has been decreased to 1.5 t_{MCLK} + 100 ns from 2 t_{MCLK} + 100 ns for a Read Cycle without a previous Write (Mode 2).

    t_{EHDV} has been decreased to 3.5 t_{MCLK} + 100 ns from 4 t_{MCLK} + 100 ns for a Read Cycle with a previous Write (Mode 2).
12. t_{ELEL} has been decreased to 2 t_{MCLK} from 2 t_{MCLK} + 145 ns (Mode 2).
13. t_{CLDV} has been decreased to 55 ns from 65 ns (Mode 3).
14. t_{CHKH} is specified for V_{IH} = 2.4V, decreased from V_{IH} = 3.0V. Note 3 has been added which states an on-chip pullup will drive DSACK0# to approximately 2.4V. An external pullup is required to drive this signal to a higher voltage (Mode 3).
15. t_{CHAI} has been increased to 10 ns from 5 ns. t_{CHAI} no longer includes CS# High to R/W# Invalid (Mode 3).
16. t_{CHRI} = 5 ns has been added to specify CS# High to R/W# Invalid (Mode 3).
17. t_{EHDV} has been decreased to 55 ns from 65 ns for Reads of the High Speed Registers (Mode 3).
18. t_{EHDV} has been decreased to 1.5 t_{MCLK} + 100 ns from 2 t_{MCLK} + 100 ns for a Read Cycle without a previous Write (Mode 3).

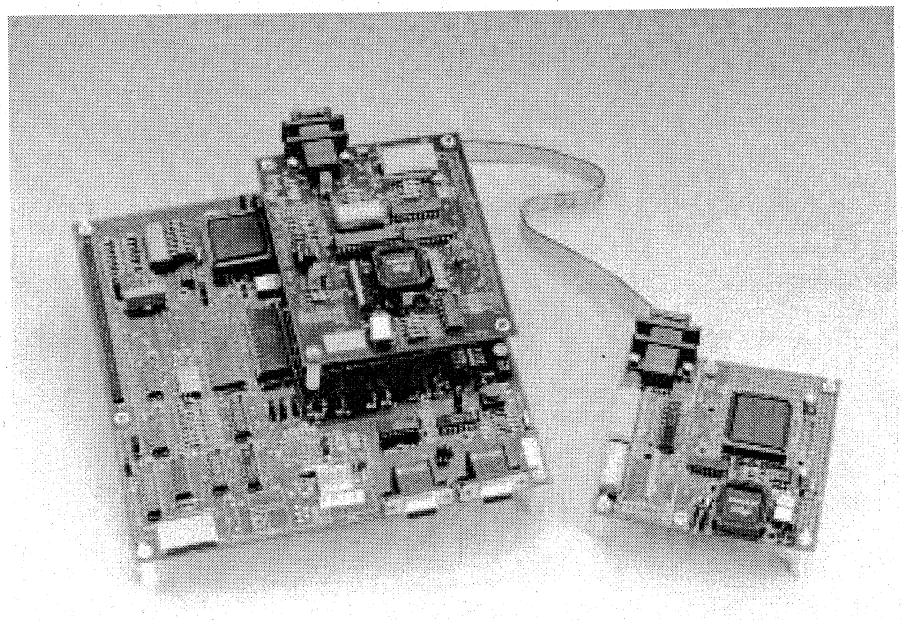
    t_{EHDV} has been decreased to 3.5 t_{MCLK} + 100 ns from 4 t_{MCLK} + 100 ns for a Read Cycle with a previous Write (Mode 3).
19. The t_{AVAL} specification name has been corrected to t_{AVAV} (Mode 3).
20. t_{CHAI} has been increased to 10 ns from 5 ns (Mode 3).
21. The input voltage in the A.C. Testing Input Diagram have been revised to V_{CC} − 0.5V from 3.0V (high level) and revised to 0.1V from 0.8V (low level).

The following differences exist between the -001 version and the -002 revision.

1. The RAM block in Figure 1. 82527 Block Diagram was previously called DPRAM.
2. The INT#/(V_{CC}/2) pin in Figure 2. 44-Pin PLCC Package and in other descriptions was previously called the INT#/(V_{DD}/2) pin.
3. The Mode0 and Mode1 pin descriptions were modified to include the following note: These pins are weakly held low during reset.
4. The DSACK0# pin description was changed to reflect an open-drain output.
5. V_{IL1} for RX0 in comparator bypass mode was added.
6. V_{IH1} hysteresis on RESET# was added.
7. V_{IH2} for RX0 in comparator bypass mode was added.
8. I_{SLEEP} current with V_{CC}/2 output enabled was corrected from 700 μA minimum to 700 μA maximum.
9. I_{SLEEP} current with V_{CC}/2 output disabled was corrected from 100 μA minimum to 100 μA maximum.
10. I_{PD} current was changed from 10 μA minimum to 25 μA maximum.
11. The following note was added to the electrical characteristics: Port pins are weakly held high after reset until the port configuration registers are written (9FH, AFH).
12. The following D.C. Characteristics Specifications have been removed and replaced by the Internal Delay 1 and Internal Delay 2 specifications. These specifications reflect the production test methodology which requires these two delays to be tested together.
    a. Delay Dominant to Recessive
    b. Delay Recessive to Dominant
    c. Input Delay with Comparator Bypassed
    d. Rise Time
    e. Fall Time
13. The following A.C. Characteristics for 8-Bit/16-Bit Multiplexed Intel Modes (Modes 0,1) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{LLAX} has been decreased to 20 ns from 22.5 ns.
    c. t_{LLRL} has been increased to 20 ns from 0 ns.
    d. t_{CLLL} has been added.
    e. t_{WHLH} has been increased to 8 ns from 0 ns.
    f. t_{WHCH} has been added.
    g. t_{RLDV1} has been added.
    h. t_{WLYH} has been changed to t_{WLYZ} to reflect the READY pin is an open-drain output.
    i. t_{WHYH} has been changed to t_{WHYZ} to reflect the READY pin is an open-drain output.
    j. t_{RLYH} has been changed to t_{RLYZ} to reflect the READY pin is an open-drain output.
    k. t_{WHDV} has been increased to 2 t_{MCLK} + 250 ns from 2 t_{MCLK} + 100 ns.
    l. The following note was added: References to WR# also pertain to WRH#.
    m. The following definition was added for a "read cycle without a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the falling edge of RD# (for the current read cycle) is greater than 2 t_{MCLK}.
    n. The following definition was added for a "write cycle with a previous write": The time between the rising edge of WR#/WRH# (for the previous write cycle) and the next rising edge of WR#/WRH# (for the current write cycle) is less than 2 t_{MCLK}.

14. The timing diagrams for 8-Bit/16-Bit Multiplexed Intel Modes (Modes 0,1) have been changed to show ALE rising before CS# falls.
15. The following A.C. Characteristics for 8-Bit Multiplexed Non-Intel Modes (Modes 2) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{SLAX} has been decreased to 20 ns from 22.5 ns.
    c. t_{EVDV} has been decreased to (2, 4) t_{MCLK} + 100 ns from (2, 4) t_{MCLK} + 145 ns.
    d. t_{ELDV} minimum has been decreased to t_{MCLK} from t_{MCLK} + 100 ns.
    e. t_{ELDV} maximum has been increased to 2 t_{MCLK} + 500 ns from 2 t_{MCLK} + 100 ns.
    f. t_{EHEL} for registers except 02H, 04H, 05H has been renamed to t_{ELEL} and the specification has been decreased to 2 t_{MCLK} + 145 ns from 4 t_{MCLK} + 145 ns.
    g. t_{SLEH} has been increased to 20 ns from 0 ns.
    h. t_{CLSL} has been added.
    i. t_{ELCH} has been added.
    j. The following definition was added for a "read cycle without a previous write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 t_{MCLK}.
    k. The following definition was added for a "write cycle with a previous write": The time between the falling edge of E (for the previous write cycle) and the next falling edge of E (for the current write cycle) is less than 2 t_{MCLK}.
16. The following A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{CLDV} has been decreased for low speed registers to (2, 4) t_{MCLK} + 100 ns from (2, 4) t_{MCLK} + 145 ns.
    c. t_{CHKH} comment "with 3.3 KΩ Pullup and 100 pF Load" has been removed since t_{CHKH} is tested with a current source.
    d. t_{CLKL} for a Write Access with a Previous Write has been renamed to t_{CHKL}.
    e. The note "E and AS must be tied high in this mode" has been added.
    f. The following definition was added for a "read cycle without a previous write": The time between the rising edge of CS# (for the previous write cycle) and the falling edge of CS# (for the current read cycle) is greater than 2 t_{MCLK}.
    g. The following definition was added for a "write cycle with a previous write": The time between the rising edge of CS# (for the previous write cycle) and the next rising edge of CS# (for the current write cycle) is less than 2 t_{MCLK}.
17. The following A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3) have been changed:
    a. $1/t_{MCLK}$ has been increased to 8 MHz from 5 MHz.
    b. t_{ELDZ} minimum has been removed.
    c. t_{AVCL} has been added.
    d. t_{CHAI} has been added.
    e. The following definition was added for a "read cycle without a previous write": The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 t_{MCLK}.
    f. The following definition was added for a "write cycle with a previous write": The time between the falling edge of E (for the previous write cycle) and the next falling edge of E (for the current write cycle) is less than 2 t_{MCLK}.
18. The following A.C. Characteristics for Serial Interface Mode have been changed:
    a. t_{SKHI} has been decreased to 84 ns from 119 ns.
    b. t_{SKLO} has been decreased to 84 ns from 119 ns.
    c. t_{PDO} has been decreased to 59 ns from 84 ns.
    d. t_{SETUP} has been decreased to 35 ns from 59 ns.
    e. t_{HOLD} has been decreased to 84 ns from 109 ns.
19. The note in the A.C. Testing Input diagram referenced V_{OH} was previously named V_{IH}.

EV82527 EVALUATION KIT



272263-01

The EV82527 evaluation kit demonstrates the capabilities of the 82527 serial communications controller and the Controller Area Network (CAN) protocol. This evaluation kit represents a quick approach to learning the features of the 82527 device and CAN Specification 2.0 29-bit message identifiers.

DESCRIPTION

The EV82527 evaluation kit features the 82527 device and the CAN protocol, Specification 2.0. The 82527 device implements CAN Specification 2.0 and is optimized to allow the host microcontroller to remain dedicated to its application control function. The host microcontroller interface to the 82527 is analogous to that of a RAM. The transmission, reception and error confinement routines are hardwired in the 82527 and are transparent to the user.

FEATURES

The EV82527 evaluation kit consists of three boards: an EV87C196KR motherboard, an 82527 daughterboard and a DV82527 satellite board, plus a software monitor that assembles MCS®-96 code online.

- The motherboard is a fully functional evaluation board which contains the host microcontroller, the Intel 87C196KR.
- The daughterboard is configured with an RS-485 CAN bus interface and can be easily adapted to other physical layer implementations.
- The daughterboard communicates with a DV82527 satellite board acting as an additional network node. The satellite board requires no host-CPU programming and uses dip switches to choose various communication options.

BENEFITS

- Quick setup and installation
- Interfaces to high performance 16-bit host-CPU

October 1992
Order Number: 272263-001

intel

EV82527 EVALUATION KIT

- Assists the development of CAN application software
- Demonstrates CAN Specification 2.0 protocol and features
- Uses standard Personal Computer host

87C196KR MOTHERBOARD

Assembly language programs for the 87C196KR motherboard may be downloaded to the microcontroller and executed. The monitor program has the following features:

- Program loading
- Program disassembly
- In-monitor assembler that allows program to be written on-line
- 16 breakpoints
- Single-stepping
- Specific commands to interrogate 82527 messages and status

The 87C916KR is a powerful 16-bit microcontroller with high speed I/O, an A/D converter, full duplex serial I/O (synchronous and asynchronous), 768 bytes of RAM and 16 Kbytes of EPROM.

82527 DAUGHTERBOARD

The interface between the 82527 CAN device and the 87C196KR microcontroller is completed by connecting the mother and daughterboards together. The 82527 device interfaces to the 87C196KR using either an 8- or 16-bit multiplexed address/data bus.

CAN bus communication utilizes the on-board RS-485 interface or connects to a user defined physical interface.

The two 8-bit I/O ports of the 82527 device connect to dip switches or LED displays allowing the user to change or monitor the operation of the 82527 and the 87C196KR devices.

DV82527 SATELLITE BOARD

The daughterboard connects to a satellite board via a cable serving as the CAN bus. It executes a series of fixed programs which are user-selected dip switches. The satellite board receives and transmits one-byte messages of either 11- or 29-bit message identifier format. Messages may use one of four possible message identifiers. The satellite sends remote frames as well.

The reception and transmission of satellite board messages is monitored on LED displays.

PERSONAL COMPUTER REQUIREMENTS

The EV82527 evaluation kit is hosted on an IBM PC AT, XT or BIOS-compatible clone. The PC must meet the following requirements:

- 512 Kbytes of memory
- One 1.2 Meg floppy Disk Drive
- MS-DOS 3.0 or later
- A serial (COM1 or COM2) at 9600 baud
- ASM-96, iC-96 or PL/M-96 or any 8096 Assembler/Compiler that generates Object Module Format code
- A text editor such as AEDIT

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